LME49600 High-Performance, High-Fidelity, High-Current Headphone Buffer

Check for Samples: LME49600

FEATURES

- **Pin-Selectable Bandwidth and Quiescent Current**
- **Pure Fidelity, Pure Performance**
- **Short Circuit Protection**
- **Thermal Shutdown**
- **TO–263 Surface-Mount Package**

APPLICATIONS

- **Headphone Amplifier Output Drive Stage**
- **Line Drivers**
- **Low Power Audio Amplifiers**
- **High-Current Operational Amplifier Output Stage**
- **ATE Pin Driver Buffer**
- **Power Supply Regulator**

DESCRIPTION

The LME49600 is a high performance, low distortion high fidelity 250mA audio buffer. The LME49600 is designed for a wide range of applications. It can be used inside the feedback loop of op amps.

The LME49600 offers a pin-selectable bandwidth: a low current, 110MHz bandwidth mode that consumes 7.3mA and a wide 180MHz bandwidth mode that consumes 13.2mA. In both modes the LME49600 has a nominal 2000V/µs slew rate. Bandwidth is easily adjusted by either leaving the BW pin unconnected or connecting a resistor between the BW pin and the V_{EE} pin.

The LME49600 is fully protected through internal current limit and thermal shutdown.

KEY SPECIFICATIONS

- **Low THD+N (V_{OUT} = 3V_{RMS}, f = 1kHz, Figure 26): 0.00003% (typ)**
- **Slew Rate: 2000V/µs (typ)**
- **High Output Current: 250mA (typ)**
- **Bandwidth**
  - **BW Pin Floating: 110MHz (typ)**
  - **BW Connected to V_{EE}: 180MHz (typ)**
- **Supply Voltage Range: ±2.25V ≤ V_S ≤ ±18V**

Typical Application Diagram

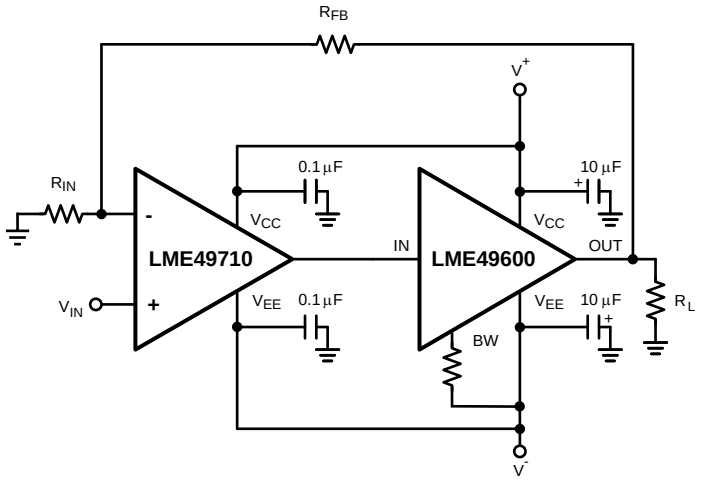


Figure 1. High Performance, High Fidelity LME49600 Audio Buffer Application

Functional Block Diagram

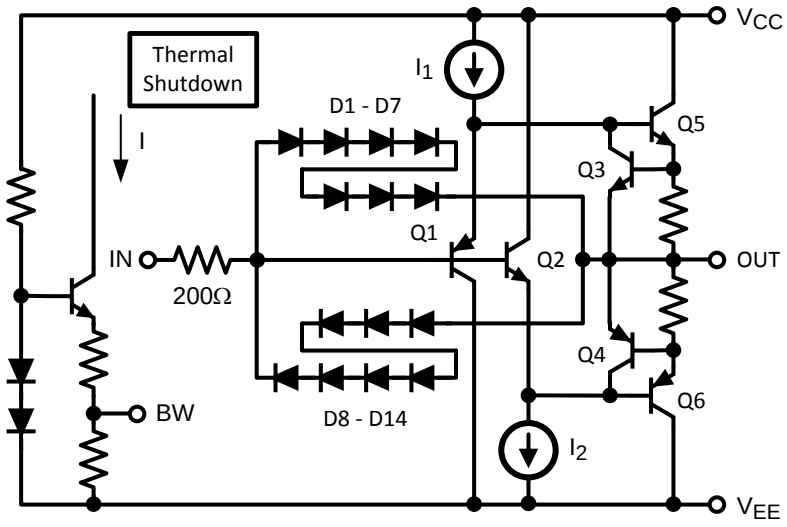
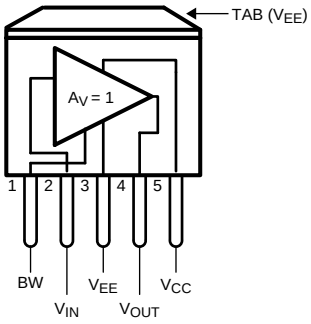


Figure 2. Simplified Circuit Diagram (Note: I_1 and I_2 are mirrored from I)

Connection Diagram



The KTT package is non-isolated package. The package's metal back and any heat sink to which it is mounted are connected to the same potential as the $-V_{EE}$ pin.

Figure 3. KTT Package (Top View)
See Package Number KTT0005B

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

Supply Voltage		±20V
ESD Ratings(4)		2000V
ESD Rating(5)		200V
Storage Temperature		−40°C to +150°C
Junction Temperature		150°C
Thermal Resistance	θ_{JC}	4°C/W
	θ_{JA}	65°C/W
	θ_{JA}(6)	20°C/W
Soldering Information	TO-263 Package (10 seconds)	260°C

(1) All voltages are measured with respect to ground, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine Model, 220pF – 240pF discharged through all pins.
(6) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX}–T_A)/\theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LME49600, typical application (shown in Figure 26) with V_{SUPPLY} = 30V, R_L = 32Ω, the total power dissipation is 1.9W. θ_{JA} = 20°C/W for the TO–263 package mounted to 16in^2 1oz copper surface heat sink area.

OPERATING RATINGS(1)(2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	−40°C ≤ T_A ≤ 85°C
Supply Voltage		±2.25V to ±18V

(1) All voltages are measured with respect to ground, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.

SYSTEM ELECTRICAL CHARACTERISTICS FOR LME49600

The following specifications apply for V_S = ±15V, f_{IN} = 1kHz, unless otherwise specified. Typicals and limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LME49600		Units (Limits)
			Typical (1)	Limit (2)	
I_Q	Total Quiescent Current	I_{OUT} = 0 BW pin: No connect BW pin: Connected to V_{EE} pin	 7.3 13.2	 10.5 18	 mA (max) mA (max)
THD+N	Total Harmonic Distortion + Noise (3)	A_V = 1, V_{OUT} = 3V_{RMS}, R_L = 32Ω, BW = 80kHz, closed loop see Figure 26. f = 1kHz f = 20kHz	 0.000035 0.0005		 % %
SR	Slew Rate	30 ≤ BW ≤ 180MHz V_{OUT} = 20V_{P-P}, R_L = 100Ω	2000		V/µs
BW	Bandwidth	A_V = –3dB BW pin: No Connect R_L = 100Ω R_L = 1kΩ	 100 110		 MHz MHz
		A_V = –3dB BW pin: Connected to V_{EE} pin R_L = 100Ω R_L = 1kΩ	 160 180		 MHz MHz
	Voltage Noise Density	f = 10kHz BW pin: No Connect	3.0		nV/√Hz
		f = 10kHz BW pin: Connected to V_{EE} pin	2.6		nV/√Hz
t_s	Settling Time	ΔV = 10V, R_L = 100Ω 1% Accuracy BW pin: No connect BW pin: Connected to V_{EE} pin	 200 60		 ns ns
A_V	Voltage Gain	V_{OUT} = ±10V R_L = 67Ω R_L = 100Ω R_L = 1kΩ	 0.93 0.95 0.99	 0.90 0.92 0.98	 V/V (min) V/V (min) V/V (min)
V_{OUT}	Voltage Output	Positive I_{OUT} = 10mA I_{OUT} = 100mA I_{OUT} = 150mA	 V_{CC} –1.4 V_{CC} –2.0 V_{CC} –2.3	 V_{CC} –1.6 V_{CC} –2.1 V_{CC} –2.7	 V (min) V (min) V (min)
		Negative I_{OUT} = –10mA I_{OUT} = –100mA I_{OUT} = –150mA	 V_{EE} +1.5 V_{EE} +3.1 V_{EE} +3.5	 V_{EE} +1.6 V_{EE} +2.4 V_{EE} +3.2	 V (min) V (min) V (min)
I_{OUT}	Output Current		±250		mA
I_{OUT-SC}	Short Circuit Output Current	BW pin: No Connect BW pin: Connected to V_{EE} pin	±490 ±490	 ±550	mA (max) mA (max)
I_B	Input Bias Current	V_{IN} = 0V BW pin: No Connect BW pin: Connected to V_{EE} pin	 ±1.0 ±3.0	 ±2.5 ±5.0	 µA (max) µA (max)
Z_{IN}	Input Impedance	R_L = 100Ω BW pin: No Connect BW pin: Connected to V_{EE} pin	 7.5 5.5		 MΩ MΩ
V_{OS}	Offset Voltage		±17	±60	mV (max)
V_{OS}/°C	Offset Voltage vs Temperature	40°C ≤ T_A ≤ +125°C	±100		µV/°C

(1) Typical specifications are specified at 25°C and represent the parametric norm.
(2) Tested limits are ensured to AOQL (Average Outgoing Quality Level).
(3) This is the distortion of the LME49600 operating in a closed loop configuration with an LME49710. When operating in an operational amplifier's feedback loop, the amplifier's open loop gain dominates, linearizing the system and determining the overall system distortion.

TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency vs Quiescent Current

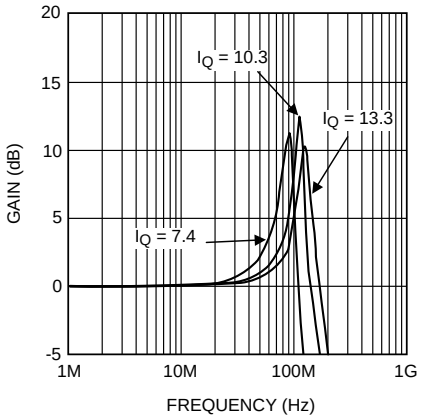


Figure 4.

Phase vs Frequency vs Quiescent Current

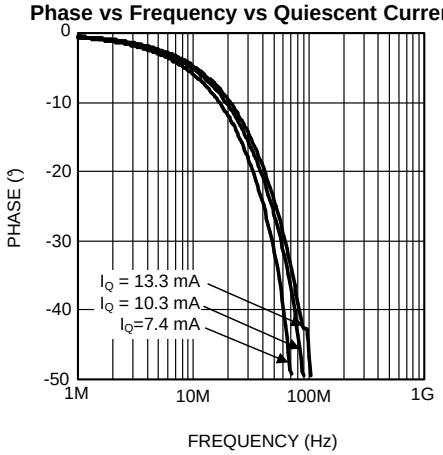


Figure 5.

Gain vs Frequency vs Power Supply Voltage Wide BW Mode

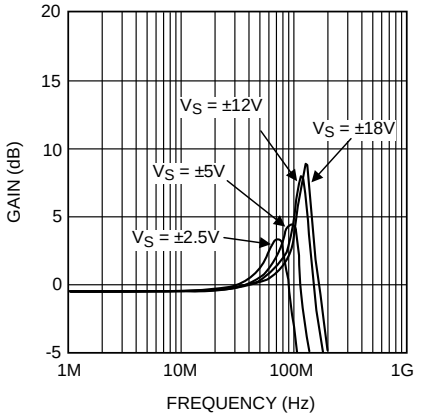


Figure 6.

Phase vs Frequency vs Supply Voltage Wide BW Mode

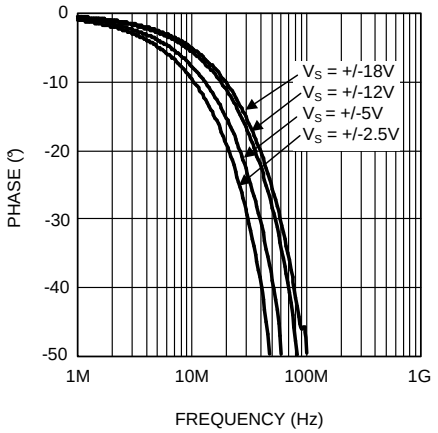


Figure 7.

Gain vs Frequency vs Power Supply Voltage Low I_Q Mode

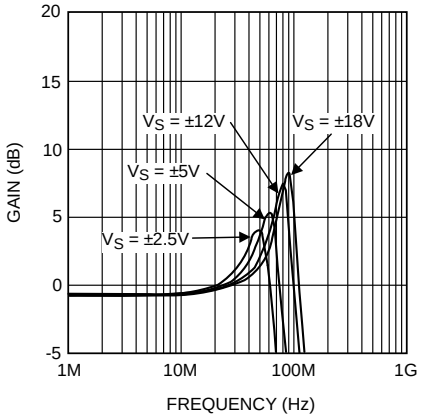


Figure 8.

Phase vs Frequency vs Supply Voltage Low I_Q Mode

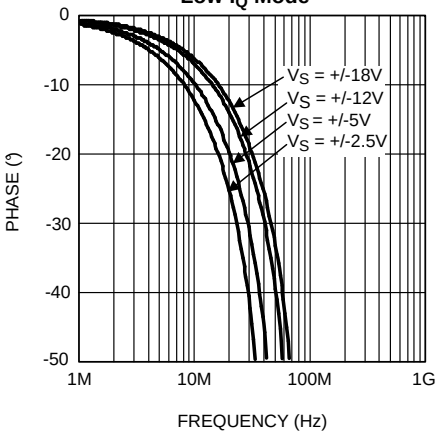


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Gain vs Frequency vs R_{LOAD} Wide BW Mode

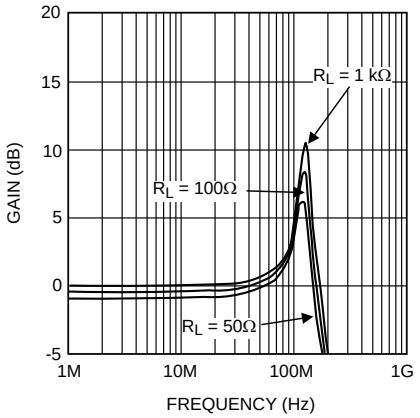


Figure 10.

Phase vs Frequency vs R_{LOAD} Wide BW Mode

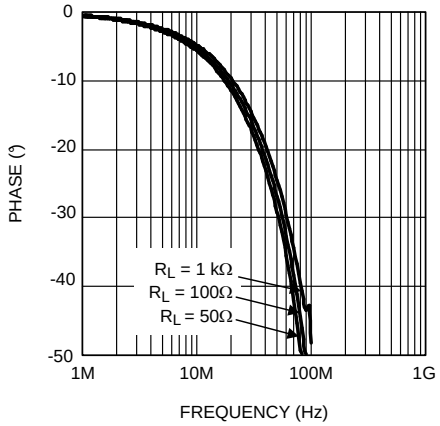


Figure 11.

Gain vs Frequency vs R_{LOAD} Low I_Q Mode

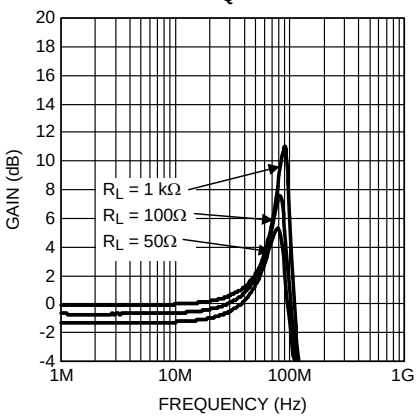


Figure 12.

Phase vs Frequency vs R_{LOAD} Low I_Q Mode

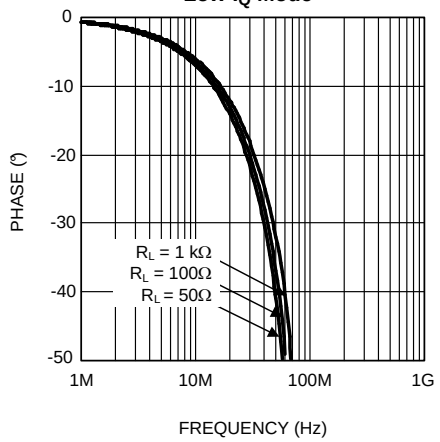


Figure 13.

Gain vs Frequency vs C_{LOAD} Wide BW Mode

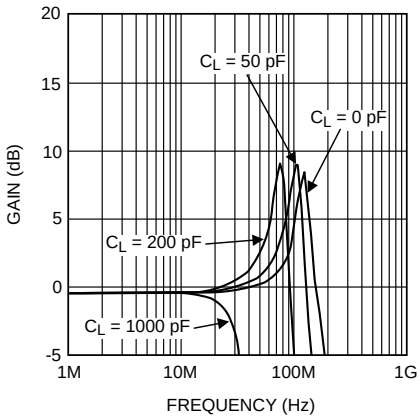


Figure 14.

Phase vs Frequency vs C_{LOAD} Wide BW Mode

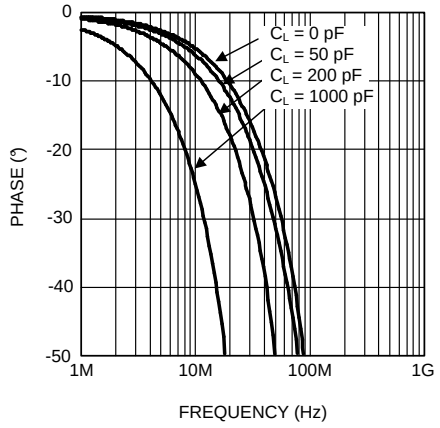


Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Gain vs Frequency vs C_{LOAD} Low I_Q Mode

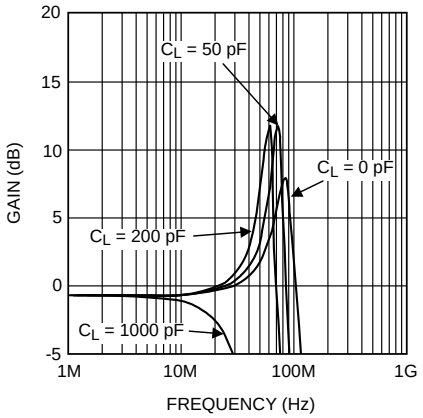


Figure 16.

Phase vs Frequency vs C_{LOAD} Low I_Q Mode

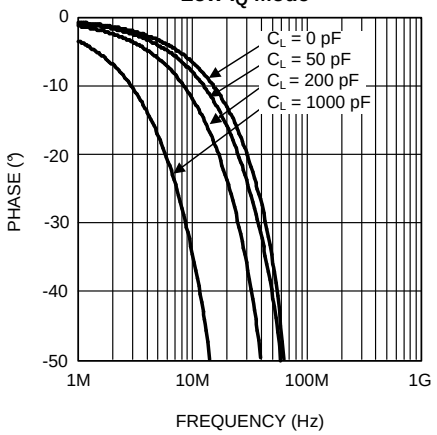


Figure 17.

+PSRR vs Frequency V_S = ±15V, Wide BW Mode

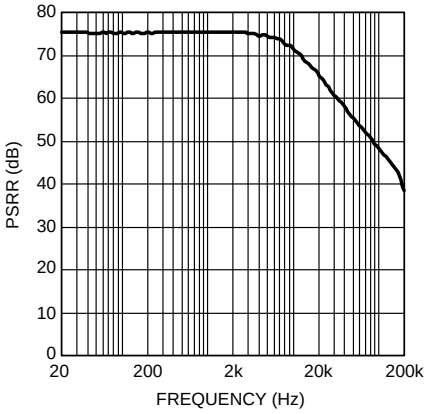


Figure 18.

+PSRR vs Frequency V_S = ±15V, Low I_Q Mode

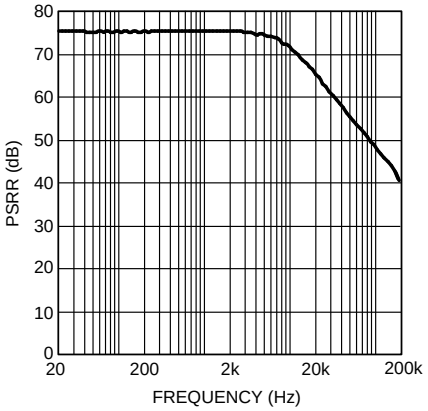


Figure 19.

+PSRR vs Frequency V_S = ±15V, Wide BW Mode

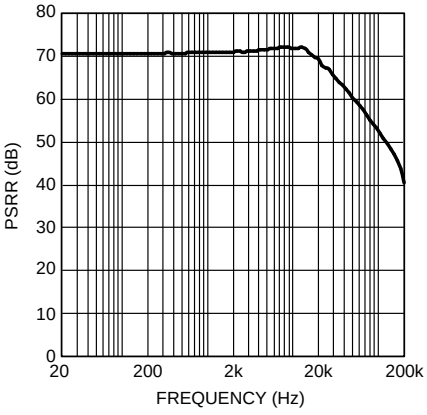


Figure 20.

+PSRR vs Frequency V_S = ±15V, Low I_Q Mode

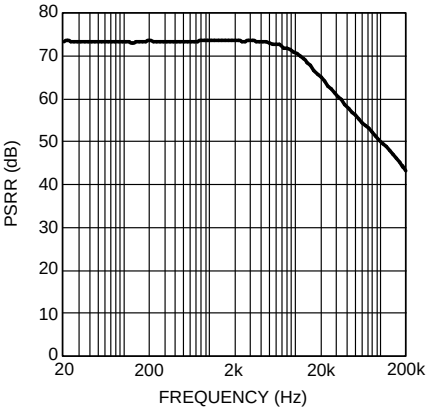


Figure 21.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Quiescent Current vs Bandwidth Control Resistance

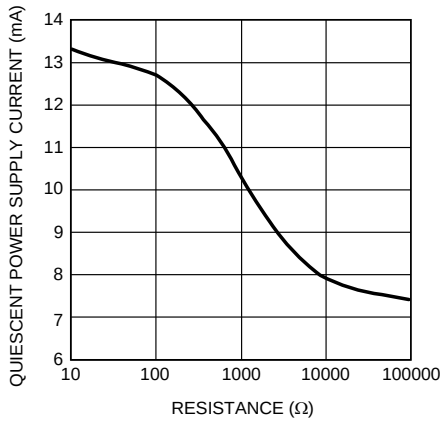


Figure 22.

THD+N vs Output Voltage
V_S = ±15V, R_L = 32Ω, f = 1kHz
Both channels driven

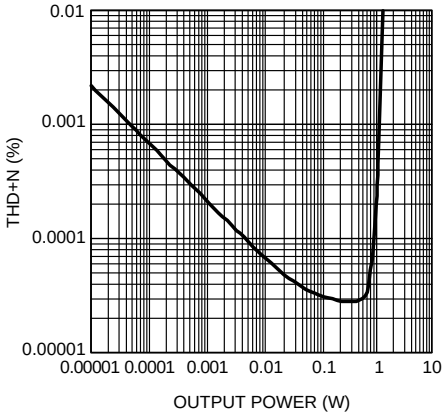


Figure 23.

High BW Noise Curve

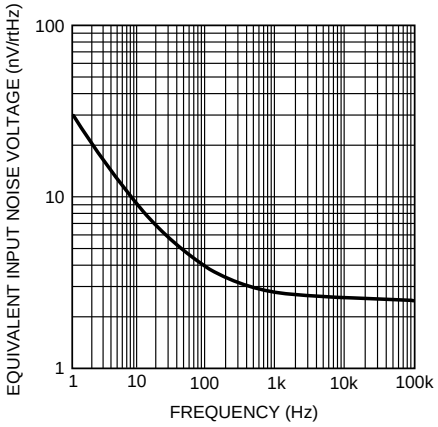


Figure 24.

Low BW Noise Curve

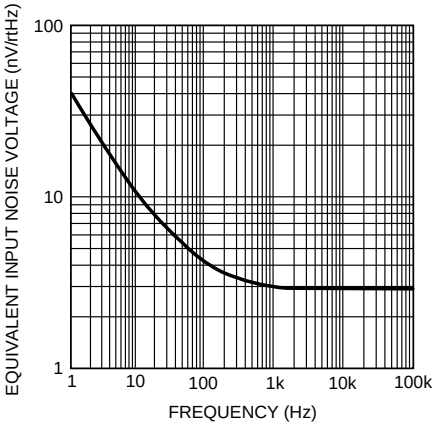


Figure 25.

TYPICAL APPLICATION DIAGRAM

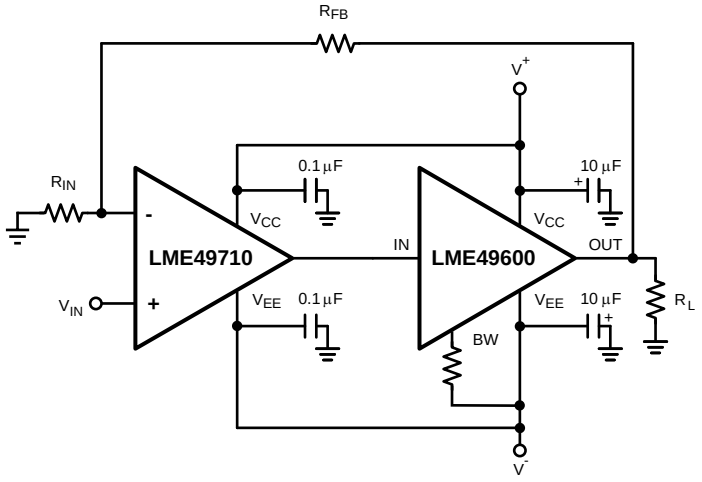


Figure 26. High Performance, High Fidelity LME49600 Audio Buffer Application

DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49710/LME49600 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49710/LME49600's low residual distortion is an input referred internal error. As shown in Figure 27, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 27.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This data sheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

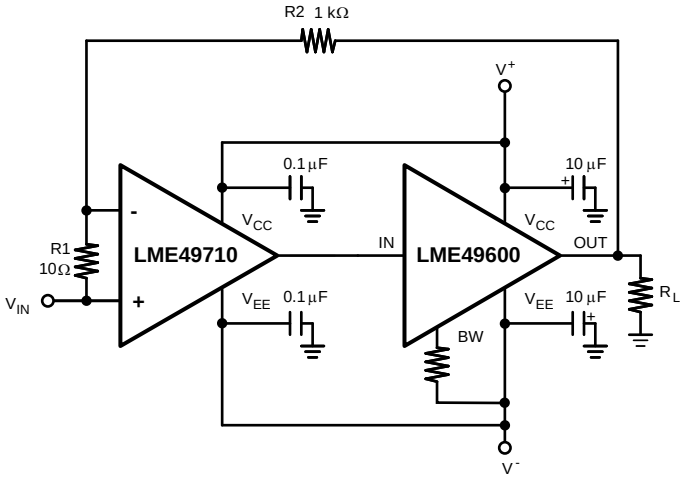


Figure 27. THD+N Distortion Test Circuit

APPLICATION INFORMATION

HIGH PERFORMANCE, HIGH FIDELITY HEADPHONE AMPLIFIER

The LME49600 is the ideal solution for high output, high performance high fidelity head phone amplifiers. When placed in the feedback loop of the LME49710, LME49720 or LME49740 High Performance, High Fidelity audio operational amplifier, the LME49600 is able to drive 32Ω headphones to a dissipation of greater than 500mW at 0.00003% THD+N while operating on ±15V power supply voltages. The circuit schematic for a typical headphone amplifier is shown in Figure 28.

Operation

The following describes the circuit operation for the headphone amplifier's Left Channel. The Right Channel operates identically.

The audio input signal is applied to the input jack (HP31 or J1/J2) and dc-coupled to the volume control, VR1. The output signal from VR1's wiper is applied to the non-inverting input of U2-A, an LME49720 High Performance, High Fidelity audio operational amplifier. U2-A's AC signal gain is set by resistors R2, R4, and R6. To allow for a DC-coupled signal path and to ensure minimal output DC voltage regardless of the closed-loop gain, the other half of the U2 is configured as a DC servo. By constantly monitoring U2-A's output, the servo creates a voltage that compensates for any DC voltage that may be present at the output. A correction voltage is generated and applied to the feedback node at U2-A, pin 2. The servo ensures that the gain at DC is unity. Based on the values shown in Figure 28, the RC combination formed by R11 and C7 sets the servo's high-pass cutoff at 0.16Hz. This is over two decades below 20Hz, minimizing both amplitude and phase perturbations in the audio frequency band's lowest frequencies.

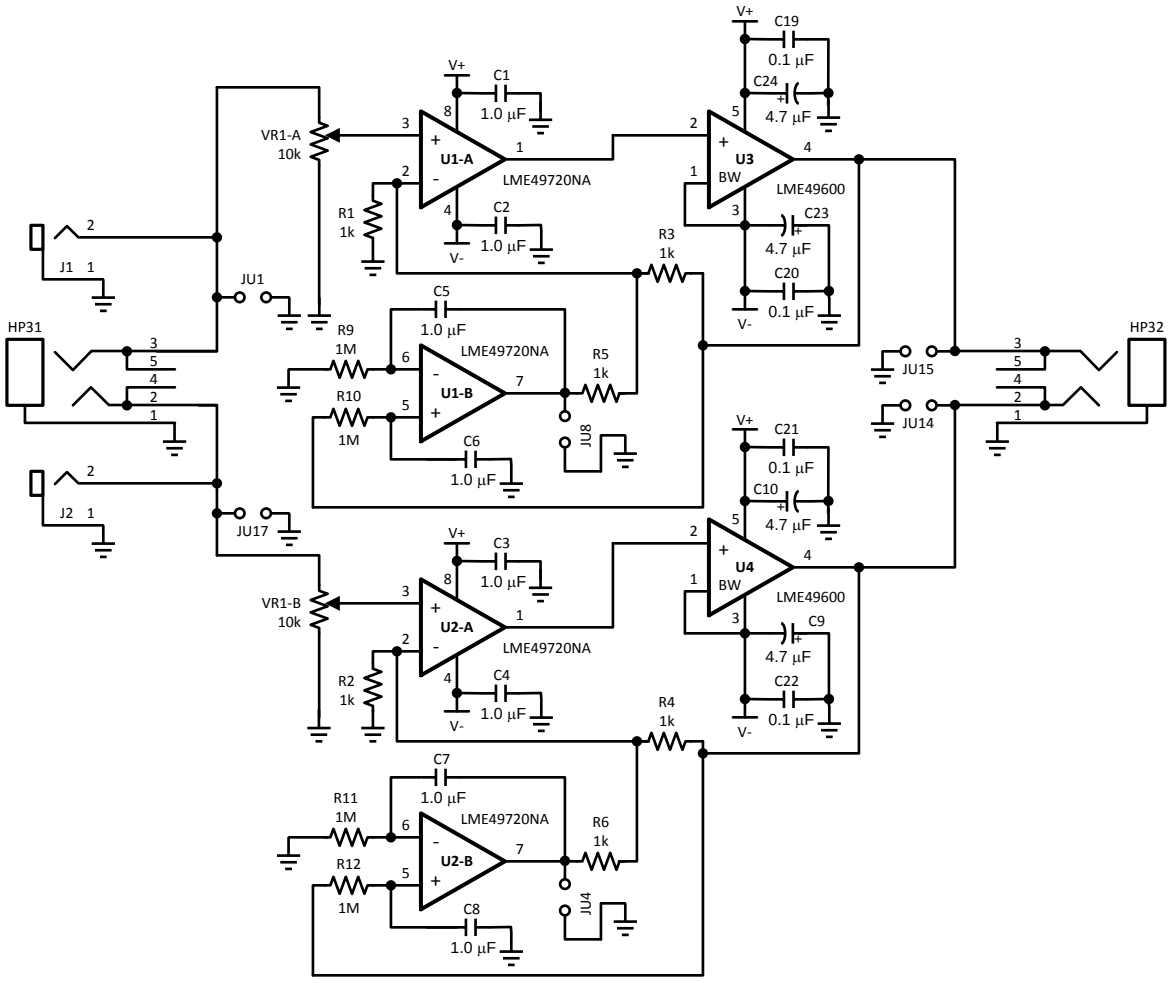


Figure 28. LME49600 Delivers High Output Current for this High Performance Headphone Amplifier

AUDIO BUFFERS

Audio buffers or unity-gain followers, have large current gain and a voltage gain of one. Audio buffers serve many applications that require high input impedance, low output impedance and high output current. They also offer constant gain over a very wide bandwidth.

Buffers serve several useful functions, either in stand-alone applications or in tandem with operational amplifiers. In stand-alone applications, their high input impedance and low output impedance isolates a high impedance source from a low impedance load.

SUPPLY BYPASSING

The LME49600 will place great demands on the power supply voltage source when operating in applications that require fast slewing and driving heavy loads. These conditions can create high amplitude transient currents. A power supply's limited bandwidth can reduce the supply's ability to supply the needed current demands during these high slew rate conditions. This inability to supply the current demand is further exacerbated by PCB trace or interconnecting wire inductance. The transient current flowing through the inductance can produce voltage transients.

For example, the LME49600's output voltage can slew at a typical ±2000V/µs. When driving a 100Ω load, the di/dt current demand is 20 A/µs. This current flowing through an inductance of 50nH (approximately 1.5" of 22 gage wire) will produce a 1V transient. In these and similar situations, place the parallel combination of a solid 5µF to 10µF tantalum capacitor and a ceramic 0.1µF capacitor as close as possible to the device supply pins.

Ceramic capacitors with values in the range of 10µF to 100µF, ceramic capacitor have very lower ESR (typically less than 10mΩ) and low ESL when compared to the same valued tantalum capacitor. The ceramic capacitors, therefore, have superior AC performance for bypassing high frequency noise.

In less demanding applications that have lighter loads or lower slew rates, the supply bypassing is not as critical. Capacitor values in the range of 0.01µF to 0.1µF are adequate.

SIMPLIFIED LME49600 CIRCUIT DIAGRAM

The LME49600's simplified circuit diagram is shown in Figure 2. The diagram shows the LME49600's complementary emitter follower design, bias circuit and bandwidth adjustment node.

Figure 29 shows the LME49600 connected as an open-loop buffer. The source impedance and optional input resistor, R_S, can alter the frequency response. As previously stated, the power supplies should be bypassed with capacitors connected close to the LME49600's power supply pins. Capacitor values as low as 0.01µF to 0.1µF will ensure stable operation in lightly loaded applications, but high output current and fast output slewing can demand large current transients from the power supplies. Place a recommended parallel combination of a solid tantalum capacitor in the 5µF to 10µF range and a ceramic 0.1µF capacitor as close as possible to the device supply pins.

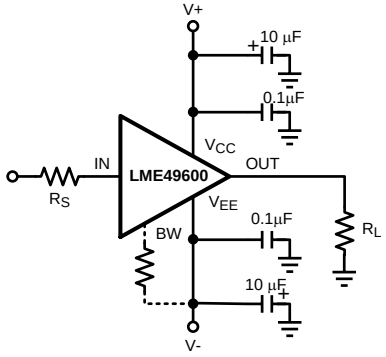


Figure 29. Buffer Connections

OUTPUT CURRENT

The LME49600 can continuously source or sink 250mA. Internal circuitry limits the short circuit output current to approximately ±450mA. For many applications that fully utilize the LME49600's current source and sink capabilities, thermal dissipation may be the factor that limits the continuous output current.

The maximum output voltage swing magnitude varies with junction temperature and output current. Using sufficient PCB copper area as a heat sink when the metal tab of the LME49600's surface mount TO–263 package is soldered directly to the circuit board reduces thermal impedance. This in turn reduces junction temperature. The PCB copper area should be in the range of $3in^2$ ($12.9cm^2$) to $6in^2$ ($38.7cm^2$).

THERMAL PROTECTION

LME49600 power dissipated will cause the buffer's junction temperature to rise. A thermal protection circuit in the LME49600 will disable the output when the junction temperature exceeds 150°C. When the thermal protection is activated, the output stage is disabled, allowing the device to cool. The output circuitry is enabled when the junction temperature drops below 150°C.

The TO–263 package has excellent thermal characteristics. To minimize thermal impedance, its exposed die attach paddle should be soldered to a circuit board copper area for good heat dissipation. Figure 30 shows typical thermal resistance from junction to ambient as a function of the copper area. The TO–263's exposed die attach paddle is electrically connected to the V_{EE} power supply pin.

LOAD IMPEDANCE

The LME49600 is stable under any capacitive load when driven by a source that has an impedance of 50Ω or less. When driving capacitive loads, any overshoot that is present on the output signal can be reduced by shunting the load capacitance with a resistor.

OVERVOLTAGE PROTECTION

If the input-to-output differential voltage exceeds the LME49600's Absolute Maximum Rating of 3V, the internal diode clamps shown in Figure 2 and conduct, diverting current around the compound emitter followers of Q1/Q5 (D1 – D7 for positive input), or around Q2/Q6 (D8 – D14 for negative inputs). Without this clamp, the input transistors Q1/Q2 and Q5/Q6 will zener and damage the buffer.

To ensure that the current flow through the diodes is held to a save level, the internal 200Ω resistor in series with the input limits the current through these clamps. If the additional current that flows during this situation can damage the source that drives the LME49600's input, add an external resistor in series with the input (see Figure 29).

BANDWITH CONTROL PIN

The LME49600's –3dB bandwidth is approximately 110MHz in the low quiescent-current mode (7.3mA typical). Select this mode by leaving the BW pin unconnected.

Connect the BW pin to the V_{EE} pin to extend the LME49600's bandwidth to a nominal value of 180MHz. In this mode, the quiescent current increases to approximately 13.2mA. Bandwidths between these two limits are easily selected by connecting a series resistor between the BW pin and V_{EE} .

Regardless of the connection to the LME49600's BW pin, the rated output current and slew rate remain constant. With the power supply voltage held constant, the wide-bandwidth mode's increased quiescent current causes a corresponding increase in quiescent power dissipation. For all values of the BW pin voltage, the quiescent power dissipation is equal to the total supply voltage times the quiescent current (I_Q * (V_{CC} + |V_{EE} |)).

BOOSTING OP AMP OUTPUT CURRENT

When placed in the feedback loop, the LME49600 will increase an operational amplifier's output current. The operational amplifier's open loop gain will correct any LME49600 errors while operating inside the feedback loop.

To ensure that the operational amplifier and buffer system are closed loop stable, the phase shift must be low. For a system gain of one, the LME49600 must contribute less than 20° at the operational amplifier's unity-gain frequency. Various operating conditions may change or increase the total system phase shift. These phase shift changes may affect the operational amplifier's stability.

Unity gain stability is preserved when the LME49600 is placed in the feedback loop of most general-purpose or precision op amps. When the LME46900 is driving high value capacitive loads, the BW pin should be connected to the V_{EE} pin for wide bandwidth and stable operation. The wide bandwidth mode is also suggested for high speed or fast-settling operational amplifiers. This preserves their stability and the ability to faithfully amplify high frequency, fast-changing signals. Stability is ensured when pulsed signals exhibit no oscillations and ringing is minimized while driving the intended load and operating in the worst-case conditions that perturb the LME49600's phase response.

HIGH FREQUENCY APPLICATIONS

The LME49600's wide bandwidth and very high slew rate make it ideal for a variety of high-frequency open-loop applications such as an ADC input driver, 75Ω stepped volume attenuator driver, and other low impedance loads. Circuit board layout and bypassing techniques affect high frequency, fast signal dynamic performance when the LME49600 operates open-loop.

A ground plane type circuit board layout is best for very high frequency performance results. Bypass the power supply pins (V_{CC} and V_{EE}) with 0.1µF ceramic chip capacitors in parallel with solid tantalum 10µF capacitors placed as close as possible to the respective pins.

Source resistance can affect high-frequency peaking and step response overshoot and ringing. Depending on the signal source, source impedance and layout, best nominal response may require an additional resistance of 25Ω to 200Ω in series with the input. Response with some loads (especially capacitive) can be improved with an output series resistor in the range of 10Ω to 150Ω.

THERMAL MANAGEMENT

Heatsinking

For some applications, the LME49600 may require a heat sink. The use of a heat sink is dependent on the maximum LME49600 power dissipation and a given application's maximum ambient temperature. In the TO-263 package, heat sinking the LME49600 is easily accomplished by soldering the package's tab to a copper plane on the PCB. (Note: The tab on the LME49600's TO-263 package is electrically connected to V_{EE}.)

Through the mechanisms of convection, heat conducts from the LME49600 in all directions. A large percentage moves to the surrounding air, some is absorbed by the circuit board material and some is absorbed by the copper traces connected to the package's pins. From the PCB material and the copper, it then moves to the air. Natural convection depends on the amount of surface area that contacts the air.

If a heat conductive copper plane has perfect thermal conduction (heat spreading) through the plane's total area, the temperature rise is inversely proportional to the total exposed area. PCB copper planes are, in that sense, an aid to convection. These planes, however, are not thick enough to ensure perfect heat conduction. Therefore, eventually a point of diminishing returns is reached where increasing copper area offers no additional heat conduction to the surrounding air. This is apparent in Figure 30 as the thermal resistance reaches an asymptote above a copper area of $8in^2$). As can be seen, increasing the copper area produces decreasing improvements in thermal resistance. This occurs, roughly, at $4in^2$ of 1 oz copper board. Some improvement continues until about $16in^2$. Boards using 2 oz copper boards will have decrease thermal resistance providing a better heat sink compared to 1 oz. copper. Beyond 1oz or 2oz copper plane areas, external heat sinks are required. Ultimately, the 1oz copper area attains a nominal value of 20°C/W junction to ambient thermal resistance (θ_{JA}) under zero air flow.

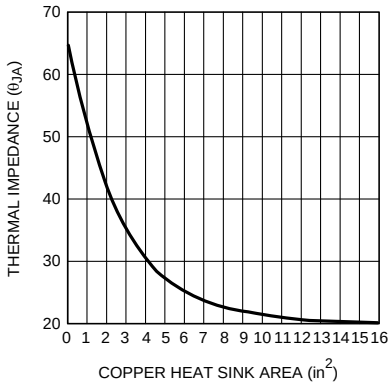


Figure 30. Thermal Resistance for 5-lead TO–263 Package Mounted on 1oz. Copper

A copper plane may be placed directly beneath the tab. Additionally, a matching plane can be placed on the opposite side. If a plane is placed on the side opposite of the LME49600, connect it to the plane to which the buffer's metal tab is soldered with a matrix of thermal vias per JEDEC Standard JESD51-5.

Determining Copper Area

Find the required copper heat sink area using the following guidelines:

1. Determine the value of the circuit's power dissipation, P_D.

2. Specify a maximum operating ambient temperature, $T_{A(MAX)}$. (Note that the die temperature, T_J, will be higher than T_A by an amount that is dependent on the thermal resistance from junction to ambient, θ_{JA}). Therefore, T_A must be specified such that T_J does not exceed the absolute maximum die temperature of 150°C.

3. Specify a maximum allowable junction temperature, $T_{J(MAX)}$, This is the LME49600's die temperature when the buffer is drawing maximum current (quiescent and load). It is prudent to design for a maximum continuous junction temperature of 100°C to 130°C. Ensure, however, that the junction temperature never exceeds the 150°C absolute maximum rating for the part.

4. Calculate the value of junction to ambient thermal resistance, θ_{JA}

5. θ_{JA} as a function of copper area in square inches is shown in Figure 30. Choose a copper area that will ensure the specified $T_{J(MAX)}$ for the calculated θ_{JA}. The maximum value of junction to ambient thermal resistance, θ_{JA}, is defined as:

$$\theta_{JA} = (T_{J(MAX)} - T_{A(MAX)}) / P_{D(MAX)} \quad (°C/W)$$

where

- $T_{J(MAX)}$ = the maximum recommended junction temperature
- $T_{A(MAX)}$ = the maximum ambient temperature in the LME49600's environment
- $P_{D(MAX)}$ = the maximum recommended power dissipation (1)

NOTE

The allowable thermal resistance is determined by the maximum allowable temperature increase:

$T_{RISE} = T_{J(MAX)} - T_{A(MAX)}$

Thus, if ambient temperature extremes force T_{RISE} to exceed the design maximum, the part must be de-rated by either decreasing P_D to a safe level, reducing θ_{JA} further or, if available, using a larger copper area.

Procedure

1. First determine the maximum power dissipated by the LME49600, $P_{D(MAX)}$. For the simple case of the buffer driving a resistive load, and assuming equal supplies, $P_{D(MAX)}$ is given by:

$$P_{DMAX(AC)} = (I_S \times V_S) + (V_S)^2 / (2\pi^2 R_L) \text{ (Watts)} \quad (2)$$

$P_{DMAX(DC)} = (I_S \times V_S) + (V_S)^2 / R_L$ (Watts)

where

- $V_S = |V_{EE}| + V_{CC}$ (V)
- I_S =quiescent supply current (A) (3)

Equation (2) is for sinusoidal output voltages and Equation (3) is for DC output voltages.

2. Determine the maximum allowable die temperature rise,

$T_{RISE(MAX)} = T_{J(MAX)} - T_{A(MAX)}$ (°C) (4)

3. Using the calculated value of $T_{RISE(MAX)}$ and $P_{D(MAX)}$, find the required value of junction to ambient thermal resistance combining Equation (1) and Equation (5) to derive Equation (9):

$\theta_{JA} = T_{RISE(MAX)} / P_{D(MAX)}$ (5)

4. Finally, choose the minimum value of copper area from Figure 30 based on the value for θ_{JA}.

Example

Assume the following conditions: $V_S = |V_{EE}| + V_{CC} = 30V$, $R_L = 32\Omega$, $I_S = 15mA$, sinusoidal output voltage, $T_{J(MAX)} = 125°C$, $T_{A(MAX)} = 85°C$.

Applying Equation (3):

$P_{DMAX} = (I_S \times V_S) + (V_S)^2 / 2\pi^2 R_L$
$= (15mA)(30V) + 900V^2 / 142\Omega$
$= 1.86W$ (6)

Applying Equation (5):

$T_{RISE(MAX)} = 125°C – 85°C$
$= 40°C$ (7)

Applying Equation (9):

$\theta_{JA} = 40°C/1.86W$
$= 21.5°C/W$ (8)

Examining the Copper Area vs. θ_{JA} plot indicates that a thermal resistance of 50°C/W is possible with a $12in^2$ plane of one layer of 1oz copper. Other solutions include using two layers of 1oz copper or the use of 2oz copper. Higher dissipation may require forced air flow. As a safety margin, an extra 15% heat sinking capability is recommended.

When amplifying AC signals, wave shapes and the nature of the load (reactive, non-reactive) also influence dissipation. Peak dissipation can be several times the average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

The LME49600's dissipation in DC circuit applications is easily computed using Equation (4). After the value of dissipation is determined, the heat sink copper area calculation is the same as for AC signals.

SLEW RATE

A buffer's voltage slew rate is its output signal's rate of change with respect to an input signal's step changes. For resistive loads, slew rate is limited by internal circuit capacitance and operating current (in general, the higher the operating current for a given internal capacitance, the faster the slew rate).

However, when driving capacitive loads, the slew rate may be limited by the available peak output current according to the following expression.

$dv/dt = I_{PK} / C_L$ (9)

Output voltages with high slew rates will require large output load currents. For example if the part is required to slew at 1000V/µs with a load capacitance of 1nF, the current demanded from the LME49600 is 1A. Therefore, fast slew rate is incompatible with a capacitive load of this value. Also, if C_L is in parallel with the load, the peak current available to the load decreases as C_L increases.

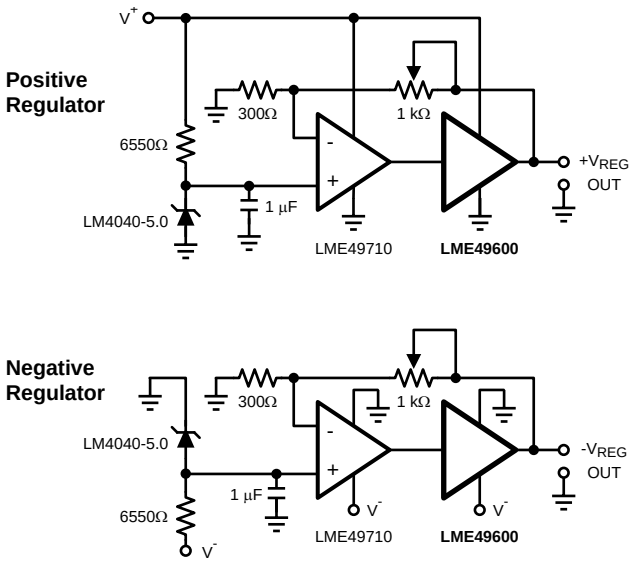


Figure 31. High Speed Positive and Negative Regulator

REVISION HISTORY

Rev	Date	Description
1.0	01/15/08	Initial release.
1.01	01/16/08	Edited specification table.
1.02	02/07/08	Edited applications information.
1.03	03/28/08	Text edits.
E	04/04/13	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49600TS/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 85	LME49600 TS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

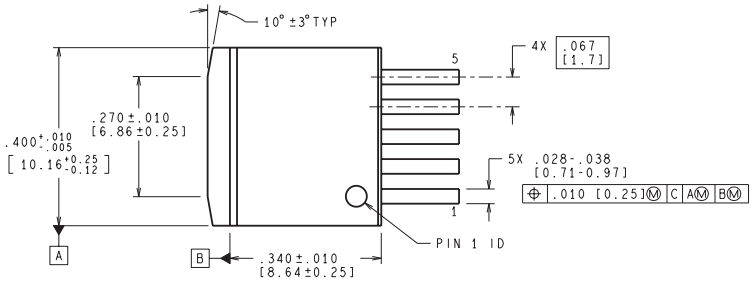
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

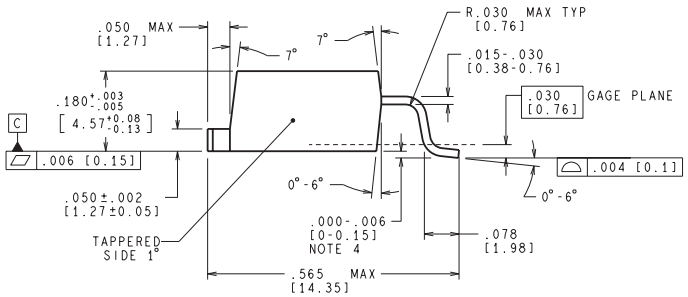
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

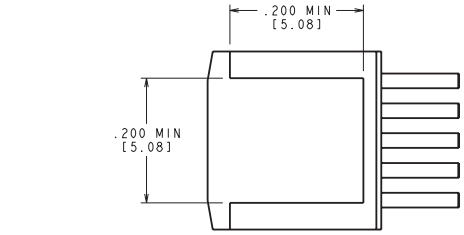
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

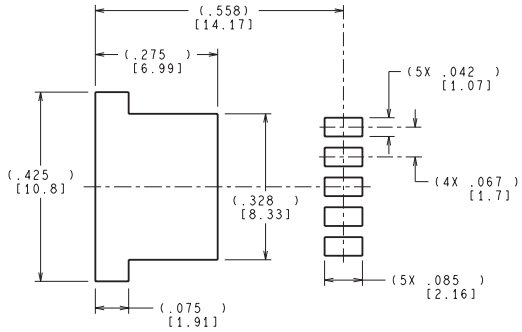
KTT0005B







BOTTOM SIDE OF PACKAGE



LAND PATTERN RECOMMENDATION

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

TS5B (Rev D)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265