# Application Note AN-1155

## Linear Mode Operation of Radiation Hardened MOSFETS

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## I. INTRODUCTION

INTERNATIONAL Rectifier would like to present this document to explain our approach to the linear mode operation of our high reliability (hi-rel) MOSFETS. We will review the definition of this mode of operation and its associated problems. The problems unique to this mode of operation have been widely discussed in the literature for over a decade, and this document will cover areas of interest to our particular products. These areas include

--First, the problems that are particular to the designers of MOSFET circuits that implement linear mode operation.

--Second, a description of the gain of our hi-rel MOSFETS and representative zero temperature gate threshold crossovers.

--Third, a brief history of the proposed solutions by various sources.

--Fourth, our proposed solution method involving new curves of safe operating area based on test results.

## II. A REVIEW OF THE LINEAR MODE OF OPERATION AND ITS PROBLEMS

### *A. Definition of the Linear Mode*

The linear mode of MOSFET operation is not to be confused with the linear region, where the MOSFET drain current is a linear function of the drain voltage. Linear mode of operation is defined as operation of the MOSFET where small changes of Vgs results in linear changes of the drain to source current.

In the non-saturated region of MOSFET operation the drain current is defined by [1] as

$$I_D = \frac{\beta}{2}\left[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2\right] \quad (1)$$

where β is termed the device transconductance parameter such that

$$\beta = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[{}^{A}/_{V^2}\right] \quad (2)$$

In saturation, the drain current is described by the equation

$$I_D = \frac{\beta}{2}(V_{GS} - V_{T0})^2 \quad (3)$$

### *B. The Problem*

Operation of the MOSFET in linear mode can create what has been called “thermal current focusing” [1], “electro-thermal instability” [3], “thermal runaway”, and has been labeled by various similar terms, but all refer to the same basic problem. Any MOSFET is susceptible to this failure mode, and this has been very well described in [1]-[4]. To summarize the problem for discussion in this work, the failure mode can be described qualitatively by examining the drain current (Id) versus gate to source voltage (Vgs) graphs for any given MOSFET.

Figure II-1 shows the transfer curve of the IR1405, an IR part from commercial MOSFET trench technology product line. In all graphs of this type that are discussed in this paper, it is important to note the cross-over point where the gain of the device is equal regardless of the MOSFET temperature. This is called the gain zero temperature crossover point, which is approximately 5.8V in this example. At values of Vgs above this point, the gain of the device is less at higher temperature. Cells of the MOSFET structure that are hotter will channel less current than the surrounding, cooler cells. The local hot spot can initially be caused by any number of non-idealities such as small local solder voids under the packaged parts or small nonuniformities in the silicon structure. This is an example of a positive temperature coefficient for Rds(on), which allows the hotter cells to reduce their drain current and on-state conduction losses such that they can cool off. Below this zero temperature crossover point, any increase in cell temperature results in more drain current, which allows the cell to pull in current from its neighbors. Having more current conducted through the cell makes its temperature rise due to on-state losses, so the gain will then increase further, until the device temperature maximum is reached and the part fails in a spectacular manner at the hot spot.

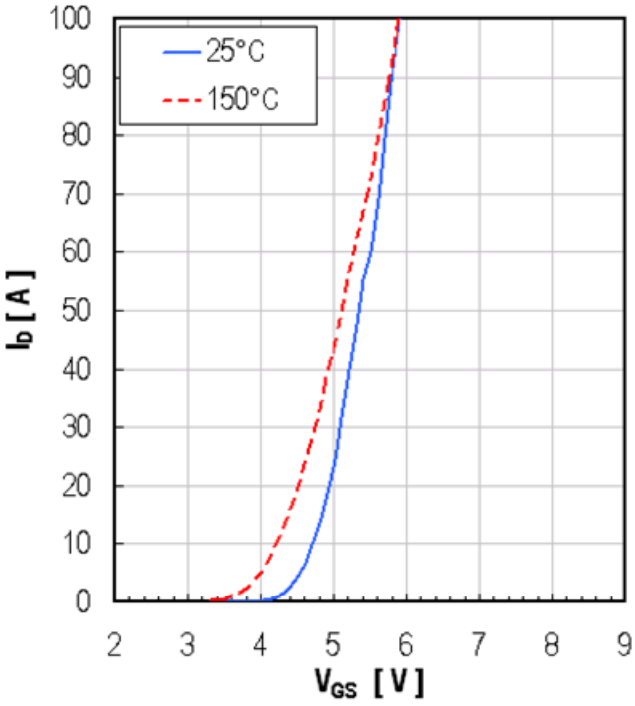


Figure II-1: Transfer Curve for IRF1405. This figure shows the relationship between the applied gate voltage and the resulting drain current through the transconductance gain of the device. The trouble with linear mode operation begins when the designer operates in the region below the zero temperature crossover (defined as the point where the device's gain is the same for all temperatures). In this case that is approximately 5.8V from gate to source.

An example of a part failure in linear mode is shown in Figure II-2 and Figure II-3. This is a MOSFET from the commercial product line of IR (to date, we have not confirmed any cases of hi-rel MOSFET failure due to linear mode operation in any of our customers' production hardware). This part failed at a Vds of 16V and an Ids of 4.2A.

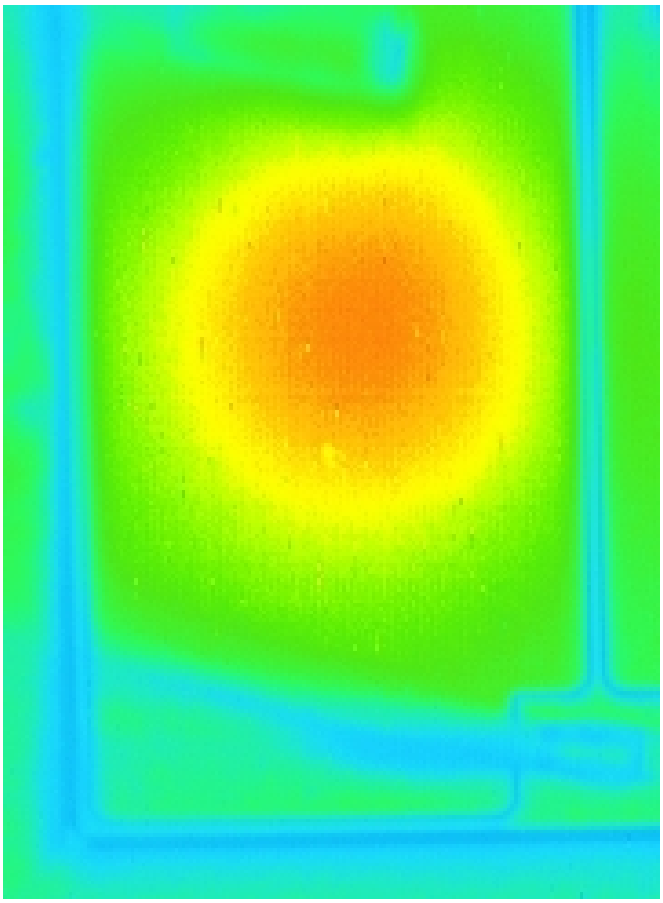

Figure II-2: Thermal image of a failure of an IRF1405Z. The picture shows the hotspot that develops when the problem of linear mode operation manifests itself. The die temperature is not uniform and a severe gradient forms where the gain of the local MOSFET cells have started to draw in the current from neighboring cells.

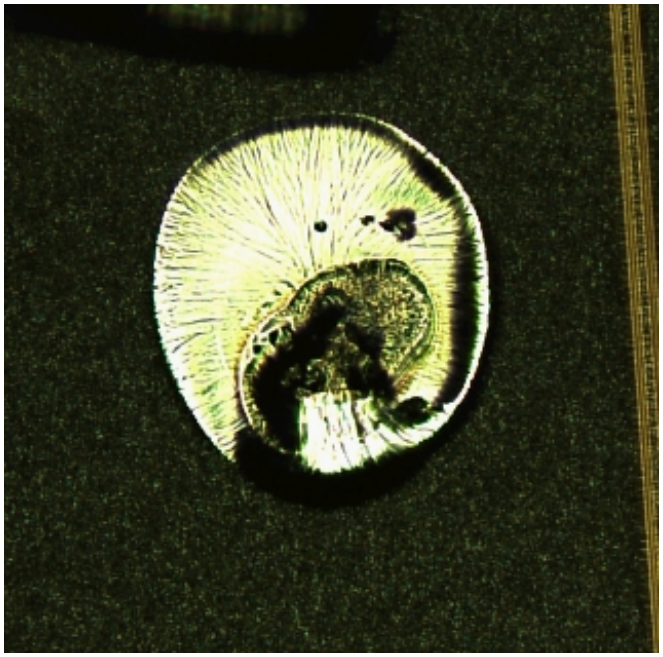

Figure II-3: Visual Image of the IRF1405Z failure. This type of visual pattern is more attractive when observed on the surface of the moon, instead of on the surface of parts that are trying to land there.

PSPICE models that are available from IR (& that can be obtained by browsing to http://www.irf.com/product-info/models/) do not predict this failure as they assume a uniform die temperature to simulate MOSFET behavior.

## III. Evolution of Device Gain and the Zero Temperature Crossover Point

The IR radiation hardened MOSFETs were optimized to be used in switching applications, not linear applications. In switching power devices, it is desired to improve the device gain as new technology is introduced. Older devices therefore have lower gains than the new devices. Unfortunately for the designers of circuits that implemented the linear mode, that means that this problem gets worse with newer parts (and could be the reason why this has not been so much of a widespread problem in the past).

Figure III-1 through Figure III-4 show the improvement in gain of the various generations of radiation hardened (rad hard) MOSFETs offered from IR. The figures also show the zero temperature crossover point for representative parts from each generation of design. The slope of the curves show how the gain was increased for each generation, and the crossover points give some idea of the range of gate voltages which would be of concern for linear mode operation.

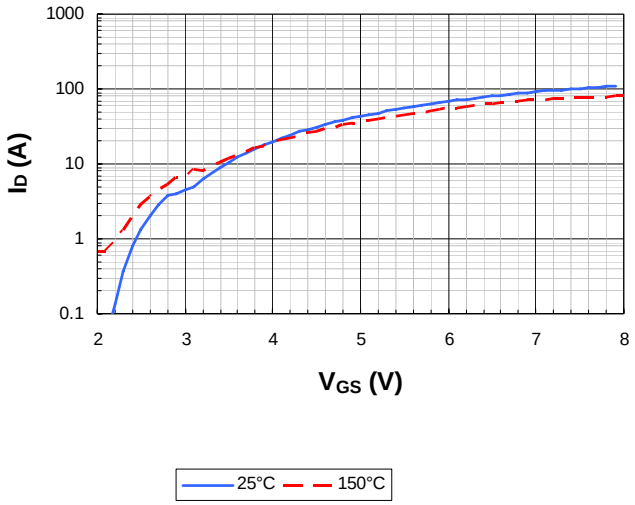


Figure III-1: Transfer Curve for IRHM9260 (Generation 4, P channel device). This figure shows the relationship between the applied gate voltage and the resulting drain current through the transconductance gain of the device. The trouble with linear mode operation begins when the designer operates in the region below the zero temperature crossover (defined as the point where the device's gain is the same for all temperatures). In this case that is approximately 3.9V from gate to source.

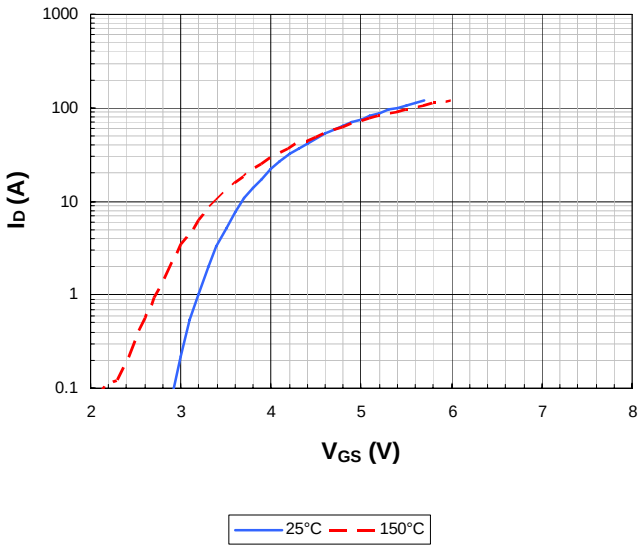


Figure III-2: Transfer Curve for IRHMS597260 (R5, P channel device). Note the increased slope of the curve versus the previous Generation 4 device, showing greater potential for instability with respect to device gain, along with a higher zero temperature crossover voltage.

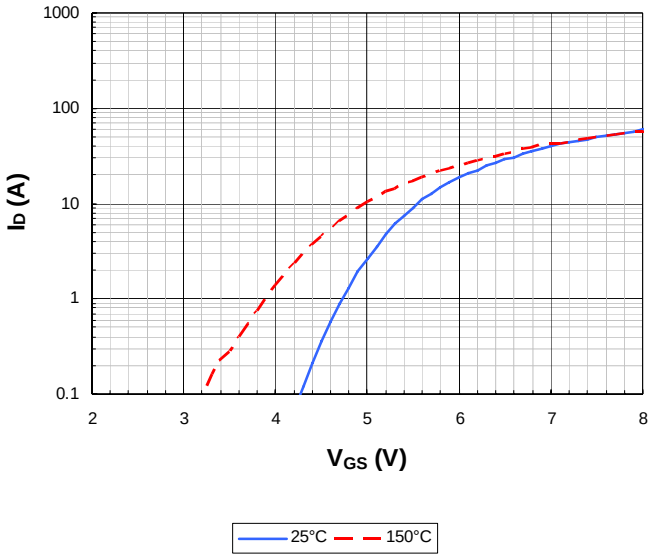


Figure III-3: Transfer Curve for IRHNJ67130 (R6). Note the significantly larger zero temperature crossover voltage as compared to previous generations. There is an increase in gain as well. However some of this is due to the inherently larger gain of N channel over P channel devices, due to the higher mobility of electrons as compared to holes.

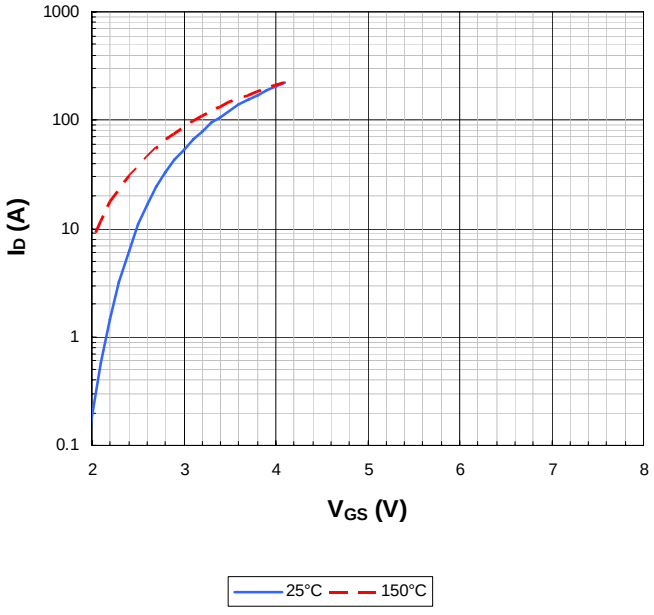


Figure III-4: Transfer Curve for IRHLNA77064 (R7). This is a logic-level-driven device, so the gain shifts even higher for this generation of devices. Note that the gain at the zero temperature crossover point is one order of magnitude higher than the Generation 4 devices.

## IV. Proposed Solutions

There have been a number of proposed solutions to this problem. The first has been shown to be fairly ineffective [5], the thermal instability method has been in use for the commercial grade of IR parts, but for our hi-rel components the best method is an SOA curve derived from test data.

### *A. Placing a Knee in the SOA Curves*

The failure of some types of MOSFETs would lend one to the conclusion that a "knee" could be artificially inserted into the SOA curve in order to prevent incorrect linear mode operation of MOSFETs, or perhaps even placing a guard banded version of an SOA line would be sufficient. Figure IV-1 shows a typical SOA curve from [5] and it can be seen why one would be tempted to modify the SOA boundaries with new lines or inserting a knee in the curve. However, the accuracy of either of these approaches would depend on the overall sample size and/or the accuracy of the data point at the extreme of Vds. Not to mention that the straight-line guard band would also cut out a large area of SOA unnecessarily, and could create false perceptions of application problems that do not exist. For certain parts where the parts fail at even lower levels of Vds than shown in Figure IV-1, the SOA curve would loss an unacceptably large percentage of its area.

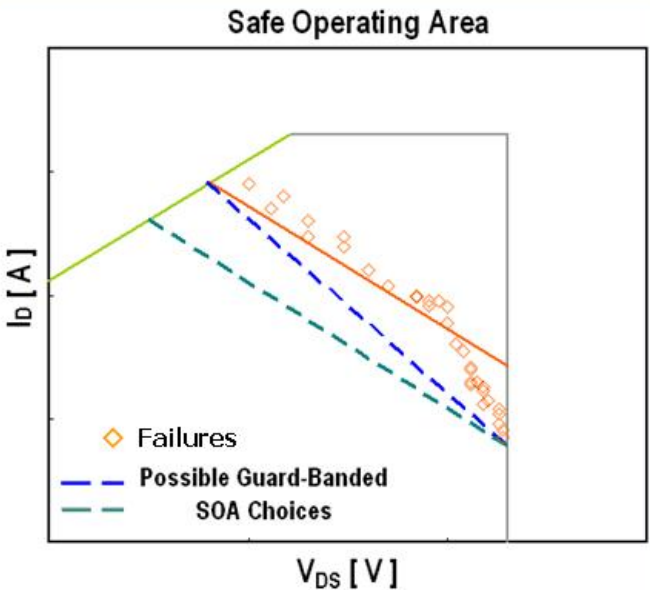


Figure IV-1: A Generic MOSFET SOA. Observed failures of the parts are plotted against the standard SOA curve. Possible guard-banded versions of the curve are also shown.

### *B. Spirito Curves*

In any device, thermal instability can occur when the electrically generated power exceeds the thermally dissipated power [6]. Spirito et al. used this as the basis for their approach [5] of an augmented safe operating area (SOA) curve. The condition of instability as defined in this approach is

$$\frac{\Delta I_D}{\Delta T} \geq \frac{1}{V_{DS} Z_\theta} \quad (4)$$

where $Z_\theta$ is the thermal impedance of the part from junction to case.

This approach, while it is useful for certain MOSFET designs, is not universally applicable. It does provide a boundary, but in the case of IR's hi-rel radiation hardened MOSFETS the device structure is such that this is not a good application. The Spirito curves would, in some cases, generate new SOA curves that are too conservative and would remove too much of the effective SOA for hi-rel applications. This would lead some of our customers to the incorrect conclusion that their circuit applications will create a failure of the part. IR has determined that a test method is best for generating SOA curves of our rad hard parts. The following section will discuss the Spirito Curves and the test-based curves with specific examples.

### *C. Testing*

The third method proposed for predicting the safe operating area of any given device, is the most basic and perhaps the most reliable one: test results. By characterizing a product family through actual testing, new curves can be generated. It has been the experience of International Rectifier Hi-Rel division that the most accurate way to characterize our parts is through individual testing instead of applying a representative curve across an entire product family.

## V. SOA Curves Based on Test Results

The method for creating new SOA curves for rad hard IR MOSFETs is based on testing actual parts. The device failure mechanism is tied to the gain of the device, which has low variability across the lots produced. Random samples of MOSFET die were chosen from a particular part deign, and the die was then assembled into a package with a lid and then tested. The parts were tested by applying specific Vds and increasing the Ids in steps until either the junction temperature reaches 150 degrees Celsius or instability is detected. As the power dissipation in the device is increased, we measure the temperature of the die and watch for signs of non-linear temperature increases. For high drain biases, this would usually happen well short of the maximum rated die temperatures for the parts. This data served as the basis for the new SOA curves.

For the first parts tested, we created a new SOA curve and plotted it with the existing SOA curves and the Spirito Curve, for the sake of comparison.

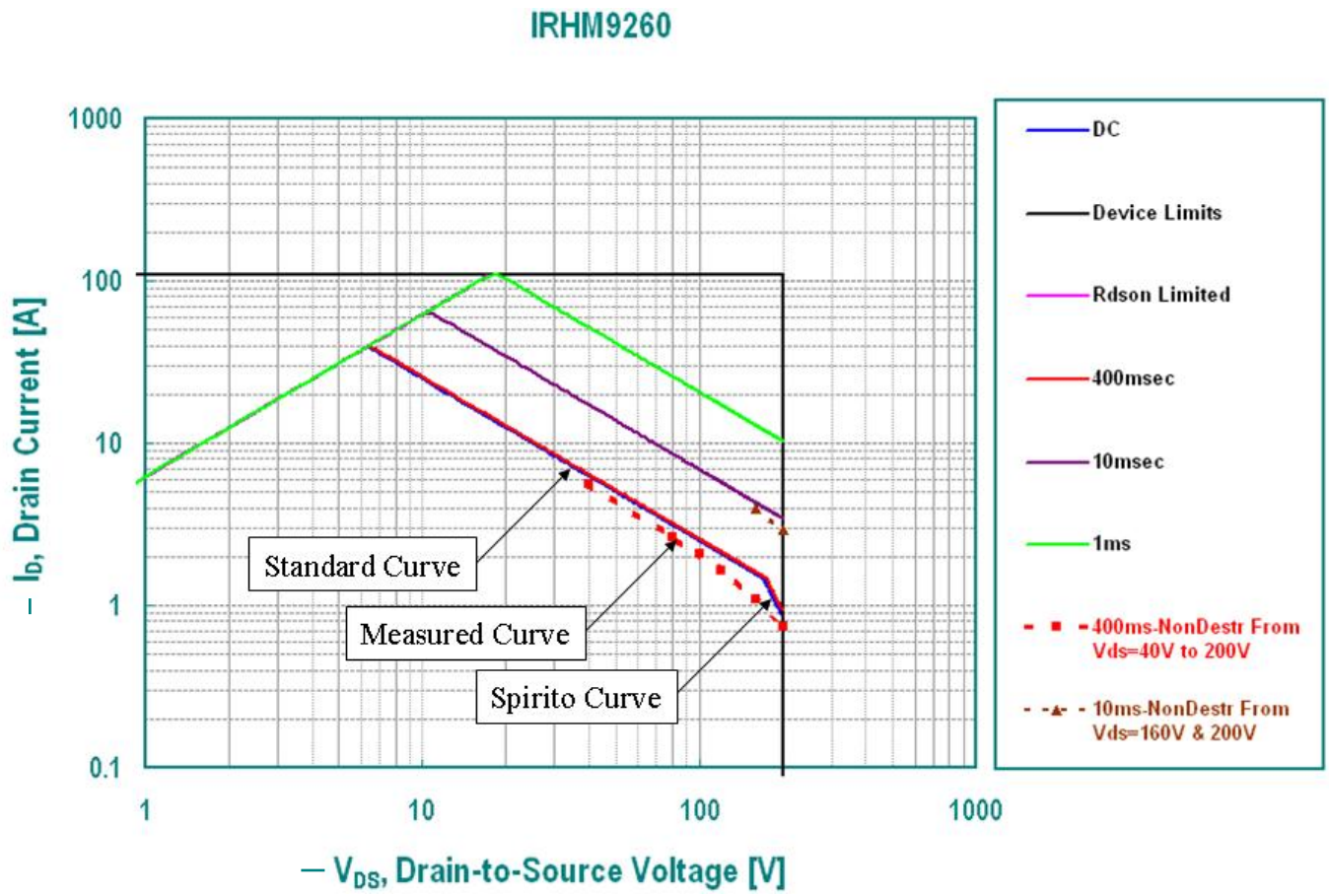


Figure V-1: IRHM9260 Preliminary SOA Curve. This shows a Gen 4 P-channel device, with the existing SOA curves for shorter pulse widths, the Spirito curve, and the measured curve derived from test results. It is important to note a few things in this figure. First, the Gen 4 device is relatively unaffected by Linear Mode operation, as noted by both the Spirito Curve and the Measured Curve. Second, the Spirito Curve in this case is not far removed from the Measured Curve. Finally, the updated SOA curve approved for use is available on the IR web site.

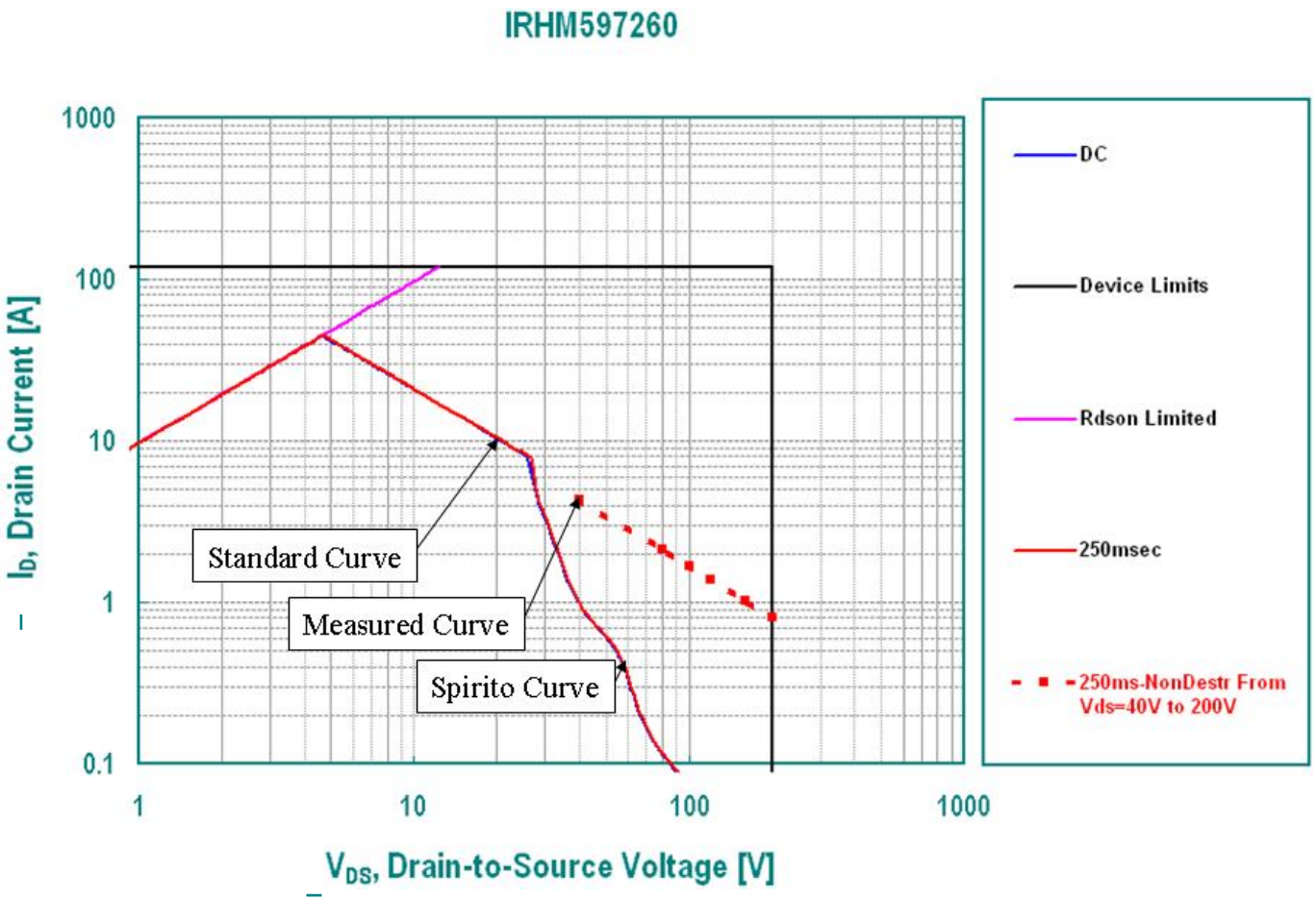


Figure V-2: IRHM597260 Preliminary SOA Curve. This shows an R5 P-channel device, with the existing SOA curves for shorter pulse widths, the Spirito curve, and the measured curve derived from test results. This figure shows how the R5 generation would seem to be more affected by the Spirito Curve. Yet the test data shows otherwise. The updated SOA curve approved for use is available on the IR web site.

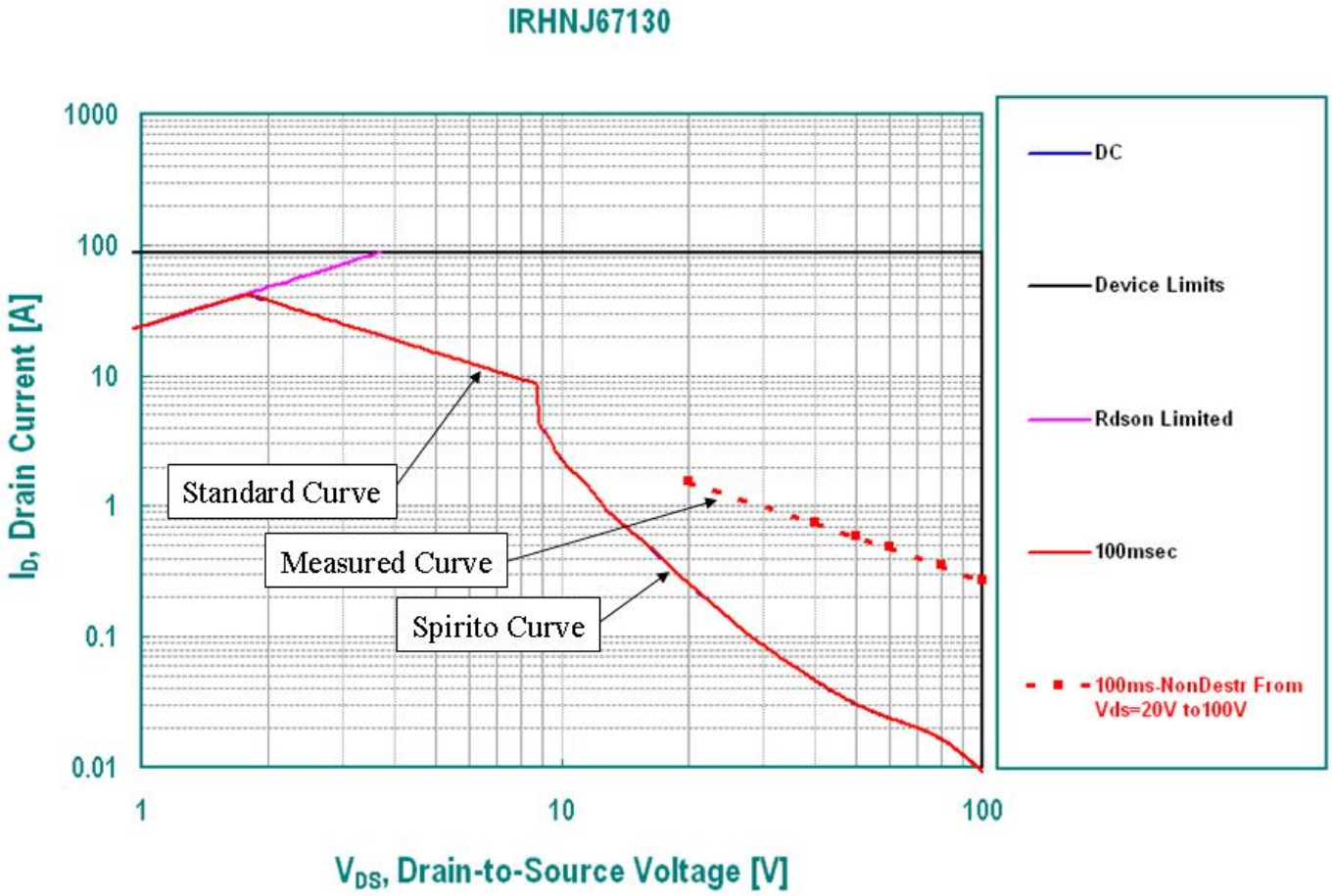


Figure V-3: IRHNJ 67130 Preliminary SOA Curve. This shows an R6 N-channel device, with the existing SOA curves for shorter pulse widths, the Spirito curve, and the measured curve derived from test results. This figure shows how the R6 generation would seem to be more affected by the Spirito Curve. Again the test data shows otherwise. The updated SOA curve approved for use is available on the IR web site.

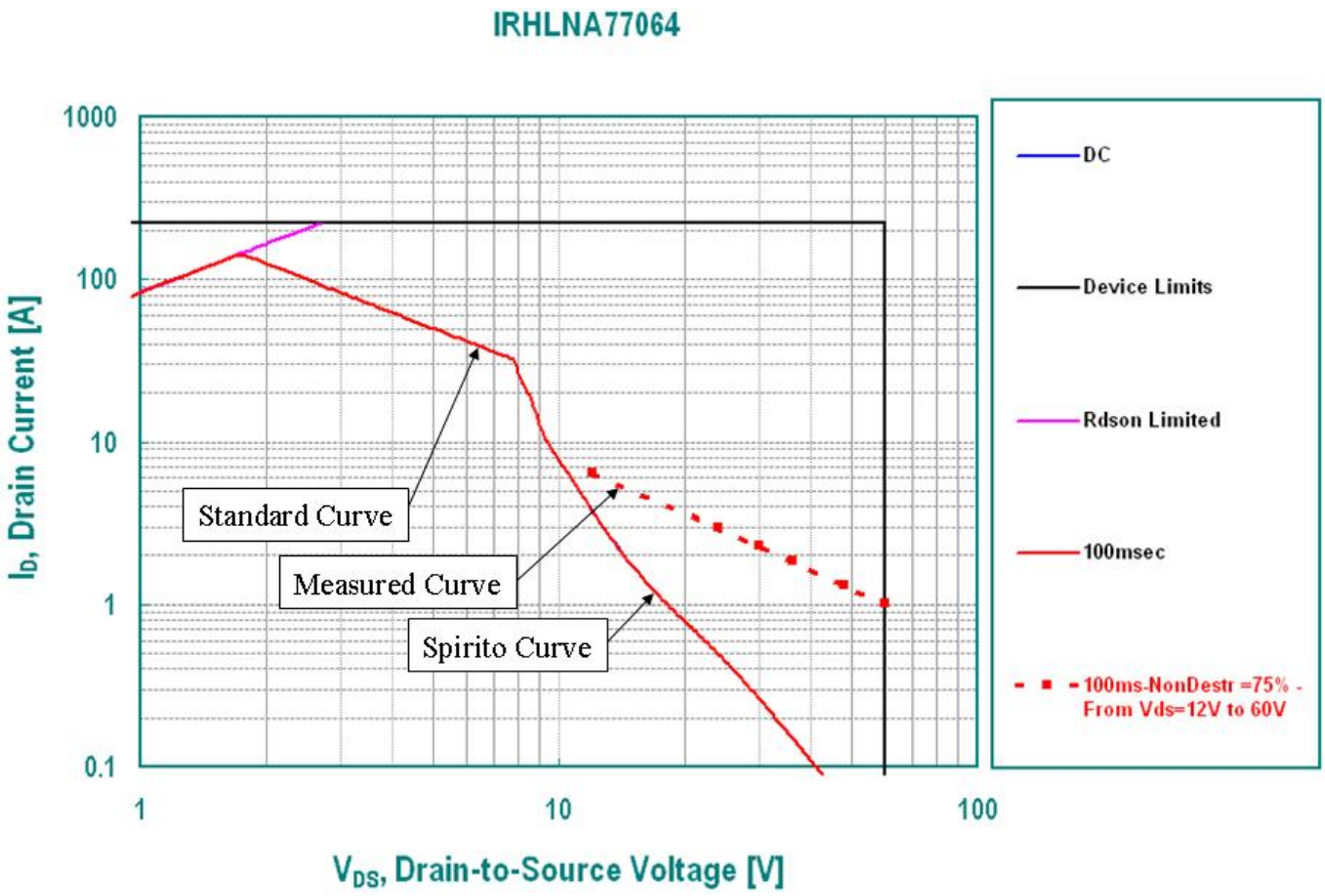


Figure V-4: IRHLNA77064 Preliminary SOA Curve. This shows an R7 N-channel device, with the existing SOA curves for shorter pulse widths, the Spirito curve, and measured curve derived from test results. This figure shows how the R7 generation would seem to be more affected by the Spirito Curve. Again the test data shows otherwise. The updated SOA curve approved for use is available on the IR web site.

## VI. Conclusion

The IR hi-rel MOSFETs, while designed for switching applications, can be used in other application if the proper SOA curves are followed. The most applicable method for creating a new SOA curve is via test characterization of the packaged part. The Spirito method, while it does yield a conservative curve of the SOA, does not accurately enough reflect the performance of IR's rad hard MOSFETs. At the time of this publication (August 2009), IR has completed new SOA curves for approximately 30% of its rad hard MOSFETs., and continues to publish new curves on the web at http://www.irf.com/product-info/hi-rel/alerts.html. The original industry alert can be found there, as well as the latest compilation of SOA curves.

## Acknowledgment

I would like to thank Milt Boden, Sandra Liu, Max Zafrani, and Lala Dhaimade (all of whom are employed by IR) for providing many answers to the questions I uncovered as this problem was being investigated, and particularly for imparting to me some of their considerable knowledge of MOSFET technology.

## References

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**Michael F. Thompson** (IEEE M'05–SM'07) became a Member (M) of IEEE in 2005, and a Senior Member (SM) in 2007. Born in Pittsburgh, PA in 1972, the author received a Bachelor of Science degree from the University of Pennsylvania in Philadelphia, PA, USA in 1994, and a Master of Science degree (with a specialty in power electronics and controls) from the State University of New York in 1998.

He has worked for Lockheed Martin and Northrop Grumman. His design experience covers AC-DC, DC-AC, DC-DC power conversion at power levels that range from milliwatts to megawatts. He is familiar with the construction and characteristics of energy storage devices and the complexities of digital controls for power systems. Low noise output ripple designs and distributed power systems are of interest to him. He is presently working for International Rectifier as the Hi-Rel Field Application Engineer for the Eastern United States and is based out of his office in Maryland.