

## Application Note 050

### Failure Mode of SCR-Output Relays vs. MOSFET-Output Relays at High Temperature

#### Introduction

High temperature is a common environmental stress in many solid state relay applications. Application engineers must have a solid understanding of how a relay can be expected to fail if the temperature exceeds the rating of the package. This paper aims to compare the theoretical and experimental failure modes of SCR-output relays vs. MOSFET-output relays at high temperature.

Let us first define failure for an SSR as a condition in which we lose control of the output. For example, if we want to turn the output off and are unable to do so, that will be considered a failure. Similarly, if we try to turn the output on and we are stuck in an open condition, that is a failure.

Solid state relays are typically rated for an operating temperature in the neighborhood of 85° C. This nominal figure depends on the maximum junction temperature of the output structure. We consider high temperature to be any temperature above 85° C.

This report is broken up into two parts: 1) theoretical discussion of SCR and MOSFET at high temperature; 2) experimental results supporting theory.

#### Theoretical Discussion

##### SCRs at High Temperature

An SCR is simply a p-n-p-n structure with a gate terminal (Fig.1). We can break the structure down as back-to-back transistors, one p-n-p, the other n-p-n. With that simplification, we can see that temperature analysis of the bipolar transistor extends logically to the SCR structure.

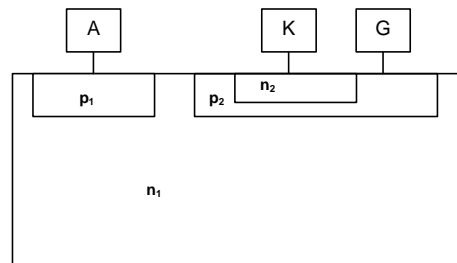
It is a well known empirical fact that leakage current approximately doubles with every 10° C increase in temperature.<sup>1</sup> In a bipolar transistor, this increase in leakage is accentuated by the "transistor action" of

the device. This can be explained by using an n-p-n transistor as an example. As we increase the temperature, more and more electrons are able to jump the barrier from the emitter to the base. This further biases the base region with respect to the emitter and collector, causing an increase in collector current. In fact, a transistor can be turned on simply by applying high temperature - sufficient leakage current can be generated to trigger the transistor action.

This discussion extends to the SCR, which is nothing more than two bipolar transistors driving each other. Any effect felt by the bipolar transistor is only magnified when discussing the SCR. The effect is not additive, it is multiplicative.

There is another temperature-related phenomenon we must point out: as we increase temperature, diode voltage decreases at an approximate rate of 2 mV/°C.<sup>2</sup> Therefore, a transistor in the on state will have a tendency to not only stay on at high temperature, but to conduct even more fully; i.e., the barrier between p- and n-type regions is reduced even more.

The result of these two phenomena is that the bipolar transistor has a negative temperature coefficient; the higher the temperature, the higher the collector current at a given base drive.



**Fig. 1: SCR structure**

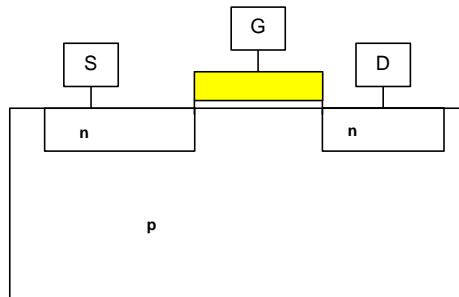
Let's now extend the discussion to the SCR, specifically in Solid State Optronics device S742. The S742 uses two SCRs in the output; thus, it can only be utilized in AC applications. This is because the only way to prevent these particular SCRs from conducting once they are turned on is to reverse the voltage across their terminals. This is dictated by the output of the application. In a DC application, once the SCR is turned on, there is no way of turning it off. Under DC, the SCR never experiences the reverse voltage condition across its terminals necessary to prevent conduction.

An SCR in the off state will tend to turn on and stay on (latch) at high temperatures. Of course, in the S742 one SCR will always be non-conducting because of the reverse voltage on the output. But the other will tend to turn on even without an input signal because of the above considerations.

### MOSFETs at High Temperature

Under no gate bias, a MOSFET can be thought of as a pair of back-to-back p-n diodes (Fig. 2), from source-to-bulk and bulk-to-drain. Again, we point to the empirical fact that leakage current approximately doubles with every 10° C increase in temperature. However, as we increase temperature, we can think of the leakage current from each diode cancelling each other out, resulting in no net change in current.

The dominant temperature-related mechanism for the MOSFET is the reduction in carrier mobility. This reduction exists because of the increase of scattering a carrier experiences due to the increased excitation



**Fig. 2: MOSFET structure**

of lattice sites in silicon at high temperature. The mobility of carriers in the channel of a MOSFET behaves according to the following empirical expression<sup>3</sup>:

$$\mu(T) = \mu(300 \text{ K}) / (T/300)^a \quad \text{where } T \text{ is measured in kelvins and } a \text{ is } 1.0-1.5$$

This relation shows that mobility may decrease as much as 40% for a 100° C temperature increase. Decreased mobility leads directly to an increase in on-resistance. Thus, we can say that the MOSFET's on-resistance has a positive temperature coefficient.

On the other hand,  $V_T$ , the threshold voltage of a MOSFET, typically decreases by approximately 1.5 mV/°C.<sup>4</sup> The reason for this effect is that at high temperature, we can expect an increase in thermally generated carriers (leakage). With more n-type carriers available in the conducting channel, we need less of a gate voltage to achieve the same amount of conduction.

This effect would tend to counter the decrease in mobility, however, the effect is relatively weak.  $V_T$  decreases by approximately 0.15 V for a 100° C increase in temperature - this is relatively insignificant. We would expect the reduction in mobility to be the dominant mechanism at high temperature.

The reduction in  $V_T$  is further offset by the reduction in the voltage of the gate driver circuit. In SSO's MOSFET-output devices, the driver consists of 14 series diodes. These diodes generate sufficient voltage to drive the gate of the output MOSFET, allowing conduction. As mentioned above in the SCR discussion, diode voltage drops at higher temperature. This in turn reduces the drive voltage to the gate of the MOSFET. Empirical results have shown that the drive voltage is reduced by approximately the same amount as the reduction in  $V_T$ , thereby virtually cancelling the effect.

Now, let's look at the potential failure modes. A MOSFET in the off state will not turn on when exposed only to high temperature. This is because high temperature alone will not be able to create the inversion layer beneath the gate necessary for conduction. A gate voltage is required to do this. Furthermore, a MOSFET in the on state will tend to conduct less and ultimately shut off at high temperatures due to the reduction in carrier mobility.

## Experimental Results

In order to provide support for the theoretical conclusions, we ran a set of experiments with an SSO SCR-output device (SSO P/N S742) and an SSO MOSFET-output device (SSO P/N AD8C111) at high temperature. Please see attached documented procedure for details. In short, the test procedure consisted of 4 parts:

1) Take 20 S742s and put in oven cycling ON/OFF (10 HZ input square wave, 100 mA load); raise temperature until device fails and note failure mode.

2) Take 20 S742s and put in oven OFF (blocking 250  $V_{RMS}$ ); raise temperature until device fails and note failure mode.

3) Take 20 AD8C111s and put in oven cycling ON/OFF (10 HZ input square wave, 100 mA load); raise temperature until device fails and note failure mode.

4) Take 20 AD8C111s and put in oven OFF (blocking 275  $V_{RMS}$ ); raise temperature until device fails and note failure mode.

The following is a summary of the results of these experiments (please see attached documentation for further detail):

1) 18 of the 20 relays failed short; 1 failed open. The final relay didn't fail up to 145° C, at which point the oven's fuse mechanism prevented a further increase in temperature.

2) 18 of the 20 relays failed short. The other 2 relays didn't fail up to 175° C, at which point the oven's fuse mechanism prevented a further increase in temperature.

3) All 20 relays failed open - 11 of the 20 were "partially" conducting; the other 9 were completely OFF. (This result clearly shows the reduction in carrier mobility).

4) 13 of the 20 relays failed open. The other 7 didn't fail up to 150° C, at which point the oven's fuse mechanism prevented a further increase in temperature.

## Conclusion

These results support theoretical expectations; namely, SCR-output devices can be expected to fail

short at high temperature, while MOSFET-output devices can be expected to fail open.

## REFERENCES

<sup>1</sup> Yang, "Fundamentals of Semiconductor Devices", P. 105

<sup>2</sup> Yang, P. 105

<sup>3</sup> Hodges/Jackson, "Analysis and Design of Digital Integrated Circuits", P. 48

<sup>4</sup> Supertex Databook 1996, P. 3-1