International
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The Do's and Don'ts of Using MOS-Gated Transistors

In this application note, some of the most common do's and don'ts of using HEXFET® power MOSFETs are described. The objective is to help the user get the most out of these remarkable devices, while reducing "on the job" learning time to a minimum.

1. Be Mindful of The Reverse Blocking Characteristics of The Device

IGBTs have a limited reverse blocking capability of approximately 20-30 V, with high leakage. This is characterized in IR's data sheets with a Reverse Avalanche Energy (EARV). This rating is useful to absorb energy spikes due to the stray inductance in series with the anti-parallel diode. This is a significant advantage over bipolar transistors and power darlingtons. A feature of power MOSFETs is that they inherently have built into them an integral reverse body-drain diode. The existence of this diode is explained by reference to Figure 1. When the source terminal is made positive with respect to the drain, current can flow through the middle of the source cell, across a forward biased P-N junction. In the "reverse" direction, the HEXFET® power MOSFET thus behaves like a P-N junction rectifier. The integral body-drain diode is a real circuit element, and its current handling capability is typically as high as that of the transistor itself. Some circuits require an "inverse" rectifier to be connected across the switching device, and in these circuits it will often be possible to utilize the body-drain diode of the HEXFET power MOSFET provided the proper precautions are taken.

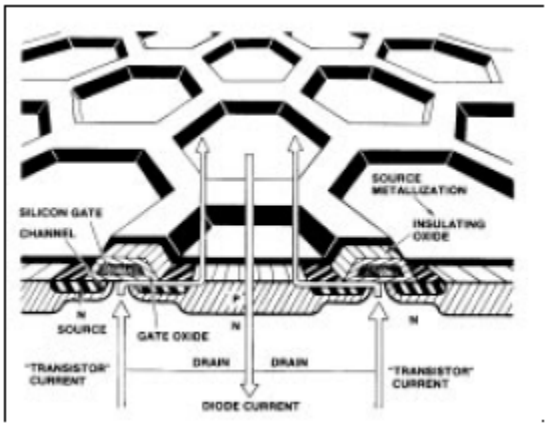

Figure 1. Basic HEXFET MOSFET Structure

2. Be Careful When Handling & Testing HEXFET® Power MOSFETs

The user's first "contact" with a MOS-gated transistor could be a package of parts arriving on his desk. Even at this stage, it behooves one to be knowledgeable about some elementary precautions. Being MOS devices, HEXFET power MOSFETs can be damaged by static charge when handling, testing or installing into a circuit. Power Devices have large input capacitance, and are able to absorb static charge without excessive buildup of voltage. In order to avoid possible problems, however, the following procedures should be followed as a matter of good practice, wherever possible:

- MOS-gated transistors should be left in their anti-static shipping bags, or conductive foam, or they should be placed in metal containers or conductive tote bins, until required for testing or connection into a circuit. The person handling the device should ideally be grounded through a suitable wrist strap, though in reality this added precaution is seldom essential.
- Devices should be handled by the package, not by the leads. When checking the electrical characteristics of the MOS-gated transistors on a curve tracer, or in a test circuit, the following precautions should be observed:
- Test stations should use electrically conductive floor and table mats that are grounded. Suitable mats are available commercially.

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- When inserting the device in a curve tracer or a test circuit, voltage should not be applied until all terminals are solidly connected into the circuit.
- When using a curve tracer, a resistor should be connected in series with the gate to damp spurious oscillations that can otherwise occur on the trace. A suitable value of resistance is 100 ohms.
- For repeated testing, it is convenient to build this resistor into the test fixture.
- When switching from one test range to another, voltage and current settings should be reduced to zero, to avoid the generation of potentially destructive voltage surges during switching.

The next step is to connect the device into an actual circuit. The following simple precautions should be observed:

- Work stations should use electrically grounded table and floor mats.
- Soldering irons *should be grounded.*

Now that the device has been connected into its circuit, it is ready for the power to be applied. From here on, success in applying the device becomes a matter of the integrity of the circuit design, and of what circuit precautions have been taken to guard against unintentional abuse of its ratings.

The following are the interrelated device and circuit considerations that lead to reliable, trouble-free design.

3. BEWARE OF UNEXPECTED GATE-TO-SOURCE VOLTAGE SPIKES

Excessive voltage will punch through the gate-source oxide layer and result in permanent damage. This seems obvious enough, but it is not so obvious that transient gate-to-source overvoltages can be generated that are quite unrelated to, and well in excess of, the amplitude of the applied drive signal. The problem is illustrated by reference to Figure 2.
If we assume that the impedance, Z, of the drive source is high, then any positive-going change of voltage applied across the drain and source terminals (caused, for example, by the switching of another device in the circuit) will be reflected as a positive-going voltage transient across the source and the drain terminals, in the approximate ratio of:

$$\frac{1}{1+\frac{C_{gs}}{C_{dg}}}$$

The above ratio is typically about 1 to 6. This means that a change of drain-to-source voltage of 300V, for example, could produce a voltage transient approaching 50V between the gate and source terminals. In practice this “aiming” voltage will not appear on the gate if the dv/dt is positive because the MOS-gated device goes in conduction at approximately Vgs = 4V, thereby clamping the dv/dt at the expense of a current transient and increased power dissipation. However, a negative-going dv/dt will not be clamped. This calculation is based upon the worst case assumption that the transient impedance of the drive circuit is high by comparison with the gate-to-source capacitance of the device. This situation can, in fact, be quite easily approximated if the gate drive circuit contains inductance—for example the leakage inductance of an isolating drive transformer. This inductance exhibits a high impedance for short transients, and effectively decouples the gate from its drive circuit for the duration of the transient.

The negative-going gate-to-source voltage transient produced under the above circumstances may exceed the gate voltage rating of the device, causing permanent damage. It is, of course, true that since the applied drain transient results in a voltage at the gate which tends to turn the device ON, the overall effect is to an extent self-limiting so far as the gate voltage transient is concerned. Whether this self-limiting action will prevent the voltage transient at the gate from exceeding the gate-source voltage rating of the device depends upon the impedance of the external circuit. Spurious turn-on is of itself undesirable, of course, though in practical terms one may grudgingly be able to accept this circuit operating imperfection, provided the safe operating area of the device is not violated.

Notice that a voltage clamp (a conventional zener diode is suitable for this purpose) to prevent the gate-source voltage rating from being exceeded will not prevent the dv/dt induced turn-on, as the gate will not reach the zener voltage. In many instances the zener is responsible for generating oscillations in the gate circuit, particularly when a significant amount of stray inductance is present. A more fundamental solution, of course, is to make the impedance of the gate circuit low enough that not only is the gate-source voltage rating not exceeded, but also the voltage transient at the gate is contained to a level at which spurious turn-on does not occur.

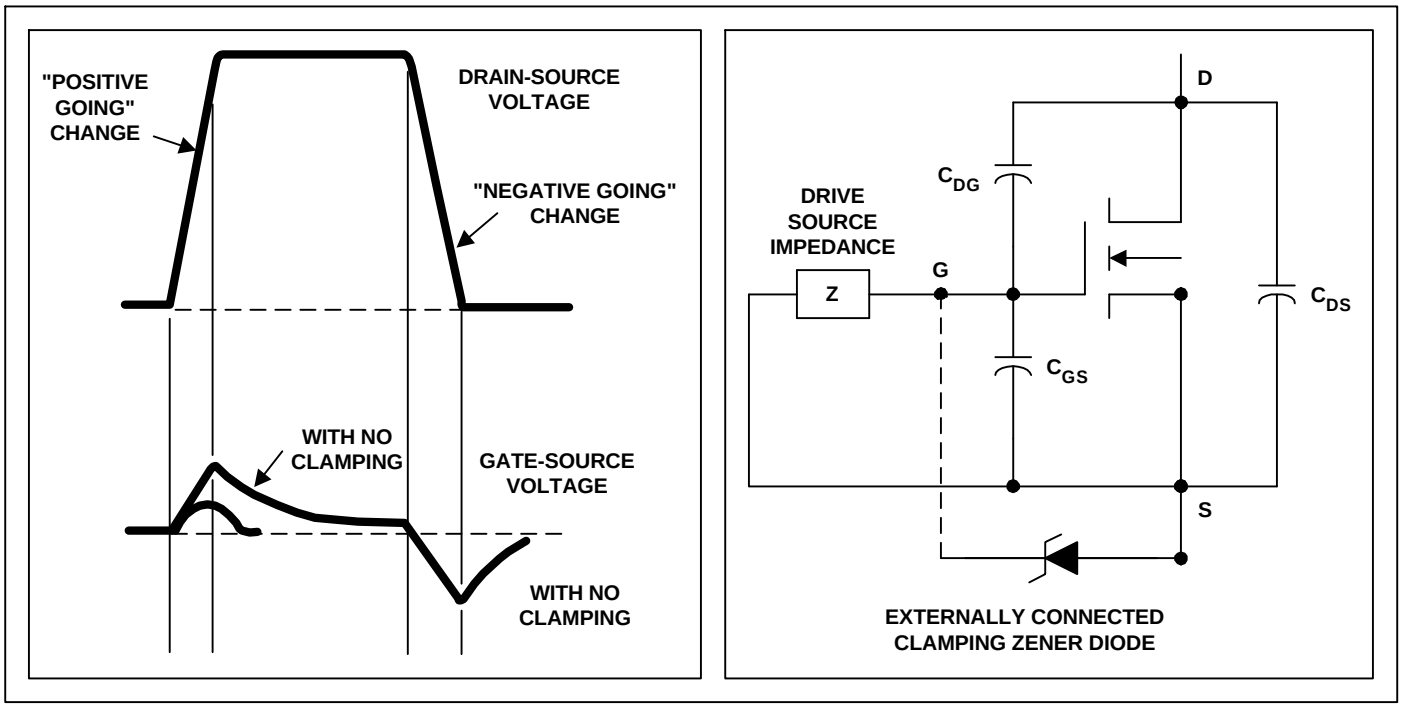

Figure 2. A Rapidly Changing Applied Drain-Source Voltage will Produce Gate-Source Transients

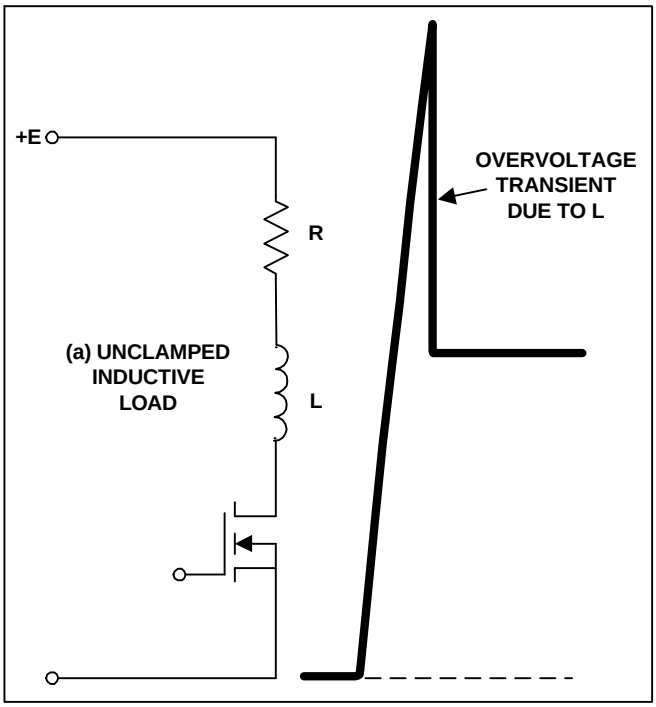

Figure 3. Drain-Source Overvoltage Transient when Switching Off with Unclamped Inductive Load

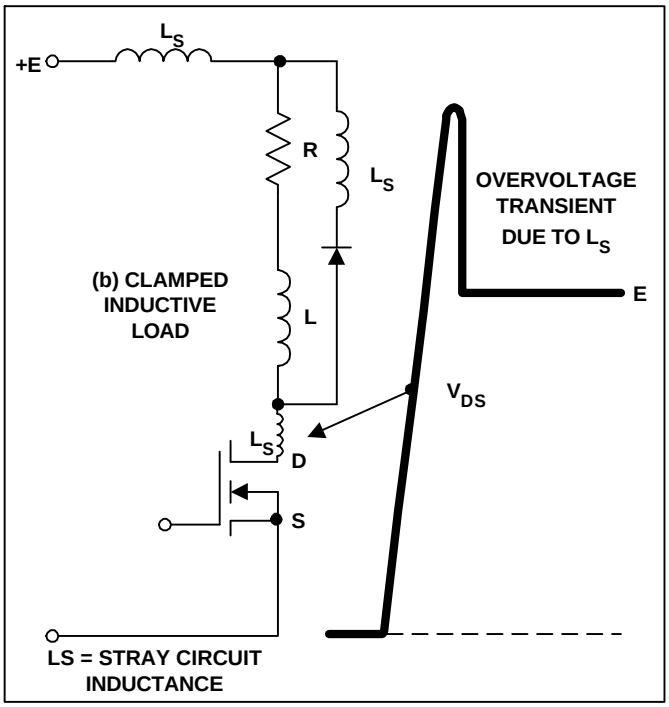

Figure 4. Drain-Source Overvoltage Transient Produced by Stray Circuit Inductance When Switching Off with Clamped, Inductive Load

It should be remembered that a collapse of voltage across the device (i.e., a negative-going dv/dt) will produce a transient negative voltage spike across the gate-source terminals. In this case, of course, there will be no tendency for the device to turn ON, and hence no tendency for the effect to be self-limiting. A zener diode connected to clamp positive transients will automatically clamp negative-going transients, limiting them to the forward conduction voltage drop of the zener.

4. BEWARE OF DRAIN OR COLLECTOR VOLTAGE SPIKES INDUCED BY SWITCHING

The uninitiated designer is often not aware that self-inflicted overvoltage transients can be produced when the device is switched OFF, even though the DC supply voltage for the drain circuit is well below the V_{DS} rating of the transistor.
Figure 3 shows how a voltage spike is produced when switching the device OFF, as a result of inductance in the circuit. The faster the device is switched, the higher the overvoltage will be.
Inductance is always present to some extent in a practical circuit, and therefore, there is always danger of inducing overvoltage transients when switching OFF. Usually, of course, the main inductive component of the load will be "clamped", as shown in Figure 4. Stray circuit inductance still exists, however, and overvoltage transients will still be produced as a result—to say nothing of the fact that the clamping diode may not provide an instantaneous clamping action, due to its "forward recovery" characteristic.

The first approach to this problem is to minimize stray circuit inductance, by means of careful attention to circuit layout, to the point that whatever residual inductance is left in the circuit can be tolerated. HEXFET®s have an inductive energy rating that makes capable of withstanding these inductive spikes, assuming that the data sheet limits for energy and temperature are not violated. IGBTs, however, do not have an avalanche rating, and a clamping device should be connected, physically as close as possible to the drain and source terminals, as shown in Figure 5. A conventional zener diode, or a "transorb" clamping device, are satisfactory for this purpose. An alternative clamping circuit is shown in Figure 6, depending on the voltage and current rating of the circuit.
The capacitor C is a reservoir capacitor and charges to a substantially constant voltage, while the resistor R is sized to dissipate the "clamping energy" while maintaining the desired voltage across the capacitor. The diode D must be chosen so that its forward recovery characteristic does not significantly spoil the transient clamping action of the circuit. A simple RC snubber can also be used, as shown in Figure 7. Note, however, that an RC snubber not only limits the peak voltage, it also slows down the effective switching speed. In so doing, it absorbs energy during the whole of the switching period, not just at the end of it, as does a voltage clamp. A snubber is therefore less efficient than a true voltage clamping device.

Note that the highest voltage transient occurs when switching the highest level of current. The waveform of the voltage across the device should be checked with a high-speed oscilloscope at the full load condition to ensure that switching voltage transients are within safe limits.

5. DO NOT EXCEED THE PEAK CURRENT RATING

All power transistors have a specified maximum peak current rating. This is conservatively set at a level that guarantees reliable operation and it should not be exceeded. It is often overlooked that, in a practical circuit, peak transient currents can be obtained that are well in excess of the expected normal operating current, unless proper precautions are taken. Heating, lighting and motor loads, for example, consume high in-rush currents if not properly controlled. A technique that ensures that the peak current does not exceed the capability of the device is to use a current sensing control that switches it OFF whenever the current instantaneously reaches a preset limit.

Unexpectedly high transient current can also be obtained as a result of rectifier reverse recovery, when a transistor is switched ON rapidly into a conducting rectifier. This is illustrated in Figure 8. The solution is to use a faster rectifier, or to slow down the switching of the transistor to limit the peak reverse recovery current of the rectifier.

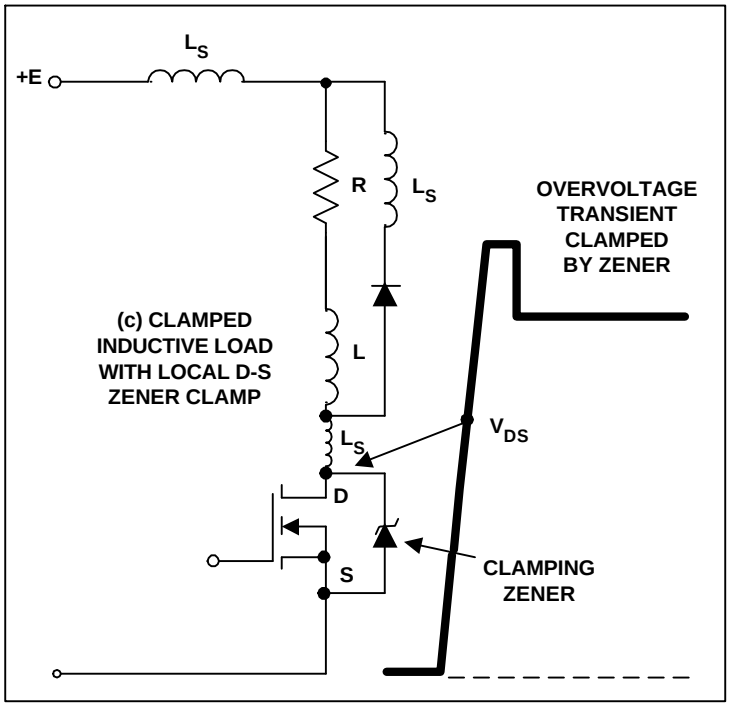

Figure 5. Overvoltage Transient at Switch-Off Clamped by Local Drain-Source Zener

6. STAY WITHIN THE THERMAL LIMITS

Power transistors are thermally limited. They must be mounted on a heatsink that is adequate to keep the junction temperature within the rated under the "worst case" condition of maximum power dissipation and maximum ambient temperature.

It must be remembered that in a switching application, the total power is due to the conduction losses and the switching loss. Switching time and switching losses of HEXFET®s are essentially independent of temperature, but the conduction losses increase with increasing temperature, because $R_{DS(on)}$ increases with temperature. IGBTs, on the contrary, have switching losses that highly dependent of temperature, while conduction losses are not. This must be taken into account when sizing the heatsink. The required thermal resistance of the heatsink can be calculated as follows:

The transistor conduction power, P_T, is given approximately by *P_T = On-state Voltage x Drain or Collector current*

The switching energy depends upon the voltage and current being switched and the type of load. The total switching loss, P_S, is the total switching energy, ε_T, multiplied by the operating frequency, f. e_T is the sum of the energies due to the individual switchings that take place in each fundamental operating cycle:

$$P_S = \varepsilon_T f$$

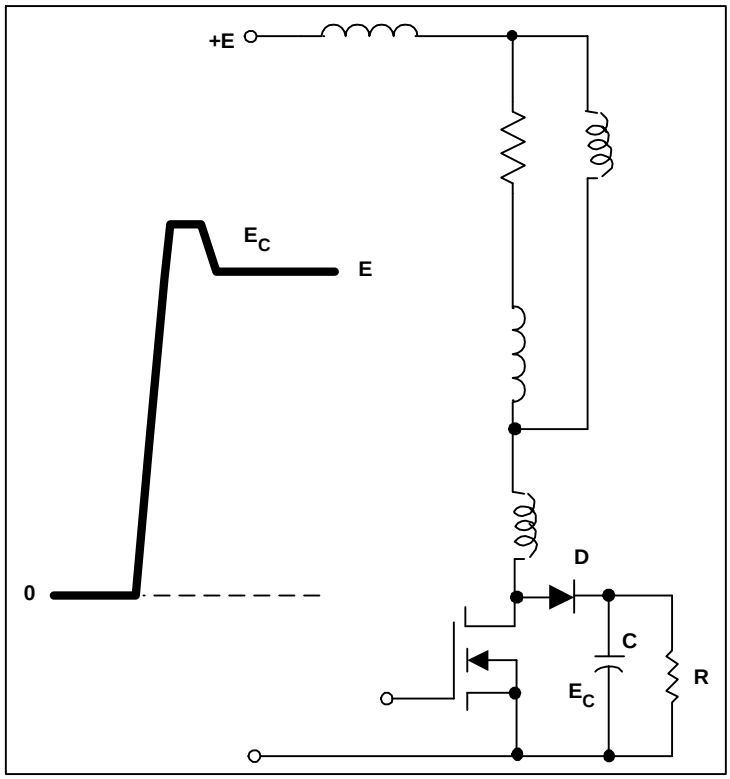

Figure 6. Overvoltage Transient at Switch-Off Limited by Local Clamp

The total power dissipation is the sum of the conduction power, P_T, and the switching power, P_S.

$$P = P_T + P_S$$

Since:

$$\Delta T_{JA} = PR_{th}$$

where:

R_{th} = junction-to-ambient thermal resistance

The junction-to-ambient thermal resistance, R_{JA}, is made up of the internal junction-to-case thermal resistance, R_{JC}, plus the case-to-heatsink thermal resistance, R_{CS}, plus the sink-to-ambient thermal resistance, R_{SA}. The first two terms are fixed for the device, and the required thermal resistance of the heatsink, R_{S-A}, for a given junction temperature rise DT_{J-A}, can be calculated from:

$$R_{S-A} = R_{J-A} - (R_{JC} + R_{C-S})$$

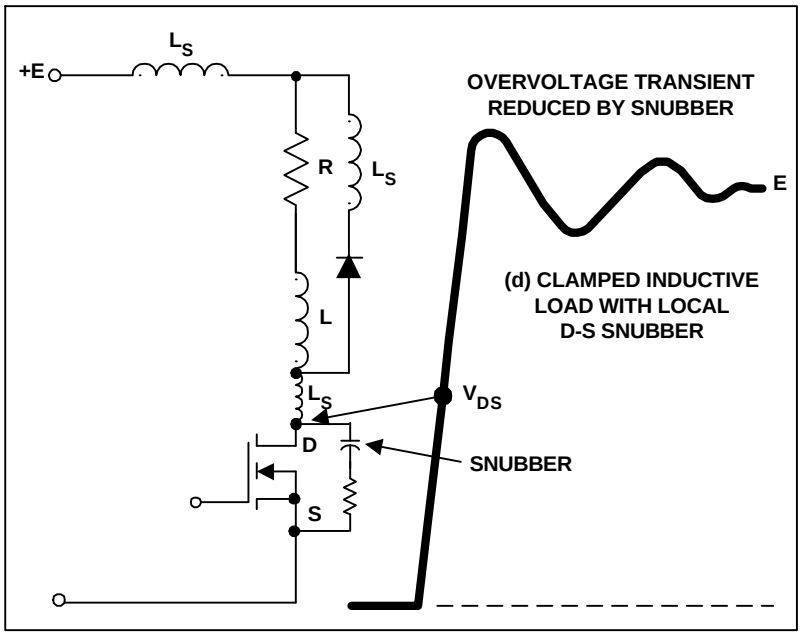

Figure 7. Overvoltage Transient at Switch-Off Limited by Local Capacitor-Resistor Snubber

7. PAY ATTENTION TO CIRCUIT LAYOUT

Stray inductance in the circuit can cause overvoltage transients, slowing down of the switching speed, unexpected unbalance of current between parallel connected devices, and unwanted oscillations.

In order to minimize these effects, stray circuit inductance must be minimized. This is done by keeping conduction paths as short as possible, by minimizing the area of current loops, by using twisted pairs of leads, and by using ground plane construction. Local decoupling capacitors alleviate the affects of any residual circuit inductance, once these measures have been taken. Circuit layout should be kept as symmetrical as possible in order to maintain balanced currents in parallel connected HEXFET®s or IGBTs. The gates of parallel connected devices should be decoupled by small ferrite beads placed over the gate connections, or by individual resistors in series with each gate. These measures prevent parasitic oscillations.

8. BE CAREFUL WHEN USING THE INTEGRAL BODY-DRAIN DIODE

The HEXFET®'s integral body-drain diode exhibits minority carrier reverse recovery. Reverse recovery presents a potential problem when switching any rectifier off; the slower the rectifier, the greater the problem. By comparison with the HEXFET® itself, the switching speed of the integral reverse rectifier is quite slow. The switching speed of a circuit which utilizes the body-drain diode of the HEXFET® may therefore be limited by the rectifier. Whether this will be so depends upon the circuit and the operating conditions.

Regardless of the overall circuit configuration, or the particular application, the "local" circuit operating situation that is troublesome occurs when the freewheeling current from an inductive load is commutated from the integral rectifier of one HEXFET® to the transistor of an "opposite" HEXFET®, the two devices forming a tandem series connected pair across a low impedance voltage source, as shown in Figure 8. This “local” circuit configuration occurs in most chopper and inverter schemes.

If the incoming HEXFET® switches ON too rapidly, the peak reverse recovery current of the integral body-drain diode of the opposite HEXFET® will rise too rapidly, the peak reverse recovery current rating will be exceeded, and the device may possibly be destroyed.

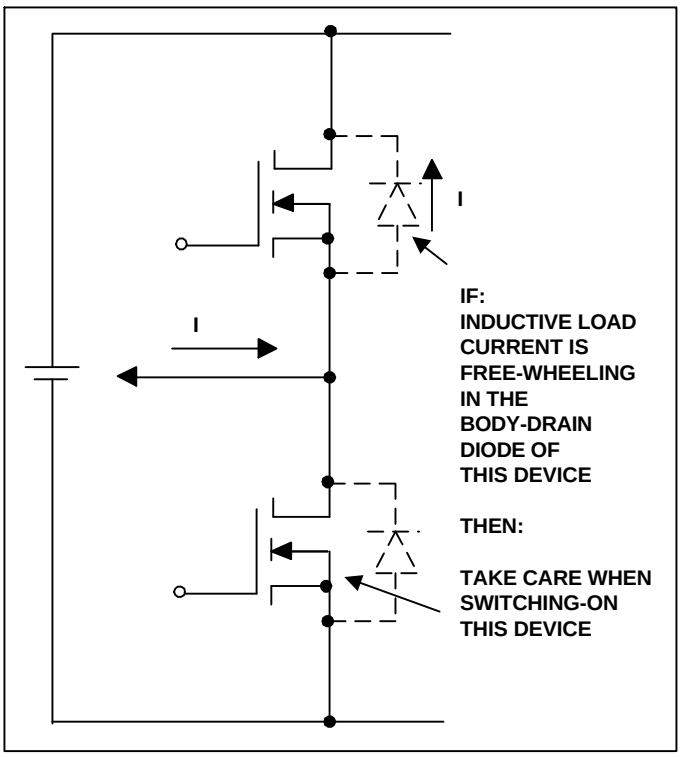

Figure 8. Local Circuit Configuration and Operating Condition Requiring Special Care When Using the HEXFET's Integral Body-Drain Diode.

The peak reverse recovery current of the rectifier can be reduced by slowing down the rate of change of current during the commutation process. The rate of change of current can be controlled by purposefully slowing down the rate of rise of the gate driving pulse. Using this technique, the peak current can be reduced to almost any desired extent, at the expense of prolonging the high dissipation switching period.

The oscillograms in Figure 9 illustrate the effect. By slowing the total switch-ON time from 300ns to 1.8ms, the peak current of the IRF330 has been decreased from 20A to 10A. The energy dissipation associated with the “unrestrained” switch-ON in Figure 9(a) is 0.9mJ, whereas it is 2.7mJ for the controlled switch-ON of Figure 9(b).

Note also that it is not necessary to slow the switching-OFF of the HEXFET®, hence the energy dissipation at switch-OFF will be relatively small by comparison with that at switch-ON. For operation at frequencies up to a few kHz, where ultra-fast switching is not mandatory, slowing the applied gate drive signal to reduce the peak reverse recovery current of the "opposite" rectifier offers a good practical solution.

9. BE ON YOUR GUARD WHEN COMPARING CURRENT RATINGS

The user can be forgiven if he assumes that the continuous drain current rating, that appears on the data sheet represents the current at which the device can actually be operated continuously in a practical system. To be sure, that's what it should represent; unfortunately it often does not.

Frequently a "continuous" current rating is assigned to the device which in practical terms cannot be used, because the resulting conduction power dissipation would be so large as to require a heatsink with an impractically low thermal resistance, and/or an impractically low ambient operating temperature. The best advice to the user is to compare different types *on the basis of high temperature conduction and switching losses*, and not of current rating. For MOSFETS, it is sufficient to compare $R_{DS(on)}$ at 25° C, and this provides a common basis for comparison. This parameter, taken in conjunction with the junction-case thermal resistance, is a much better indication of the power MOSFET true current handling capability.

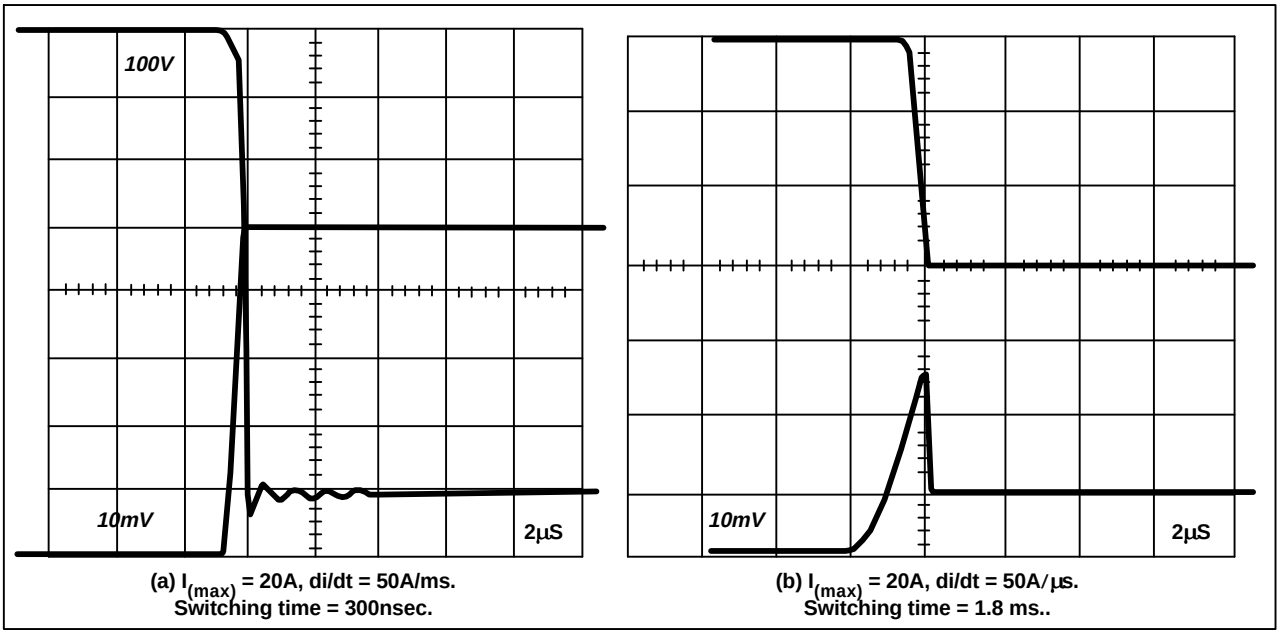

Figure 9. Oscillograms of IRF330 Switching into Reverse Rectifier of Another IRF330 with Freewheeling Current of 4A.
Top Trace: Voltage 100V/div.
Bottom Trace: Current 4A/div.
Time Scale: 2ms/div.