Application Note AN-941

PARALLELING POWER MOSFETs

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Abstract:

Whenever devices are operated in parallel, due consideration should be given to the sharing between devices to ensure that the individual units are operated within their limits. Items that must be considered to successfully parallel MOSFETs are: gate circuitry, layout considerations, current unbalance, and temperature unbalance.

This application note covers these topics and provides guidelines on paralleling.

General observations

Paralleling reduces conduction losses and junction-to-case thermal resistance. However, switching losses remain the same, or may even increase. If they are the dominant losses, only a thermal resistance improvement will be achieved by paralleling. Paralleling to take advantage of lower price of smaller devices should not be attempted without due consideration of the technical risks. It is a good engineering practice when paralleling semiconductors to obtain experimental results at the extremes of the manufacturing tolerances.

Paralleling of multiple discretes requires that power losses and, more importantly, junction temperatures of each device be equalized as much as possible. Some unbalance of losses is inevitable because of differences in electrical characteristics between different devices. This will require a certain amount of current de-rating, typically around 20%.

Even with this de-rating tight thermal coupling is necessary to ensure that individual junction temperatures stay close to each other. The isolation pad that is normally placed between the package and the sink tends to decouple junction temperatures and increases temperature differentials. From this point of view, the worst possible mounting method would be to place the paralleled devices on separate heatsinks.

A common heatspreader is a very effective way of keeping the semiconductors at the same temperature. It also serves as a mechanical carrier during assembly. If electrical isolation is required the isolation barrier can be placed between the carrier and the heatsink.

Unbalances due to circuit layout

External circuit unbalance due to non-symmetrical layout can cause significant differences in losses between paralleled devices. The most serious effects of non-symmetrical layout is the current unbalance during switching intervals and the resulting unbalance in switching losses. This will be discussed in more detail in the following sections.

Generally speaking, voltage equality is ensured by the fact that the devices are in parallel. However, under transient conditions, voltage differentials can appear across devices due to di/dt effects in unequalized stray inductances. The most serious stray circuit element to be balanced is the inductance in series with the source that is common to the gate circuit (“common source inductance”; see Figure 1). The voltage that develops across this inductance due to the di/dt at turn-on and turn-off counteracts the applied gate drive voltage and slows down the rate of change of the source current.

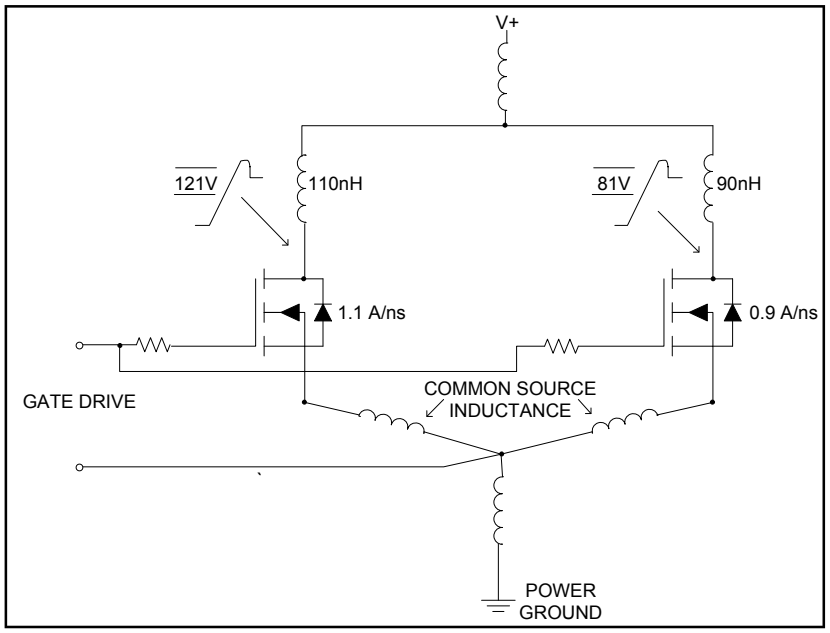

Figure 1. Common Source Inductance

If switching losses are relatively small in relation to conduction losses, a certain amount of circuit-induced unbalance of switching losses can be tolerated and layout will not be super-critical. In this case, the simple in-line arrangement that is frequently used can be satisfactory, even though not symmetrical. See Figure 2(A).

If switching losses are significant, careful attention to layout is important. The circular layout shown in Figure 2(B) is much superior in terms of balancing common source inductances and equalizing switching losses.

Individual stray inductances that are in series with the drain are of lesser concern. An unbalance of 10% in these stray inductances, combined with a di/dt unbalance of 10% translates in an unbalance of 20% in the overshoot seen at turn-off (81 vs. 121V). See Figure 1. However, if the overshoot does not violate the ratings of the MOSFET, the differential in turn-off losses is negligible. The layout of Figure 2(B) will equalize the stray inductances and associated overshoot. Differences in di/dt are generally contained and do not impact switching energy in a significant way.

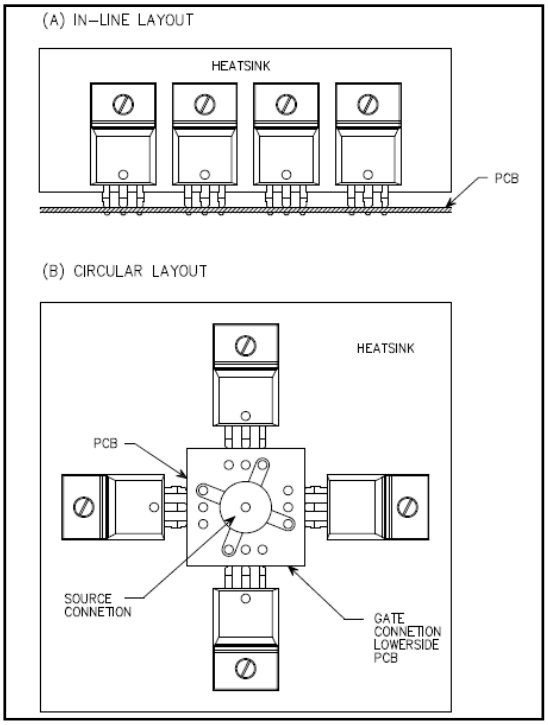

Figure 2 (A) and (B). Different Layouts

Gate oscillations

It is common knowledge that paralleled MOSFETs must have individual gate resistors. As shown in Figure 3, paralleled MOSFETs have a common low impedance path that is prone to parasitic self oscillations. This is analyzed in greater detail in Ref [1]. Individual gate resistors provide the necessary damping and gate decoupling to prevent oscillations.

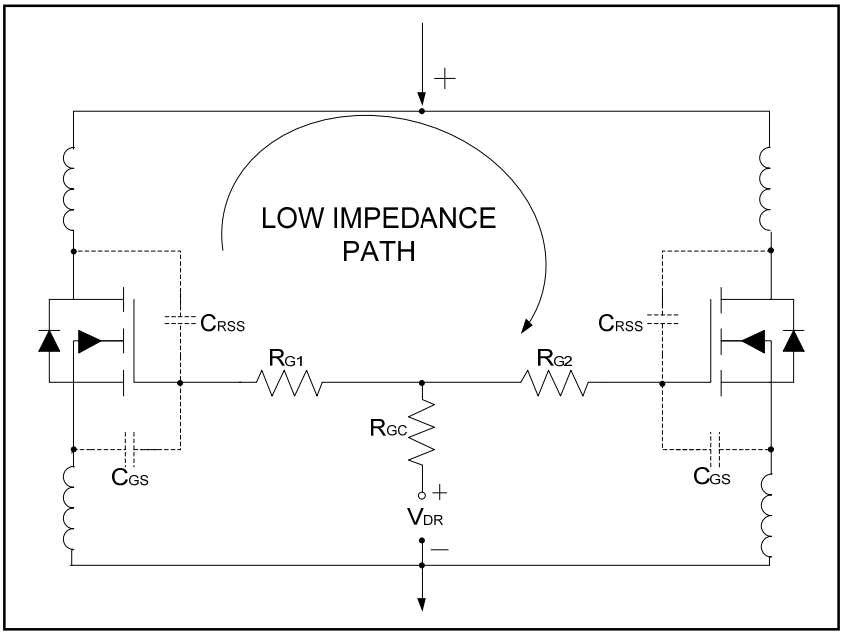

Figure 3. Low impedance path for parasitic oscillation

Excessive amounts of gate resistance degrade the switching performance of the devices and increase switching unbalance. Only the required amount should be used.

Current unbalances in steady state operation

During the periods outside of the switching transitions, the current in a parallel group of MOSFETs distributes itself in the individual devices in inverse proportion to their on-resistance. The device with the lowest on-resistance will carry the highest current. The positive temperature coefficient of the on-resistance tends to compensate this unbalance and equalize the currents.

This self-balancing mechanism is countered by the tight thermal coupling recommended in the previous section. It should be remembered, however, that semiconductor devices fail mainly because of excessive temperature and rarely because of excessive steady-state current.

The MOSFET integral diode does not have a positive temperature coefficient of voltage drop. Hence large steady-state current unbalances can occur during diode conduction. This is seldom a problem, however, because the on-resistance of the MOSFET integral with the diode that carries more current increases and, in any event, the thermal coupling insures that the junction temperature does not deviate much from the other parallel devices.

A specific example of steady-state unbalance is analyzed in the Appendix. A more detailed analysis can be found in Ref. [1].

Dynamic sharing at turn-on

Power MOSFETs do not have identical threshold and gain characteristics: the device with lower threshold and higher transconductance will tend to switch sooner than others, and attempt to take more than its share of the current. Adding to the problem is the fact that circuit inductance associated with each device may be different, and this will also contribute to unbalancing the current under switching conditions. Here we will provide a brief qualitative description of the different events that occur during a switching transition.

The problem will be introduced by considering the switching waveforms for a typical clamped inductive load. Figure 4 shows waveforms of drain current, drain-to-source voltage, and gate voltage during the turn-on interval. For reasons of clarity we have shown the applied drive pulse increasing at a relatively slow rate.

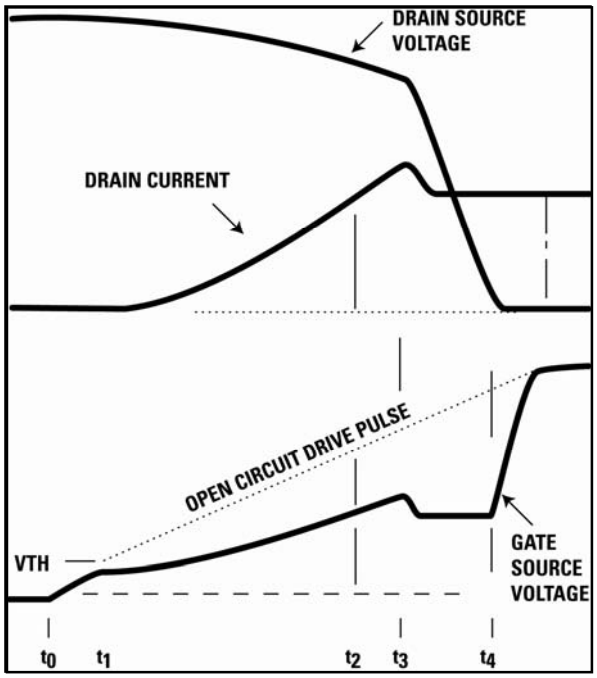

Figure 4. Waveforms at turn-ON

At time t_0, the drive pulse starts its rise. At t_1, it reaches the threshold voltage of the MOSFET, and the drain current starts to increase. At this point two things happen which make the gate-source voltage waveform deviate from its original “path." First, inductance in series with the source which is common to the gate circuit develops an induced voltage, as a result of the increasing source current. This voltage counteracts the applied gate drive voltage and slows down the rate-of-rise of voltage appearing directly across the gate and source terminals; this, in turn, slows down the rate-of-rise of the source current.

The second factor that influences the gate-source voltage is the so called "Miller" effect. During the period t_1 to t_2, some voltage is dropped across circuit inductance in series with the drain, and the drain-source voltage starts to fall. The decreasing drain-source voltage is reflected across the drain-gate capacitance, pulling a discharge current through it, and increasing the effective capacitance load on the drive circuit. This, in turn, increases the voltage drop across the impedance of the drive circuit and decreases the rate-of-rise of voltage appearing between the gate and source terminals. This also is a negative feedback effect; increasing current in the drain results in a fall of drain-to-source voltage, which, in turn, slows down the rise of gate-source voltage and tends to resist the increase of drain current. These effects are illustrated diagrammatically in Figure 5.

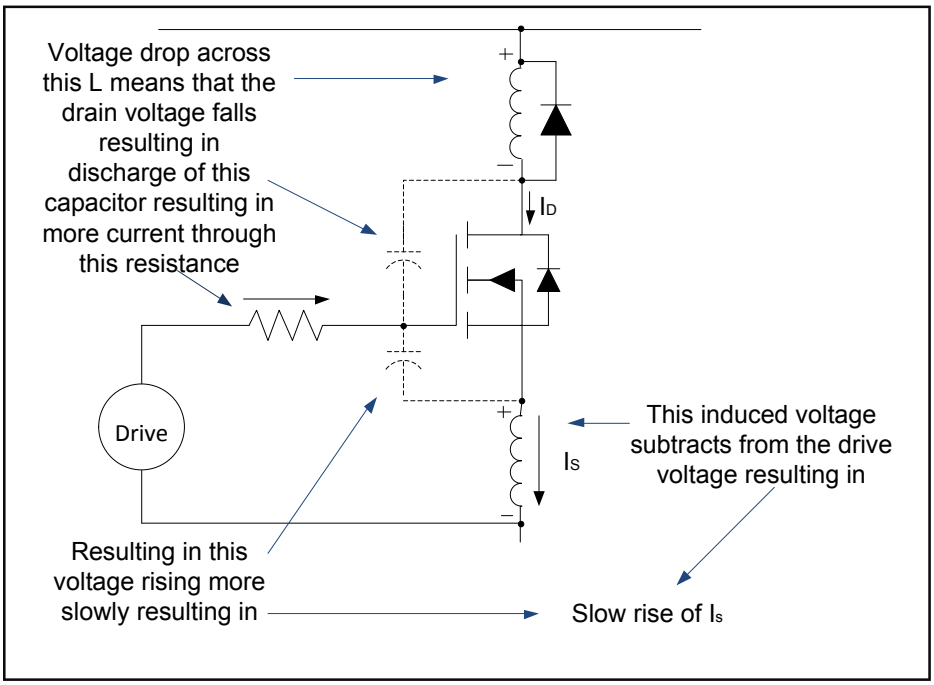

Figure 5. Representation of effects when switching-ON

This state of affairs continues throughout the period t_1 to t_2, while the current in the MOSFET rises to the level of the current flowing in the freewheeling rectifier, and it continues into the next period, t_2 to t_3, while the current increases further, due to the reverse recovery of the freewheeling rectifier.

At time t_3, the freewheeling rectifier starts to support voltage, while the drain current and the drain voltage start to fall. The rate-of-fall of drain voltage is now governed by the Miller effect, and an equilibrium condition is reached, under which the drain voltage falls at just the rate necessary for the voltage between gate and source terminals to satisfy the level of drain current established by the load. This is why the gate-to-source voltage falls as the recovery current of the freewheeling rectifier falls, then stays constant at a level corresponding to the load current, while the drain voltage is falling.

Finally, at time t_4, the MOSFET is in full conduction, and the gate-to-source voltage rises rapidly towards the applied "open circuit" value.

The above explanation, summarized in Figure 5, provides the clue to the difficulties that can be expected with parallel connected devices. The first potential difficulty is that if we apply a common drive signal to all gates in a parallel group, then the first device to turn ON—the one with the lowest threshold voltage—will tend to slow the rise of voltage on the gates of the others, and further delay the turn-on of these devices. This will be due to the Miller effect. The inductive feedback effect, on the other hand, only influences the gate voltage of its own device (assuming that each source has its own separate inductance).

The second potential difficulty is that, with unequal source inductances a dynamic unbalance of current will result, even if the devices themselves are perfectly matched. Obviously, the solution to this is to ensure that inductances associated with the individual devices are as nearly equal as possible. This can be done by proper attention to the circuit layout.

As examined in detail in Ref. [1], there are several other circuit and device parameters that will contribute to dynamic unbalance. The conclusions presented in the above mentioned paper indicate, however, that the problem is not severe, as long as attention is paid to the general guidelines presented in this application note.

Dynamic sharing at turn-off

Similar considerations apply to the dynamic sharing of current during the turn-off interval. Figure 6 shows theoretical waveforms during the turn-off interval. At t_0, the gate drive starts to fall. At t_1, the gate voltage reaches a level that just sustains the drain current. The drain-to-source voltage now starts to rise. The Miller effect governs the rate-of-rise of drain voltage and holds the gate-to-source voltage at a level corresponding to the constant drain current. At t_3, the rise of drain voltage is complete, and the gate voltage starts to fall at a rate determined by the gate-source circuit impedance, while the drain current falls to zero.

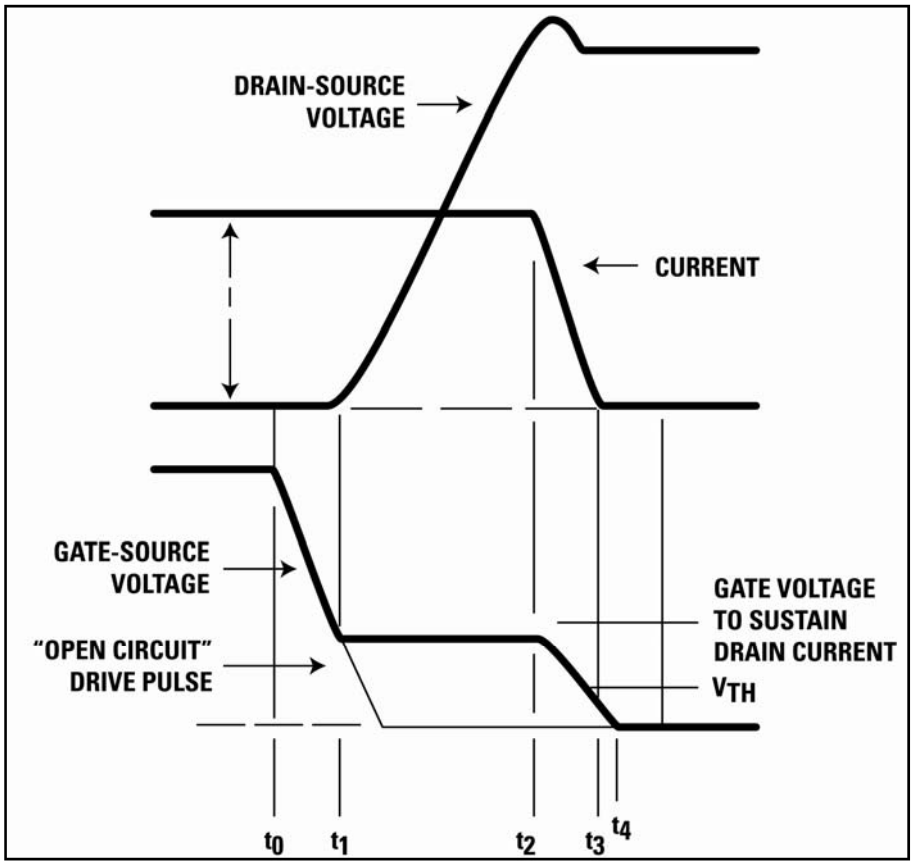

Figure 6. Typical waveforms at Turn-OFF

Figure 7 shows theoretical waveforms for two parallel connected MOSFETs with their gates connected directly together. For purposes of discussion, the source inductance is assumed to be zero. At t_1, the gate voltage reaches the point at which MOSFET B can no longer sustain its drain current.

The load current now redistributes; current in MOSFET B decreases, while that in MOSFET A increases. At t_2, MOSFET B can no longer sustain its current; both MOSFETs now operate in their 'linear" region, and the drain voltage starts to rise. The gate-to-source voltage is kept practically constant by the Miller effect, while the currents in the two MOSFETs remain at their separate levels. Clearly, the unbalance of current in this example is significant.

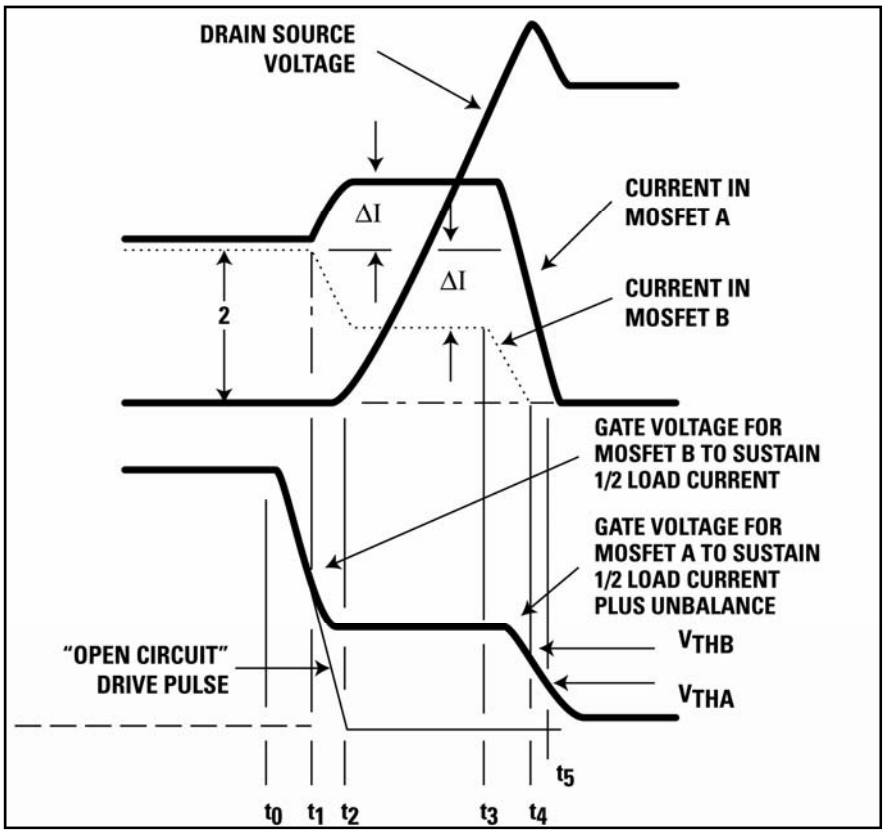

Figure 7. Effects of paralleling on turn-off waveforms

While a turn-off unbalance is potentially a more serious problem, the analysis in Ref. [1] shows that this problem can be satisfactorily contained by turning off the MOSFETs with a "hard" (very low impedance) gate drive. This by itself will almost guarantee limited dynamic unbalance at turn-off.

In summary, to achieve good sharing at turn-off the same precautions should be used as for turn-on, with the addition of a "hard" drive.

In summary

It is advisable to follow these general guidelines should be followed when paralleling MOSFETs:

- Use individual gate resistors to eliminate the risk of parasitic oscillation.
- Ensure that paralleled devices have a tight thermal coupling.
- Equalize common source inductance and reduce it to a value that does not greatly impact the total switching losses at the frequency of operation.
- Reduce stray inductance to values that give acceptable overshoots at the maximum operating current.
- Ensure the gate of the MOSFET is looking into a stiff (voltage) source with as little impedance as practical.
- Zener diodes in gate drive circuits may cause oscillations. When needed, they should be placed on the driver side of the gate decoupling resistor(s).
- Capacitors in gate drive circuits slow down switching, thereby increasing the switching unbalance between devices and may cause oscillations.
- Stray components are minimized by a tight layout and equalized by symmetrical position of components and routing of connections.

Appendix – Steady-state Unbalance Analysis

An analysis of the "worst case" device current in a group of "N" parallel connected devices can be based on the simplifying assumption that (N - 1) devices have the highest limiting value of ON-resistance, while just one lone device has the lowest limiting value of ON-resistance. The analysis can then be concentrated on the current in this one device.

The equivalent electrical circuit shown in Figure A1 simplifies the analysis further by assuming the number of devices is sufficiently large that the current that flows through each of the high resistance devices is approximately $I_{TOT}/(N-1)$. On this assumption, the voltage drop across the lone low resistance device, and hence the current in it, can be calculated.

The ON-resistance of each of the "high resistance" devices, at operating temperature, T, is given by:

$$R_{(max)T} = R_{(max)25}\left(1+\left[\left(T_A - 25\right)+\frac{I^2_{TOT}}{(N-1)^2}R_{(max)T}\,R_{JA}\right]K\right) \quad (1)$$

where $R_{(max)25}$ is the limiting maximum value of ON-resistance at 25°C, R_{JA} is the total junction-to-ambient thermal resistance in degrees C/ W, and K is the per unit change of ON-resistance per °C.

Hence,

$$R_{(max)\,T} = \frac{R_{(max)\,25}\left(1+\left[T_A - 25\right]K\right)}{1 - R_{(max)\,25}\dfrac{I^2{}_{TOT}}{(N-1)^2}R_{JA}K} \quad (2)$$

The voltage drop, V, across the parallel group is:

$$V = \frac{I_{TOT}}{(N-1)} \bullet R_{(max)T} \quad (3)$$

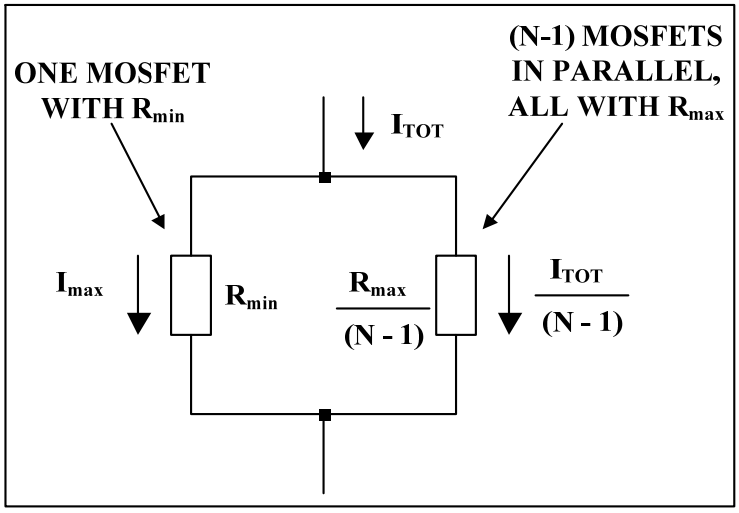

Figure A1. Simplified equivalent circuit for estimating worst case steady-state current unbalance

The resistance of the one low resistance device at its operating temperature is:

$$\mathbf{R_{(min)T} = R_{(min)25}\left(1+\left[\left(T_A - 25\right) + V\, I_{(max)}\, R_{JA}\right] K\right)} \quad (4)$$

where $R_{(min)\,25}$ is the limiting minimum value of ON-resistance at 25°C, and $I_{(max)}$ is the current in this device.

But,

$$R_{(\min)\,T} = \frac{V}{I_{(\max)}} \quad (5)$$

Hence,

$$I(\max) = \frac{-b + \sqrt{(b^2 - 4aV)}}{2a}$$

where:
$b = R_{(min)\,25}\,(1 + [T_A - 25]\,K)$
$a = R_{(min)\,25}\,V\,R_{JA}\,K$

The following example shows the “worst case" degree of current sharing that can be expected, by applying the above relationships to the IRFP150 MOSFET, and making the following assumptions:

$R_{(max)\,25} = 0.045\Omega$
$R_{(min)\,25} = 0.035\Omega$
$R_{JA} = 3$ deg. C/W

$$\frac{\mathbf{I_{TOT}}}{\mathbf{(N-1)}} = \mathbf{20A} \quad (6)$$

K = 0.006 per degree C
$T_A = 35°C$

Using the relationships (2), (3), and (5) above, it can be calculated that the "worst case" maximum value of device current is 27A for the hypothetical situation where all devices but one have high limiting ON-resistance, of 0.0452Ω and carry 20A each, whereas the remaining one has low limiting ON-resistance of 0.03Ω.

References:

1. J.B. Forsythe: "Paralleling of Power MOSFETs." IEEE-IAS Conference Record, October 1981.