



# OPA606

## Wide-Bandwidth *Difet*® OPERATIONAL AMPLIFIER

### FEATURES

- WIDE BANDWIDTH: 13MHz typ
- HIGH SLEW RATE: 35V/μs typ
- LOW BIAS CURRENT: 10pA max at  $T_A = +25^\circ\text{C}$
- LOW OFFSET VOLTAGE: 500μV max
- LOW DISTORTION: 0.0035% typ at 10kHz

### APPLICATIONS

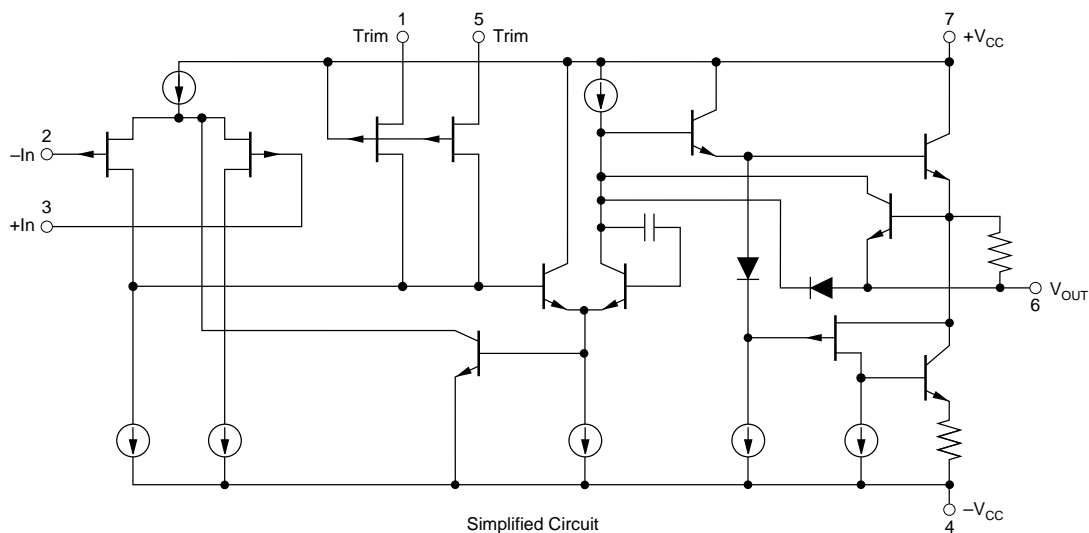
- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT
- AUDIO AMPLIFIERS

### DESCRIPTION

The OPA606 is a wide-bandwidth monolithic dielectrically-isolated FET (*Difet*®) operational amplifier featuring a wider bandwidth and lower bias current than BIFET® LF156A amplifiers. Bias current is specified under warmed-up and operating conditions, as opposed to a junction temperature of  $+25^\circ\text{C}$ .

Laser-trimmed thin-film resistors offer improved off-set voltage and noise performance.

The OPA606 is internally compensated for unity-gain stability.



*Difet*®; Burr-Brown Corp.

*BIFET*®; National Semiconductor Corp.

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# SPECIFICATIONS

## ELECTRICAL

At  $V_{CC} = \pm 15\text{VDC}$  and  $T_A = +25^\circ\text{C}$  unless otherwise noted.

PARAMETER	CONDITIONS	OPA606KM			OPA606LM			OPA606KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>FREQUENCY RESPONSE</b>											
Gain Bandwidth	Small Signal	10	12.5		11	13		9	12		MHz
Full Power Response	20Vp-p, $R_L = 2\text{k}\Omega$		515			550			470		kHz
Slew Rate	$V_O = \pm 10\text{V}$ , $R_L = 2\text{k}\Omega$	22	33		25	35		20	30		V/ $\mu\text{s}$
Settling Time <sup>(1)</sup> : 0.1%	Gain = -1, $R_L = 2\text{k}\Omega$		1.0			1.0			1.0		$\mu\text{s}$
0.01%	10V Step		2.1			2.1			2.1		$\mu\text{s}$
Total Harmonic Distortion	G = +1, 20Vp-p $R_L = 2\text{k}\Omega$ f = 10kHz		0.0035			0.0035			0.0035		%
<b>INPUT OFFSET VOLTAGE<sup>(2)</sup></b>											
Input Offset Voltage	$V_{CM} = 0\text{VDC}$		$\pm 180$	$\pm 1.5\text{mV}$		$\pm 100$	$\pm 500$		$\pm 300$	$\pm 3\text{mV}$	$\mu\text{V}$
Average Drift	$T_A = T_{MIN}$ to $T_{MAX}$		$\pm 5$			$\pm 3$	$\pm 5$		$\pm 10$		$\mu\text{V}/^\circ\text{C}$
Supply Rejection	$V_{CC} = \pm 10\text{V}$ to $\pm 18\text{V}$	82	100		90	104		80	90		dB
			$\pm 10$	$\pm 79$		$\pm 6$	$\pm 32$		$\pm 32$	$\pm 100$	$\mu\text{V/V}$
<b>BIAS CURRENT<sup>(2)</sup></b>											
Input Bias Current	$V_{CM} = 0\text{VDC}$		$\pm 7$	$\pm 15$		$\pm 5$	$\pm 10$		$\pm 8$	$\pm 25$	pA
<b>OFFSET CURRENT<sup>(2)</sup></b>											
Input Offset Current	$V_{CM} = 0\text{VDC}$		$\pm 0.6$	$\pm 10$		$\pm 0.4$	$\pm 5$		$\pm 1$	$\pm 15$	pA
<b>NOISE</b>											
Voltage, $f_O = 10\text{Hz}$	100% tested (L)		37			30	40		37		$\text{nV}/\sqrt{\text{Hz}}$
100Hz	100% tested (L)		21			20	28		21		$\text{nV}/\sqrt{\text{Hz}}$
1kHz	100% tested (L)		14			13	16		14		$\text{nV}/\sqrt{\text{Hz}}$
10kHz	(3)		12			11	13		12		$\text{nV}/\sqrt{\text{Hz}}$
20kHz	(3)		11			10.5	13		11		$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 10\text{Hz}$ to $10\text{kHz}$	(3)		1.3			1.2	1.5		1.3		$\mu\text{Vrms}$
Current, $f_O = 0.1\text{Hz}$ thru $20\text{kHz}$	(3)		1.5			1.3	2		1.7		$\text{fA}/\sqrt{\text{Hz}}$
<b>IMPEDANCE</b>											
Differential			$10^{13} \parallel 1$			$10^{13} \parallel 1$			$10^{13} \parallel 1$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{14} \parallel 3$			$10^{14} \parallel 3$			$10^{14} \parallel 3$		$\Omega \parallel \text{pF}$
<b>VOLTAGE RANGE</b>											
Common-Mode Input Range		$\pm 10.5$	$\pm 11.5$		$\pm 11$	$\pm 11.6$		$\pm 10.2$	$\pm 11$		V
Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	80	95		85	96		78	90		dB
<b>OPEN-LOOP GAIN, DC</b>											
Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	95	115		100	118		90	110		dB
<b>RATED OUTPUT</b>											
Voltage Output	$R_L = 2\text{k}\Omega$	$\pm 11$	$\pm 12.2$		$\pm 12$	$\pm 12.6$		$\pm 11$	$\pm 12$		V
Current Output	$V_O = \pm 10\text{VDC}$	$\pm 5$	$\pm 10$		$\pm 5$	$\pm 10$		$\pm 5$	$\pm 10$		mA
Output Resistance	DC, Open Loop		40			40			40		$\Omega$
Load Capacitance Stability	Gain = +1		1000			1000			1000		pF
Short Circuit Current		10	20		10	20		10	20		mA
<b>POWER SUPPLY</b>											
Rated Voltage			$\pm 15$			$\pm 15$			$\pm 15$		VDC
Voltage Range,											
Derated Performance		$\pm 5$		$\pm 18$	$\pm 5$		$\pm 18$	$\pm 5$		$\pm 18$	VDC
Current, Quiescent	$I_O = 0\text{mADC}$		6.5	9.5		6.2	9		6.5	10	mA
<b>TEMPERATURE RANGE</b>											
Specification	Ambient Temperature										
	KM, KP, LM	0		+70	0		+70	0		+70	$^\circ\text{C}$
Operating	Ambient Temperature	-55		+125	-55		+125	-40		+85	$^\circ\text{C}$
$\theta_{JA}$			200			200			155		$^\circ\text{C/W}$

NOTES: (1) See settling time test circuit in Figure 2. (2) Offset voltage, offset current, and bias current are measured with the units fully warmed up. (3) Sample tested—this parameter is guaranteed on L grade only.

## ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At  $V_{CC} = \pm 15\text{VDC}$  and  $T_A = T_{MIN}$  to  $T_{MAX}$  unless otherwise noted.

PARAMETER	CONDITIONS	OPA606KM			OPA606LM			OPA606KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>TEMPERATURE RANGE</b> Specification Range	Ambient Temp.	0		+70	0		+70	0		+70	°C
<b>INPUT OFFSET VOLTAGE<sup>(1)</sup></b> Input Offset Voltage Average Drift Supply Rejection	$V_{CM} = 0\text{VDC}$ $V_{CC} = \pm 10\text{V}$ to $\pm 18\text{V}$		$\pm 400$ $\pm 5$ 98 $\pm 13$	$\pm 2\text{mV}$   $\pm 100$		$\pm 335$ $\pm 3$ 100 $\pm 10$	$\pm 750$ $\pm 5$  $\pm 56$		$\pm 750$ $\pm 10$ 95 $\pm 18$	$\pm 3.5\text{mV}$   $\pm 126$	$\mu\text{V}$ $\mu\text{V}/^\circ\text{C}$ dB $\mu\text{V}/\text{V}$
<b>BIAS CURRENT<sup>(1)</sup></b> Input Bias Current	$V_{CM} = 0\text{VDC}$		$\pm 158$	$\pm 339$		$\pm 113$	$\pm 226$		$\pm 181$	$\pm 566$	pA
<b>OFFSET CURRENT<sup>(1)</sup></b> Input Offset Current	$V_{CM} = 0\text{VDC}$		$\pm 14$	$\pm 226$		$\pm 9$	$\pm 113$		$\pm 23$	$\pm 339$	pA
<b>VOLTAGE RANGE</b> Common-Mode Input Range Common-Mode Rejection	$V_{IN} = \pm 10\text{VDC}$	$\pm 10.4$ 78	$\pm 11.4$ 92		$\pm 10.9$ 82	$\pm 11.5$ 95		$\pm 10$ 75	$\pm 10.9$ 88		V dB
<b>OPEN-LOOP GAIN, DC</b> Open-Loop Voltage Gain	$R_L \geq 2\text{k}\Omega$	90	106		95	112		88	104		dB
<b>RATED OUTPUT</b> Voltage Output Current Output	$R_L = 2\text{k}\Omega$ $V_O = \pm 10\text{VDC}$	$\pm 10.5$ $\pm 5$	$\pm 12$ $\pm 10$		$\pm 11.5$ $\pm 5$	$\pm 12.4$ $\pm 10$		$\pm 10.4$ $\pm 5$	$\pm 11.8$ $\pm 10$		V mA
<b>POWER SUPPLY</b> Current, Quiescent	$I_O = 0\text{mADC}$		6.6	10		6.4	9.5		6.6	10.5	mA

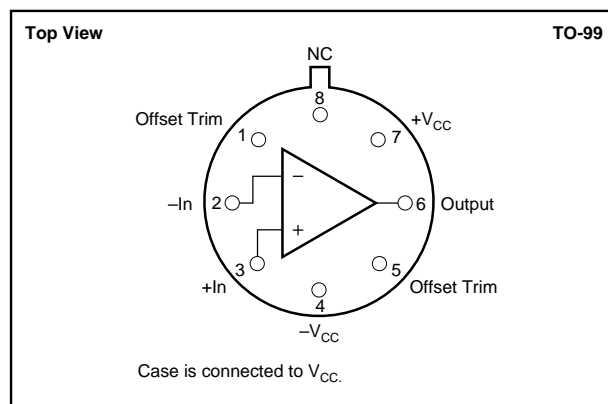
NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up.

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	$\pm 18\text{VDC}$
Internal Power Dissipation <sup>(1)</sup> .....	500mW
Differential Input Voltage .....	$\pm 36\text{VDC}$
Input Voltage Range .....	$\pm 18\text{VDC}$
Storage Temperature Range .....	M = $-65^\circ\text{C}$ to $+150^\circ\text{C}$ P = $-40^\circ\text{C}$ to $+85^\circ\text{C}$
Operating Temperature Range .....	M = $-55^\circ\text{C}$ to $+125^\circ\text{C}$ P = $-40^\circ\text{C}$ to $+85^\circ\text{C}$
Lead Temperature (soldering, 10s) .....	$+300^\circ\text{C}$
Output Short-Circuit Duration <sup>(3)</sup> .....	Continuous
Junction Temperature .....	$+175^\circ\text{C}$

NOTES: (1) Packages must be derated based on  $\theta_{JC} = 15^\circ\text{C}/\text{W}$  or  $\theta_{JA}$ . (2) For supply voltages less than  $\pm 18\text{VDC}$ , the absolute maximum input voltage is equal to the negative supply voltage. (3) Short circuit may be to power supply common only. Rating applies to  $+25^\circ\text{C}$  ambient. Observe dissipation limit and  $T_J$ .

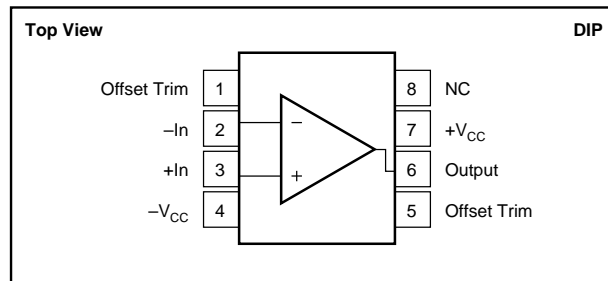
## CONNECTION DIAGRAMS



## PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
OPA606KM	TO-99	001
OPA606LM	TO-99	001
OPA606KP	Plastic DIP	006

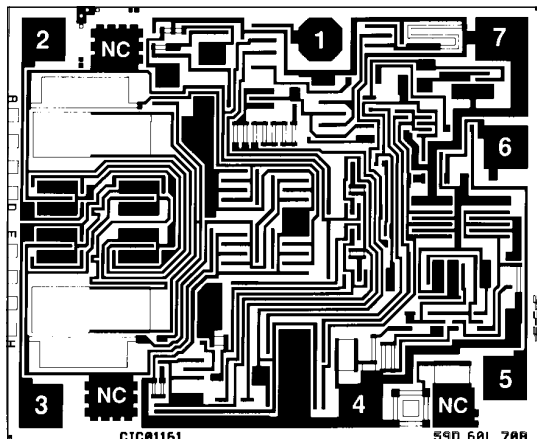
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.



## ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
OPA606KM	TO-99	$0^\circ\text{C}$ to $70^\circ\text{C}$
OPA606LM	TO-99	$0^\circ\text{C}$ to $70^\circ\text{C}$
OPA606KP	Plastic DIP	$0^\circ\text{C}$ to $70^\circ\text{C}$

DICE INFORMATION



OPA606 DIE TOPOGRAPHY

PAD	FUNCTION
1	Offset Trim
2	-In
3	+In
4	-V <sub>S</sub>
5	Offset Trim
6	Output
7	+V <sub>S</sub>
8	NC
NC	No Connection

Substrate Bias: No Connection.

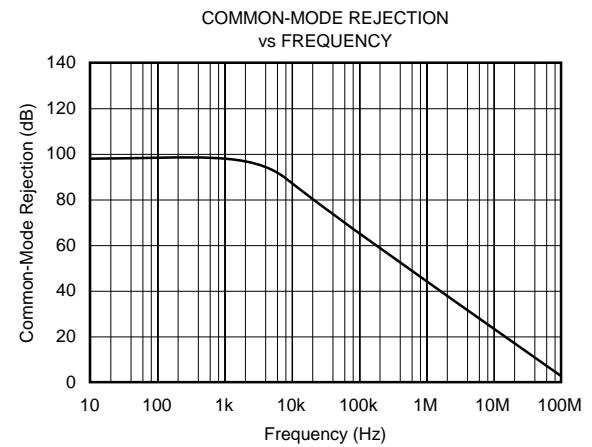
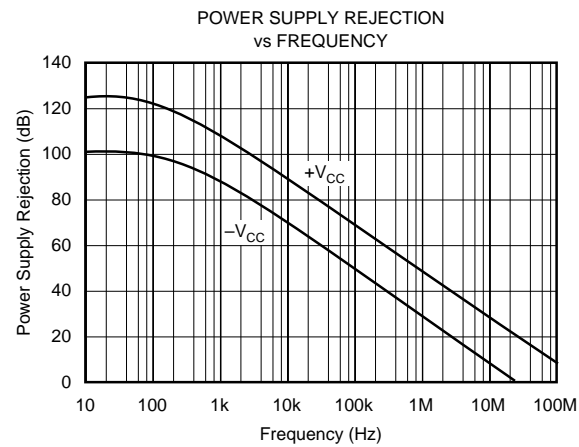
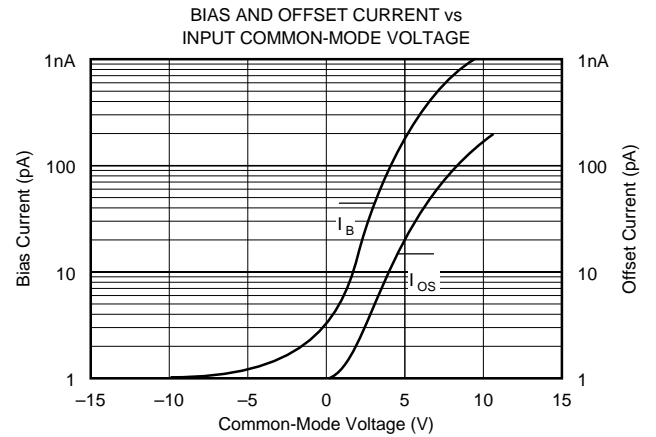
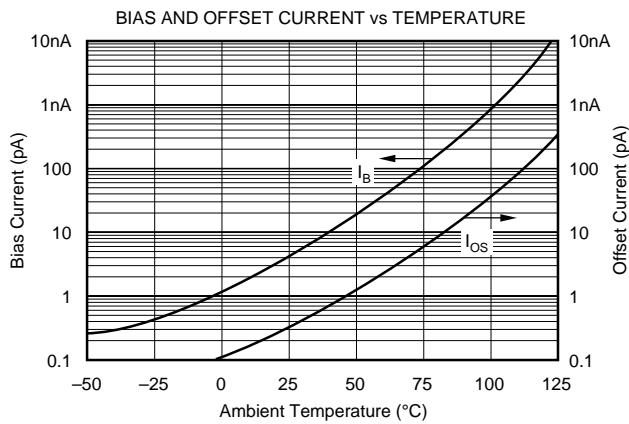
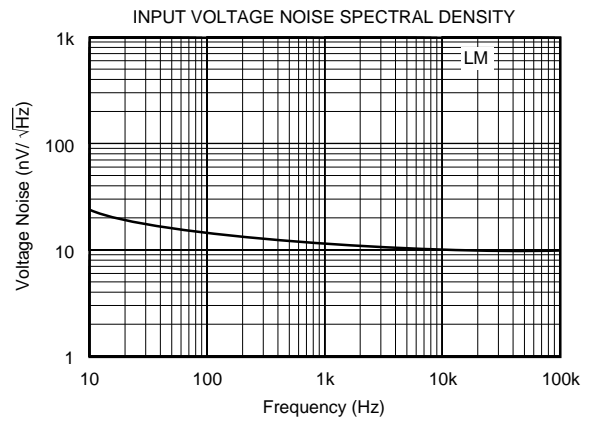
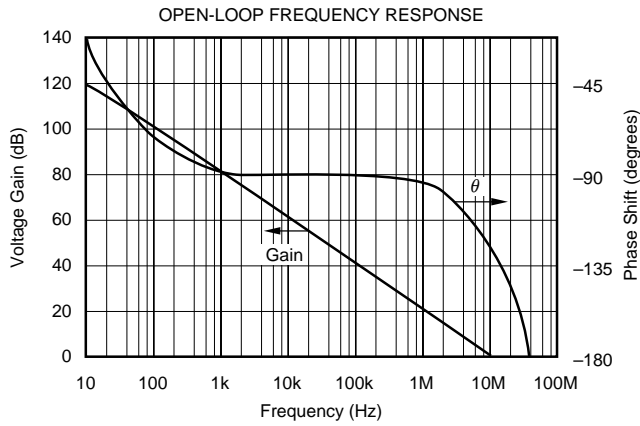
MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	65 x 54 ±5	1.65 x 1.37 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		None
Transistor Count		43

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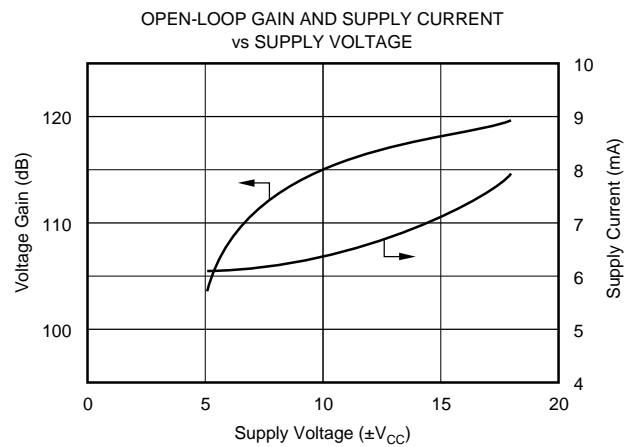
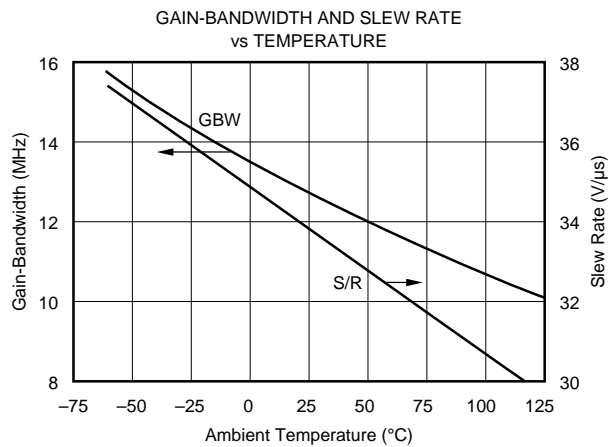
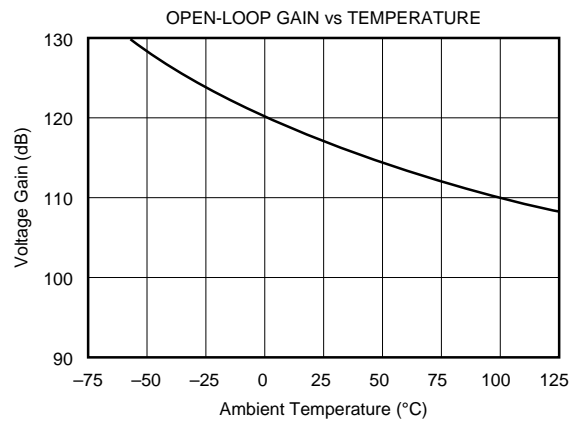
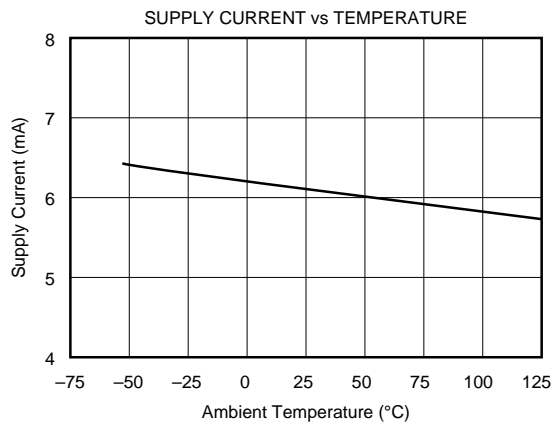
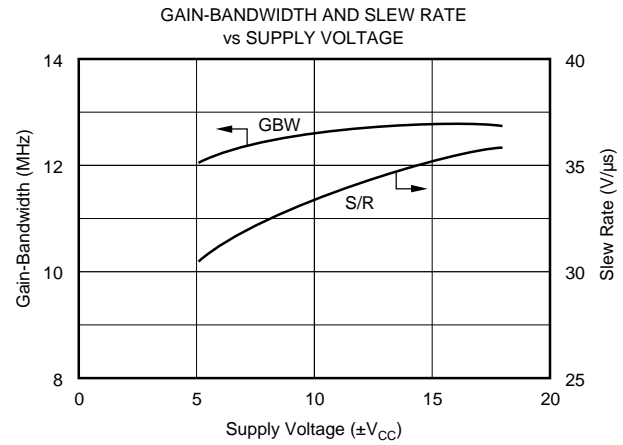
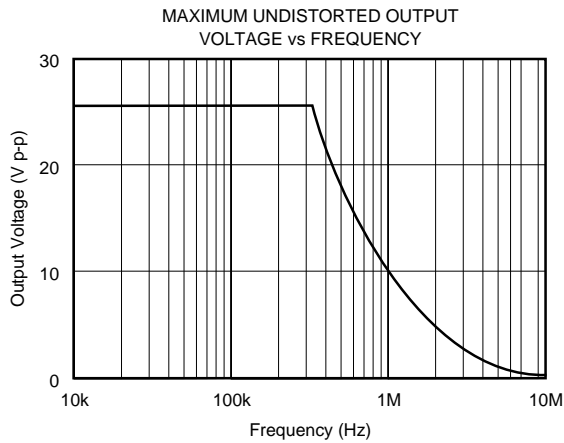
# TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{VDC}$  unless otherwise noted.



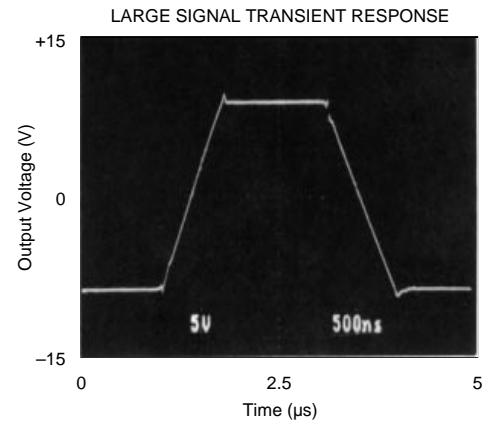
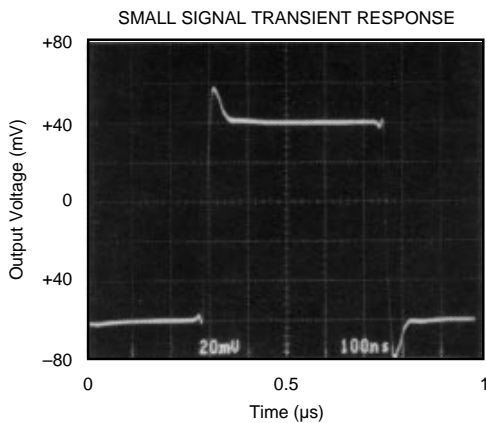
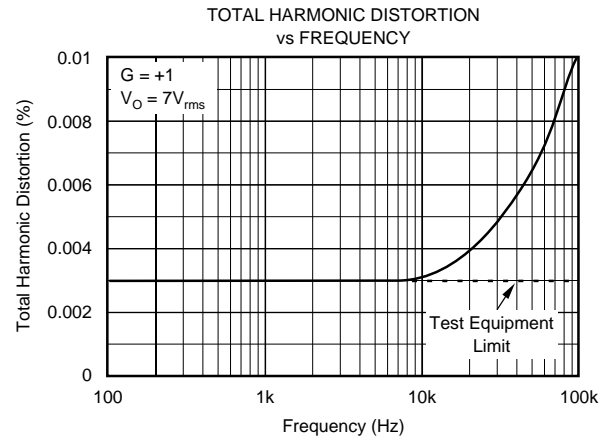
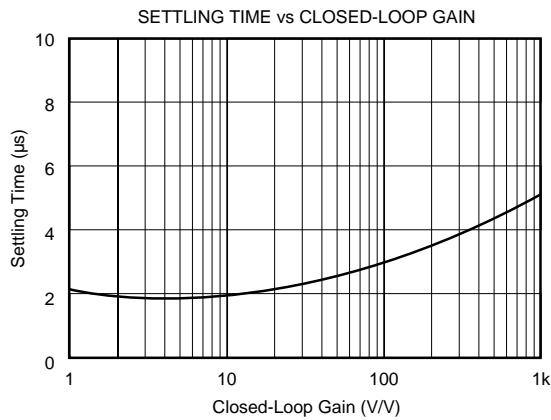
# TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{V}$  unless otherwise noted.



## TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{V}$  unless otherwise noted.



## APPLICATIONS INFORMATION

### OFFSET VOLTAGE ADJUSTMENT

The OPA606 offset voltage is laser-trimmed and will require no further trim for most applications. As with most amplifiers, externally trimming the remaining offset can change drift performance by about  $0.5\mu\text{V}/^\circ\text{C}$  for each millivolt of adjusted offset. Note that the trim (Figure 1) is similar to operational amplifiers such as LF156 and OP-16. The OPA606 can replace most other amplifiers by leaving the external null circuit unconnected.

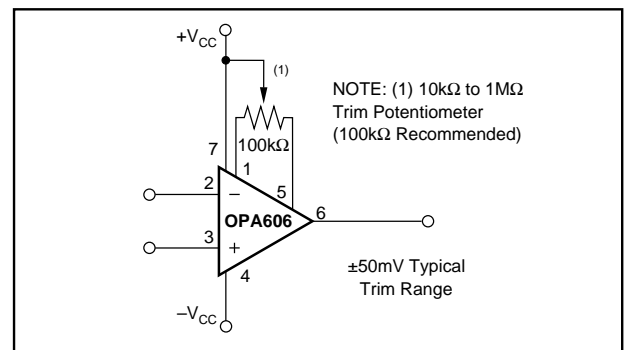


FIGURE 1. Offset Voltage Trim.

## INPUT PROTECTION

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

If the input voltage exceeds the amplifier's negative supply voltage, input current limiting must be used to prevent damage.

## CIRCUIT LAYOUT

Wideband amplifiers require good circuit layout techniques and adequate power supply bypassing. Short, direct connections and good high frequency bypass capacitors (ceramic or tantalum) will help avoid noise pickup or oscillation.

## GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce “hum” pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA606. To avoid leakage problems, it is recommended that the signal input lead of the OPA606 be wired to a Teflon® standoff. If the OPA606 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout.

A “guard” pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential (see Figure 3).

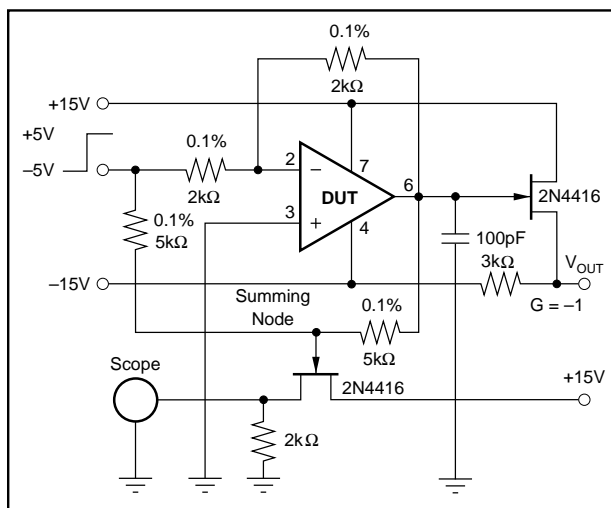


FIGURE 2. Settling Time Test Circuit.

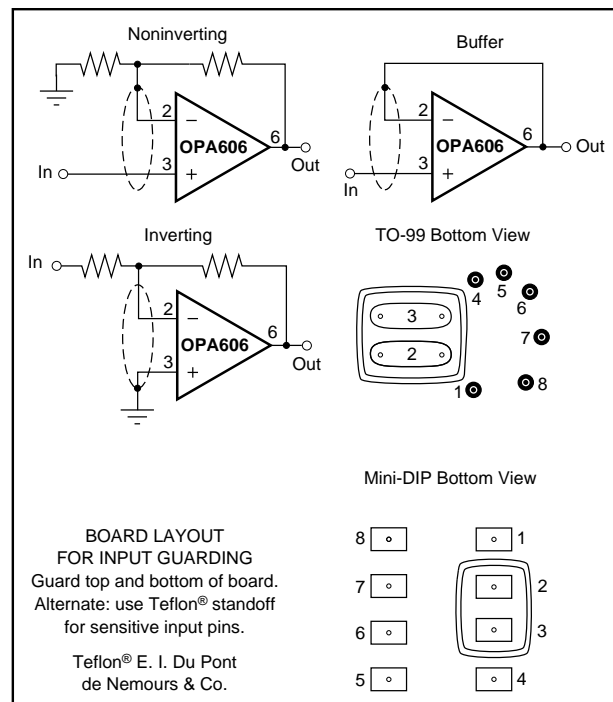


FIGURE 3. Connection of Input Guard.

## APPLICATIONS CIRCUITS

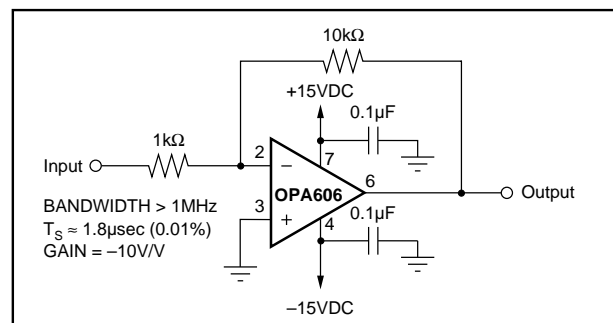


FIGURE 4. Inverting Amplifier.

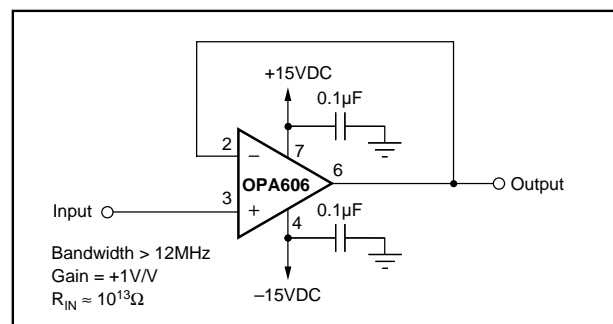


FIGURE 5. Noninverting Buffer.



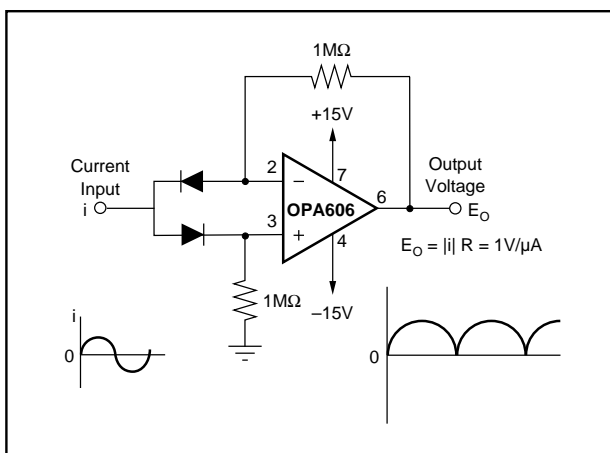


FIGURE 6. Absolute Value Current-to-Voltage Circuit.

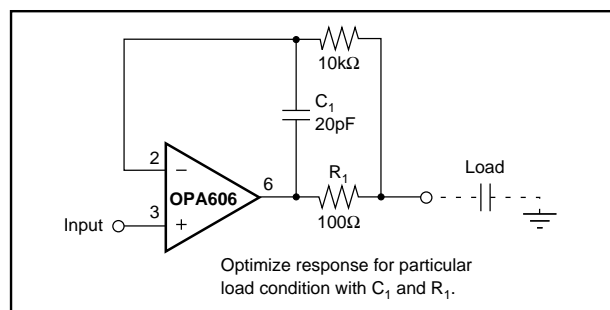


FIGURE 8. Isolating Load Capacitance from Buffer.

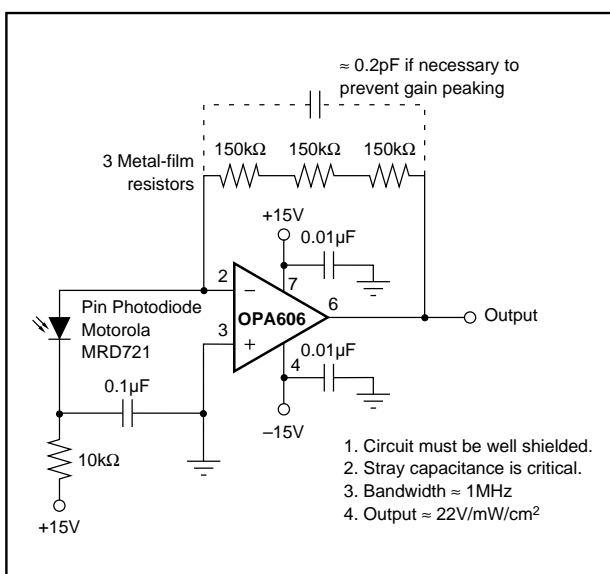


FIGURE 7. High-Speed Photodetector.

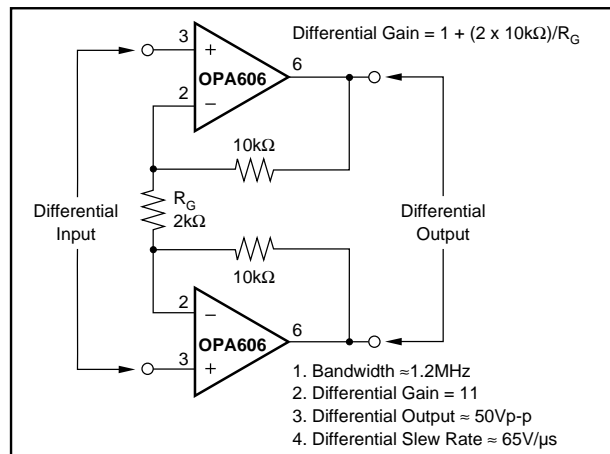


FIGURE 9. Differential Input/Differential Output Amplifier.

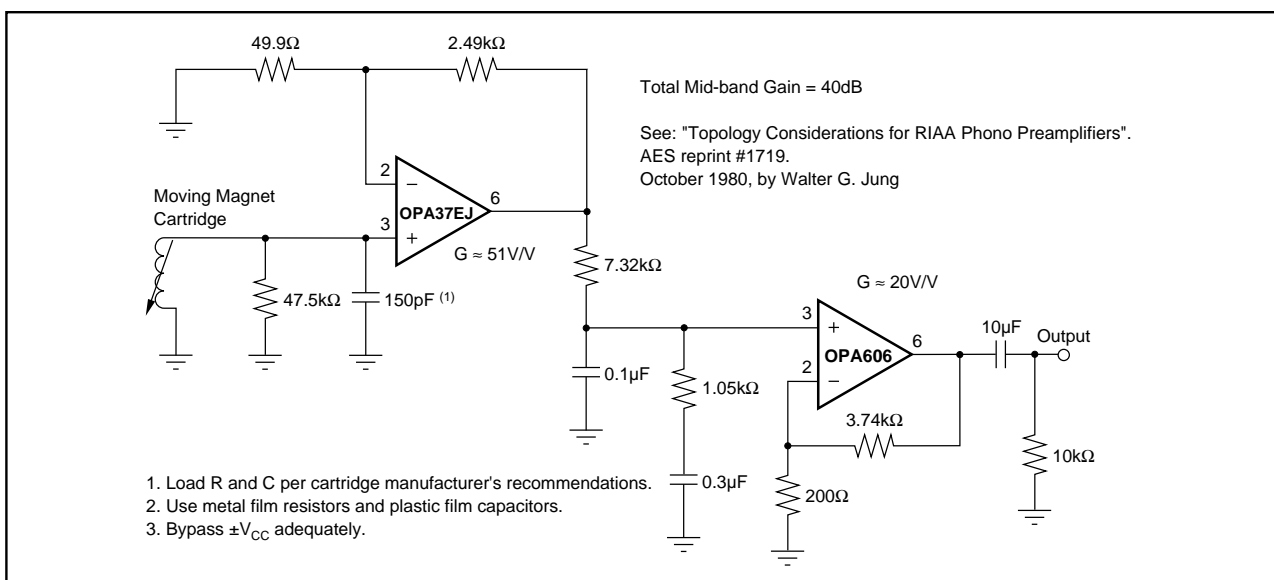


FIGURE 10. Low Noise/Low Distortion RIAA Preamplifier.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA606KP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA606KP	<a href="#">Samples</a>
OPA606KPG4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA606KP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

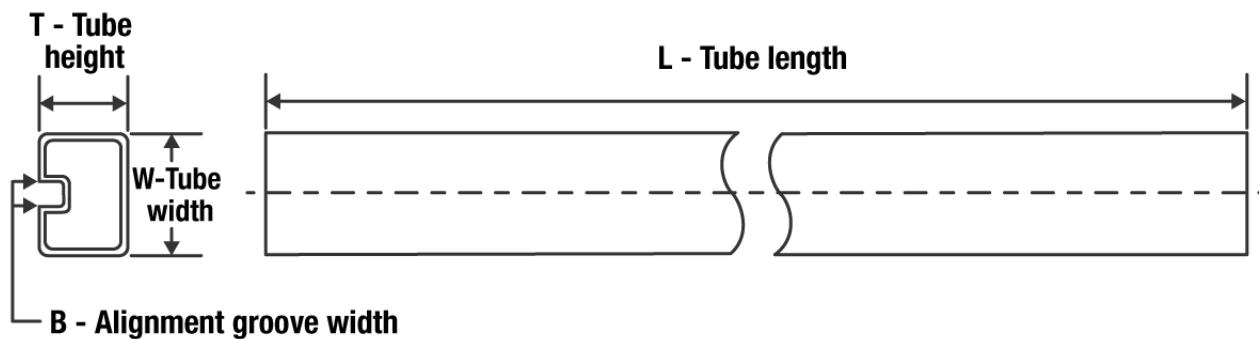
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA606KP	P	PDIP	8	50	506	13.97	11230	4.32
OPA606KPG4	P	PDIP	8	50	506	13.97	11230	4.32

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