NTNU
Kunnskap for en bedre verden

Department of Electronic Systems

TFE 4188 - Advanced Integrated Circuits

Assignment M2 - Group 5

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1 Introduction

For this milestone, the goal is to create a circuit design that implements the functionality of converting current to time. The design utilizes the Skywater Open Source PDK and its SKY130 process node.

This report serves as preliminary documentation of the current progress of the project.

2 Key Parameters

The following table presents the key parameters for the design.

Table 1: Key parameters

Name	Description	Min	Typ	Max	Unit
Width	Maximum width	-	-	160	μm
Height	Maximum height	-	-	100	μm
VDD	Input supply	1.62	1.80	1.98	V
Temperature	Temperature range to measure	-40	-	125	$^{\circ}C$
Current	Input current	-	120	200	μA

3 Specification

The following table presents the specifications for the design.

Table 2: Specifications

Name	Description	Min	Typ	Max	Unit	Notes
Accuracy	One-point accuracy	-5	0	+5	$^{\circ}C$	-
Resolution	Temperature resolution	-	-	-	$^{\circ}C$	TBD
Stability	-	-	-	-	-	TBD
Power consumption	-	-	-	-	W	TBD
Noise	Noise of the OTA	-	-	-	$V/\sqrt{HzS}$	TBD
Offset	Offset of the OTA	-	-	-	V	TBD
CMRR	CMRR of the OTA	-	-	-	dB	TBD
Gain	Gain of the OTA	-	-	-	-	TBD

4 Verification Plan

4.1 Functionality

The functionality of the current-to-time design will be verified by simulating the design in the entire temperature range. The simulation results will be analyzed to verify that the design produces a signal with variation in time with regard to the current.

5 Architecture

5.1 Integrator

The following figure presents the design of the simple integrator that was implemented:

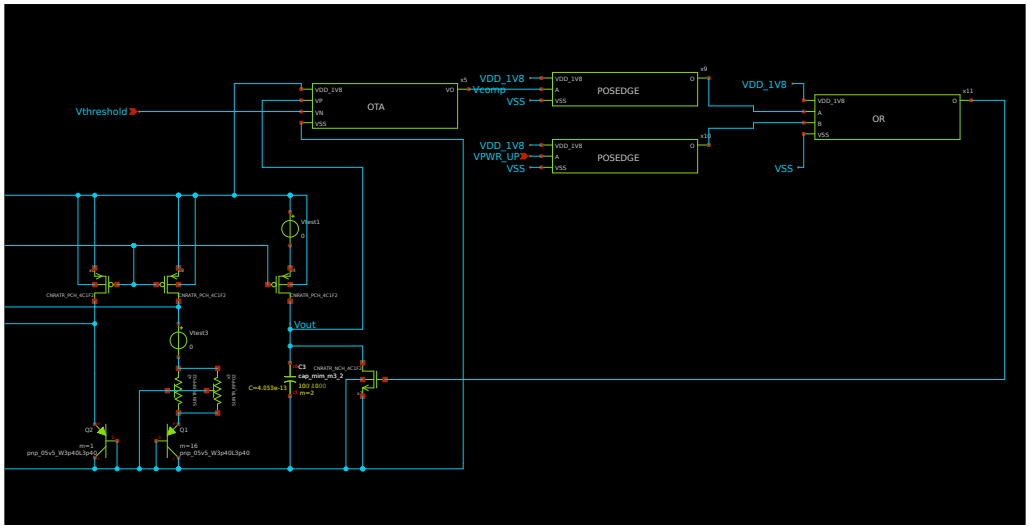

Figure 1: Integrator circuit design

The circuit works by charging up the capacitor during the on-cycle. A reset signal is applied to the gate of the NMOS to reset and drain the capacitor periodically. The output voltage is fed to a comparator, comparing it to a fixed threshold voltage of 0.9 V. The rate of the output voltage increase is dependent on the current, making it possible to convert the PTAT current to a time value by measuring the time it takes for the output of the comparator to go high.

5.2 Reset Circuit

The reset circuit works by generating a pulse as a result of the delay introduced by the three cascaded inverters. A separate pulse generator is used to initialize the reset circuit by taking a power-up pulse as the input, which goes high one ns after VDD goes high.

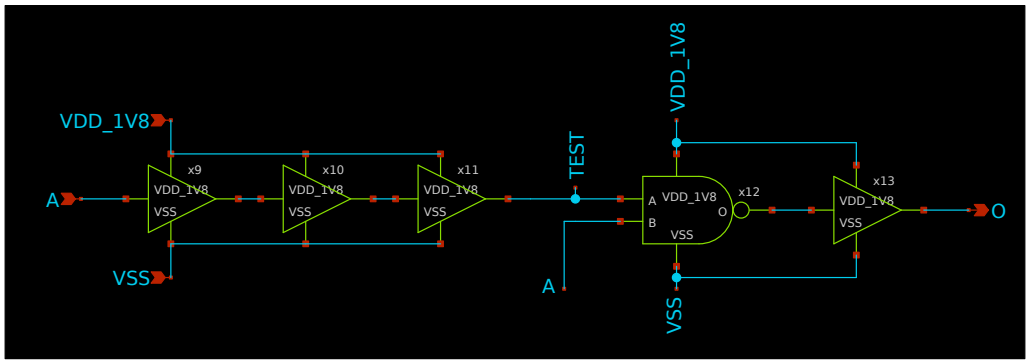

Figure 2: POSEDGE pulse generator circuit design

6 SPICE Simulations

All simulations presented in this section were performed in the typical corner. Figure 3 and Figure 4 present the simulation results for the initial MVP revision of the circuit, using a capacitor of 0.4 pF and a current of approximately 30 μA. Table 3 and Figure 5 shows the results of the revised design with a capacitor of 80 pF and a current of 5 μA.

6.1 Simulation of Output Voltages

The following figures present the simulation results of the proposed design. The simulations were performed by configuring a temperature step from -40 °C to 125 °C using the following SPICE commands:

```
optran 1 1 1 100p 2n 0

write

foreach vtemp -40 -20 0 20 40 80 125
  option temp=$vtemp
  tran 10p 1000n 10p
  write {cicname}_($vtemp).raw
  end

quit
```

The graph displays plots of the output voltages for the on-cycle of different temperatures:

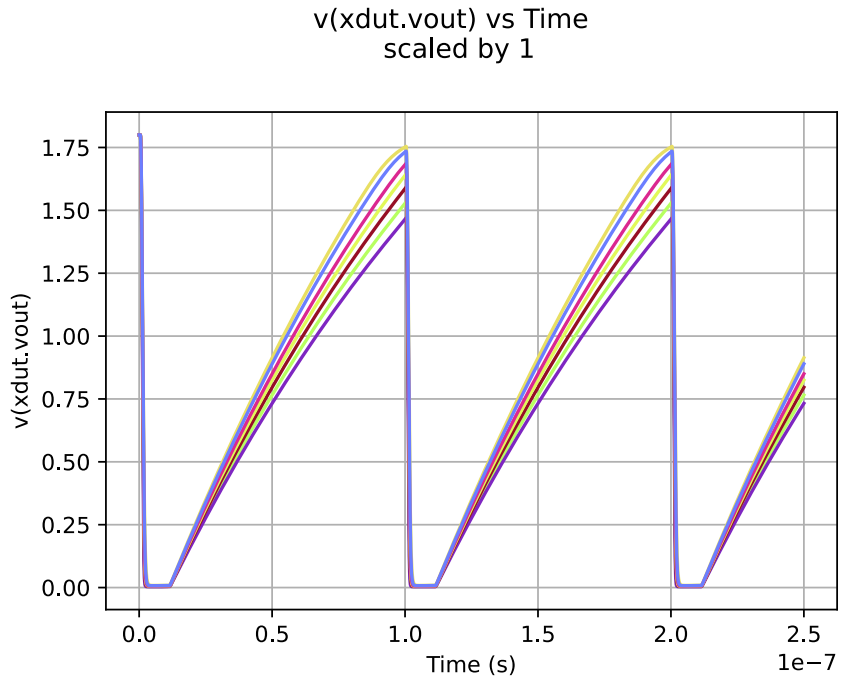

Figure 3: Simulation of output voltages from -40 °C to 125 °C

One can observe that the slope is steeper for higher temperatures.

6.2 Simulation of Comparator Output Voltages

The following graph displays the output of the comparator for different temperatures.

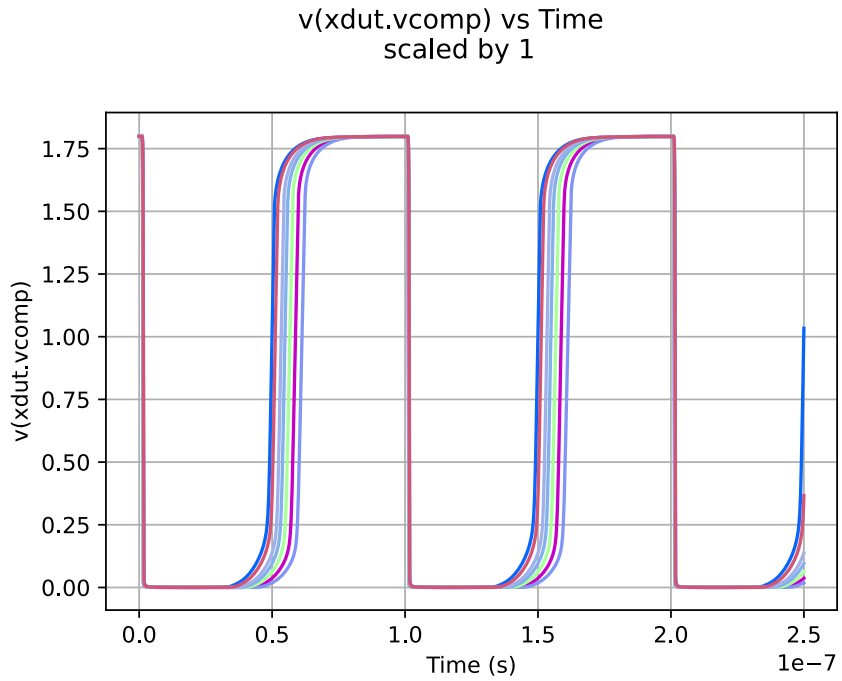

Figure 4: Simulation of comparator output voltages from -40 °C to 125 °C

One can observe that the rising edge occurs at different times depending on the temperature.

The difference in time between -40°C and 125°C is approximately 12.5 ns. To get a measurement resolution of 1°C for the entire temperature range, one would need a clock of approximately 13.2 GHz.

By increasing the size of the capacitor to 80 pF and decreasing the current to 5 μA, the time was increased to 11.4 μs, resulting in a required clock frequency of 14.5 MHz, which is well within the maximum clock of 40 MHz supported by Skywater. The following table shows the period between each rising edge of the comparator output for different temperatures with the improved design:

Table 3: Comparator time periods for varying temperatures

Temperature (°C)	-40	-20	0	20	40	60	80	100	125
Time period (μS)	27.798	29.208	30.543	31.809	33.030	34.274	35.605	37.107	39.199

This data was measured using the following ngspice commands:

```
foreach vtemp -40 -20 0 20 40 60 80 100 125
  option temp=$vtemp
  tran 10n 100u 1n uic
  write {cicname}_($vtemp).raw
  .measure tran tdiff TRIG v(xdut.vcomp) VAL=1.0 RISE=1
    TARG v(xdut.vcomp) VAL=1.0 RISE=2
end
```

The following graph shows a plot of the values from Table 3 in addition to a linear graph obtained by running a linear regression analysis of the data set:

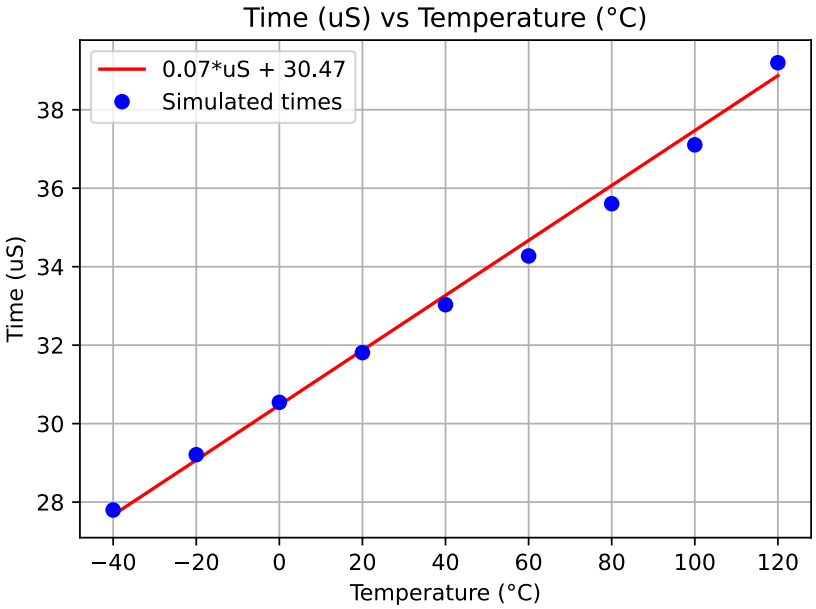

Figure 5: Comparator time periods for varying temperatures

7 Discussion

The group will continue to improve the design in the coming weeks. Since the improved design results in a required clock of only 14.5 MHz for a measurement resolution of 1°C, the group will consider reducing the size of the capacitor, which can be considered inappropriately large with its current value of 80 pF.

The current threshold voltage of 0.9 V was chosen arbitrarily and is currently forced. For the final design, this voltage could, for example, be implemented with a simple resistor divider driven by VDD. The group will experiment with different threshold voltage values in an attempt to further improve the design.