Design and Implementation of an Integrated BJT-based CMOS 8-Bit Temperature Sensor

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***Abstract*—This paper presents the theoretical foundations, the schematic design and the simulation results of an integrated bandgap-reference temperature sensor featuring a digital 8-bit interface. We use diode-connected BJTs to generate a temperature-dependent current and convert this current into a digital modulation by charging a capacitor and tracking the time until the capacitor voltage reaches a stable reference. Then we count the number of charge cycles for a specified time frame, which results in a truly digital output.**

***Index Terms*—Integrated Circuit, CMOS, Bandgap-Reference, Temperature Sensor**

I. Motivation

Most electric components show a strong temperature dependency in their characteristic behaviour. As a result, electric sensors for quantities such as magnetic fields, stress or pressure lack temperature invariance and the need for temperature compensation arises. For this correction, it is necessary to measure the temperature itself. This paper builds on previous work by Huang et al. [1], where the authors present a BJT-based CMOS temperature sensor featuring a duty-cycle modulated (DCM) output. Therefore, they implement a bandgap-based circuit that generates a proportional to absolute temperature (PTAT) current. By feeding this current into a capacitor and comparing the capacitor voltage with a reference, it is possible to convert the temperature-dependent current into a DCM signal. We modify the modulation scheme and present an approach for generating a truly digital output. The paper is organized as follows: We begin with a brief introduction to bandgap-reference design and show the top-level design of our temperature sensor. Next, we present the implementation and characterization of the individual circuit blocks, namely an operational transconductance amplifier (OTA) and a comparator based on Razavi's strongARM latch. This is followed by evaluating the individual circuits and the overall sensor performance. Finally, we sketch guidelines for future work and draw a conclusion.

II. Theoretical Foundations and Top Level Design of the Temperature Sensor

The concept is creating a temperature-dependent current and converting this current into a time period. Next, the DCM will be converted into a truly digital output on chip. Alternatively, the pulses can be decoded directly using high-speed input pins of a microcontroller.

A. Generating a Current that depends on Temperature

We start with the approach presented in 1. The key to generating a temperature-dependent current is the diode equation

$$I = A_{eff} \cdot J_S \cdot \left(e^{\frac{qV}{nk_BT}} - 1 \right) \tag{1}$$

which relates the current flowing through a diode to an applied voltage *V*, and effective width A_eff and the present temperature *T*. The factors J_s, *n*, *q* and k_b are the (normalized) saturation current density, the ideality factor of the diode, the elementary charge and the Boltzmann constant, respectively.

Neglecting the constant term (saturation current) $I_s = -A_{eff} \cdot J_s$ and solving (1) for the voltage yields

$$V = \frac{k_B T}{q} \ln\left(\frac{I}{A_{eff} \cdot J_S} \right) \tag{2}$$

Equation 2 appears very linear, however, the saturation current density J_s is also dependent on temperature. To mitigate this effect, we change from one diode to the voltage difference across two diodes placed in parallel, both conducting the same current but with a ratio of *N* for the effective areas. Using the isomorphism properties of the logarithm leads to a PTAT current:

$$\Delta U = \frac{k_B T}{q} \ln(N) = U_T \ln(N) \tag{3}$$

In the project, the diodes will be diode-connected bipolar junction transistors (BJTs).

From a technical perspective, the critical task is regulating the current passing the diodes. To be precise, the currents don't have to be equal but must have a constant ratio over the entire temperature range. We will come back to that later.

Suppose a resistor is placed in series with the larger diode, and the inputs of the two branches "big diode + resistor" and "small diode" are magically forced to be equal. In that case, the current only depends on the difference in base-collector voltages (similar to (3)) and thus has a linear temperature dependence, as desired. An OTA together with a feedback loop can be used for this purpose, as it will always try to generate an

input voltage of 0. The output of the OTA (see chapter III-A) drives a common-source stage whose output current is then mirrored to the two diode branches. The principal structure of the design is shown in Figure 1:

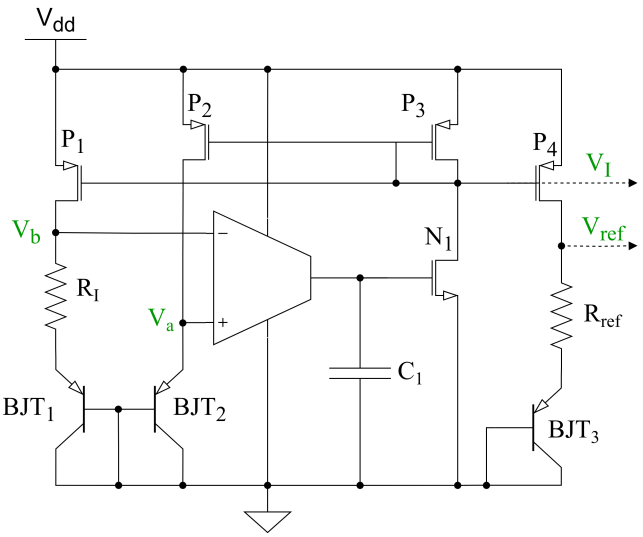

Fig. 1: Bandgap reference design.

Since the current flowing in the diodes is sourced from a common current mirror, the generated temperature-dependent current can be copied from the same current mirror for further signal processing.

For instance, this current is mirrored into a series connection of a resistor and another BJT. This branch shows a complementary to absolute temperature (CTAT) behavior, thus effectively canceling the PTAT characteristic of the mirrored current. This results in a temperature-stable reference voltage V_{ref}, see Figure 1.

B. Converting a Current into a Time Period

The current flowing in or out of a capacitance is related to the voltage across the two terminals as follows:

$$i_c(t) = C \cdot \frac{du_c(t)}{dt}. \tag{4}$$

In case of a constant current *I*, the voltage across the capacitor is now linearly increasing in time:

$$u_c(t) = u_c(t) + C \cdot I \cdot t. \tag{5}$$

Referring to [1], the current I is a mirrored version of the feedback current provided from the OTA, as described in section II-A.

Regarding design considerations, the elementary tradeoffs are shown in equation (5). On one hand, we favour large currents which improve the signal-to-noise ratio (SNR) and also increase the spacing between the currents at lower and higher temperatures. On the other hand, the maximum capacitance on-chip is limited, and thus large currents lead to lower charging times. Since we use a clocked comparator (see chapter III-B), the resolution in time is bounded by a maximum clock. In addition, the average power consumption per conversion cycle is linearly increasing with the capacitance, following the energy in a capacitor, which is given as

$$W_C = \frac{1}{2} C U^2. \tag{6}$$

We chose the capacitance to be as large as possible but within the approximate area of the feedback circuit, based on the best SNR and resolution objective. Excluding parasitic effects, the capacitance is set to be $1.29\,\mathrm{pF}$.

The linear charging model does not hold close to the supply voltage. In addition, the supply voltage itself is often not stable in practice. Thus, the reference voltage presented in chapter II-A serves as a reliable threshold for defining the capacitor to be fully charged. Detecting the moment when the capacitor voltage meets the reference voltage is the task of the comparator. We make use of a strongARM latch as described in chapter III-B, which was proposed originally by [2]. The top level design transducing the temperature-dependent current into a time period is shown below in Figure 2. The implementation of the comparator, the counter and the interface is presented in the following chapters.

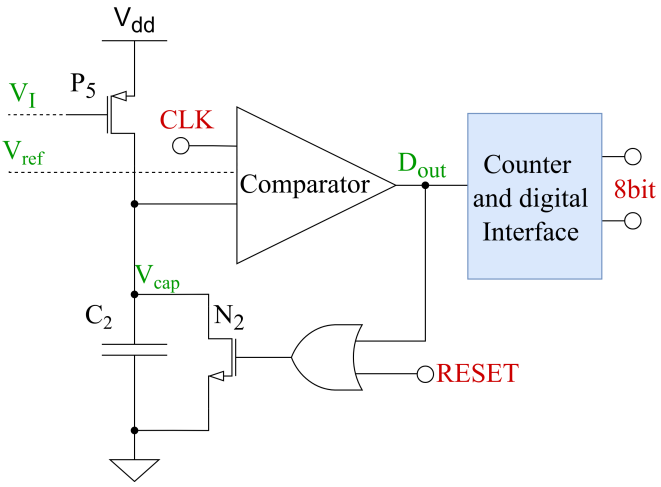

Fig. 2: Transducing a current into a time period.

III. Circuit Implementation of Block Structure Elements

A. Current Mirror OTA Design

The OTA is used in a negative feedback configuration to force a vanishing differential input voltage. This fundamental concept of OTAs ensures that the two voltage nodes V_a and V_b in Figure 1 are equal, see chapter II for details.

Our OTA consists of a differential pair followed by a current-mirror stage. As the sensor requires a single-ended feedback current, the internal currents of the inverting and non-inverting branch are added on the drain of P_3 and N_3, respectively. Since both inputs of the OTA are related to a diode voltage, the voltage values are close to the threshold

voltage of the NMOS. Thus, PMOSes are used for the input pair. The circuit is shown in Figure 3:

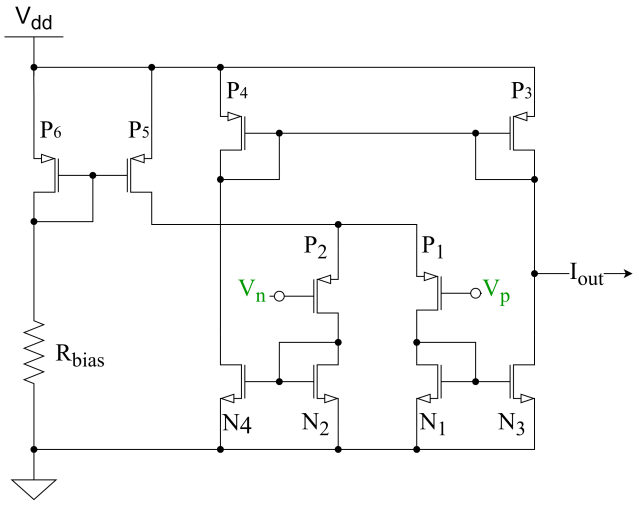

Fig. 3: OTA circuit implementation.

We make use of a resistor to generate a local bias current which is mirrored into the differential pair. The bias current is set around $5\,\mu A$. We considered reducing static power consumption while ensuring that the OTA inputs still show a minimal differential voltage, confirming the OTA is still able to regulate properly.

B. Comparator based on the strongARM latch

This paper makes use of the StrongARM latch proposed by Behzad Razavi [2]. The latch is based on a precharge-evaluate principle. Assuming a low *CLK* level, the circuit is disconnected from *GND* and the capacitances on the nodes *P*, *Q*, *X* and *Y* are charged to *VDD*. If the *CLK* rises to *VDD*, the evaluation starts with N_1 connecting the circuit back to *GND*. Next, the two transistors N_2 and N_3 conduct different amounts of current dependent on their gate-source voltage, which are defined by the differential input. As a result, the nodes *P* and *Q* discharge at different speeds. This effect is further enhanced by the cross-coupling between the gates and drains of N_4 and N_5, see Figure 4.

The strongARM latch was chosen for its zero static power consumption, intrinsic rail-to-rail output capability, and, most importantly, its high sensitivity, enabling rapid decision making [2]. Drawbacks resulting from the clocked nature of the strongARM latch will be discussed in the results section IV.

Our circuit implementation of the strongARM latch is shown below in Figure 4. In the top-level design (Figure 2), the two inputs V_p and V_n are hooked to the reference voltage and the capacitor voltage, respectively:

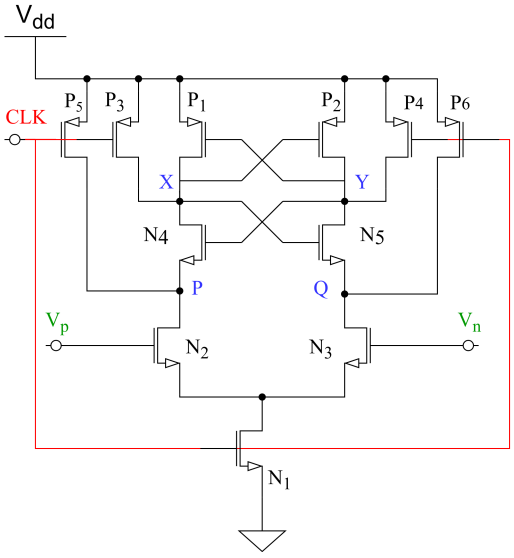

Fig. 4: StrongARM latch circuit.

After the latch has made the decision, the two output nodes X and Y are opposite, and the voltage at the *HIGH* output is restored to VDD by P_1 or P_2, respectively. For noise reasons and buffering, the nodes *P*, *Q*, *X* and *Y* are equipped with additional filter capacitors. Since the output of the strongARM latch is only valid during half of the clock cycle, an RS-latch is used as a buffer, see Figure 5.

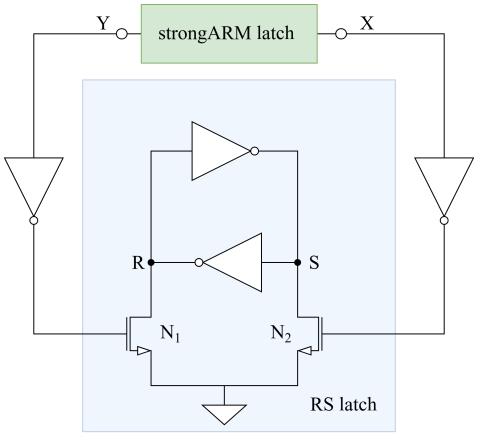

Fig. 5: RS-latch as digital output buffer.

The inverters are needed as the strongSRM latch has a (XY)=(11) output during the precharge phase, which is a prohibited input for the RS-latch [3].

C. Digital Logic and Sensor Interface

We aim for a design that generates a full-range linear digital output for the temperatures from $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$ and that does not require further signal processing after readout. Here, the straightforward solution of counting the number of required *CLK* cycles for charging the capacitor comes along with two problems:

1) Rearranging equation (5) states that the charging time shows an antiproportional relation to temperature ($\propto \frac{1}{T}$).
2) We observe a non-zero current at the lowest temperature of interest ($-40\,^{\circ}\mathrm{C}$). This offset does not arise from the malfunction of any sub-circuit, but from the bandgap-reference design itself, as indicated by equation (3).

In order to solve the two issues, we propose an inverse problem: How often can we charge the capacitor in a specified time?

Therefore, we connect the output of the comparator to the discharge transistor. To mitigate the issue of non-zero current I_{min} at the minimum temperature ($-40\,^{\circ}\mathrm{C}$), we taylor the current at maximum temperature ($125\,^{\circ}\mathrm{C}$) I_{max} to be (almost) twice as large as I_{min}: $I_{max} \triangleq 2 \cdot I_{min}$.

If we run the counter for the time period that is required to trigger an overflow at I_{min}, i.e. 256 recharge cycles, we obtain a linear full-range digital representation of the temperature, as desired. In practice, it will be necessary to introduce a margin, namely $I_{max} < 2 \cdot I_{min}$, and a slightly increased counting time to ensure that the current I_{min} reliably triggers a counter overflow.

The state machine of the digital logic is shown in Figure 6:

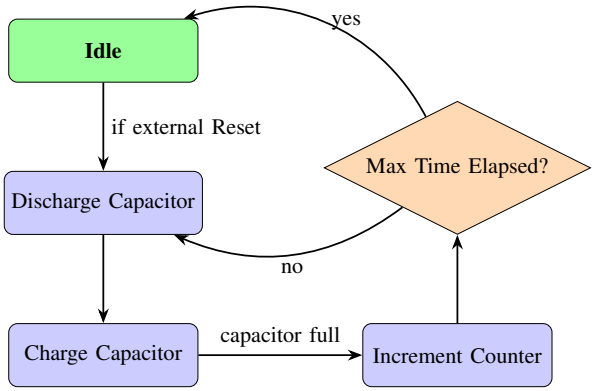

Fig. 6: State diagram of the digital logic.

The sensor has been designed for the following supply parameters and interface pins:

Input/Output	Description	Pin Labeling	Value
Input	Positive Supply Voltage	VDD	1.8 V
Input	Negative Supply Voltage	VSS	0 V
Input	Clock Signal	CLK	50 MHz
Input	Reset (active-high)	RESET	–
Output	Digital Output	D7...D0	–

TABLE I: Interface specifications.

IV. Results

A. OTA Analysis

Whenever amplifiers are used in feedback configuration, it is essential to ensure loop stability, especially if a 2nd stage amplifier is used as in this design, which has the potential to reach instability [4]. Therefore, a loop stability analysis is performed, and the results are given in Table II:

Parameter	typical	min	max	Unit
3 dB Bandwidth	172.99	100.88	280.37	kHz
Gain Margin	−16.05	−13.47	−18.40	dB
Low-Frequency/DC Gain	40.15	39.65	40.52	dB
Phase Margin	67.25	58.79	74.00	Degree
Unity Gain Frequency	17.25	9.62	27.97	MHz
Input Referred Offset	0.93	0.33	2.67	mV

TABLE II: Results of the OTA stability analysis.

As the mean values are reasonably close to the results obtained from a *typical* simulation, the following paragraph refers only to the results obtained from the latter.

Most importantly, the OTA is stable, indicated by a phase margin of $67.247°$ and a gain margin of $-16.051\,\mathrm{dB}$, i.e. the loop gain is only effective within the negative feedback domain. Our design meets the typical $40\,\mathrm{dB}$ DC gain for two-stage amplifiers. Further, the parameters show a $3\,\mathrm{dB}$ bandwidth of $172.99\,\mathrm{kHz}$ and a unity gain frequency of $17.249\,\mathrm{MHz}$. Since temperature increases or decreases for most physical systems with a (compared to the OTA parameters) large time constant, we see no need for adapting the amplifier design. Note that also each minimum value ensures stability.

B. Comparator Evaluation

The comparator plays a crucial role within the signal processing chain, since its capability to differentiate signals between $0\,\mathrm{V}$ to $1.2\,\mathrm{V}$ defines what smallest amount of temperature-dependent current our circuit can distinguish and thus contributes significantly to the sensor resolution.

We therefore analyze the comparator in a transient simulation where we keep one input tied to $0.9\,\mathrm{V}$ and have the other rising slowly from $0.89\,\mathrm{V}$ to $0.91\,\mathrm{V}$ over a time span of $10\,\mathrm{us}$ with a clock period of $20\,\mathrm{ns}$. The comparator was still able to detect a change in the differential input of $0.15\,\mathrm{mV}$.

In simulations together with the other implemented circuits, we unfavourably observe clock-feedthrough. This occurs as a ripple on both inputs, namely the reference voltage and the capacitor voltage, as seen in Figure 7. We also notice that even if the clock is run at a maximum available clock of $50\,\mathrm{MHz}$, the voltage across the capacitor rises significantly during a single clock period.

The delay between the change of the comparator output V_{comp} and the capacitor voltage V_{cap} exceeding the reference V_{ref} is indicated by the red fill in the lower plot of Figure 7. After estimating the average of V_{ref} (green line), we still suggest that the comparator is off by one clock period, which is close to the best case for a clocked comparator. As mentioned before, the noticeable change in input voltage difference within one clock period is high compared to the absolute levels, and thus lowers the effective resolution of our sensor.

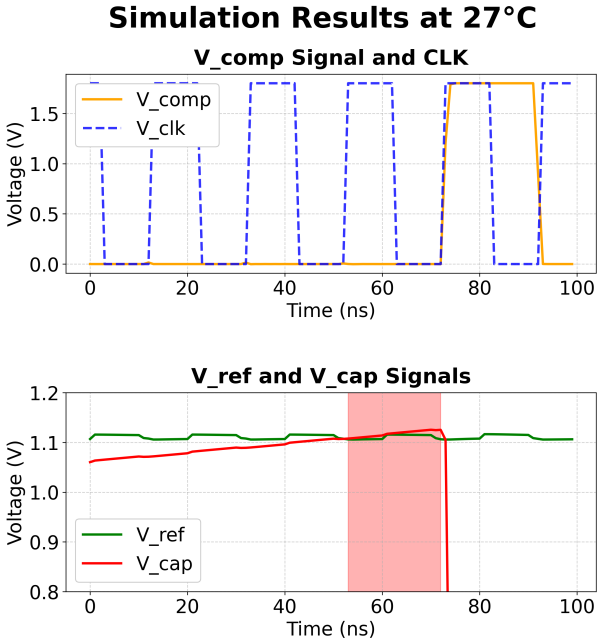

Fig. 7: Offset and delay of the comparator.

C. Temperature-to-Current Conversion

We aim for a linear rise in current on the range $-40\,^{\circ}\mathrm{C}$ to $125\,^{\circ}\mathrm{C}$, being a typical scenario in automotive and aerospace projects. Likewise, the reference voltage shall be invariant to temperature. Results obtained from a parametric temperature sweep in a transient simulation are shown below in Figure 8. We observe a current range of $0.57\,\mu\mathrm{A}$ to $1.06\,\mu\mathrm{A}$, for which the slope is slightly bending but still shows a characteristic close to being PTAT. Overall, this evaluates to a sensitivity of $2.69\,\mathrm{nA}/^{\circ}\mathrm{C}$. The reference voltage also shows a PTAT behaviour, with a swing of $15\,\mathrm{mV}$. Over the entire operation range, this leads to an error in the two least significant bits of the digital output, which calls for an improved design.

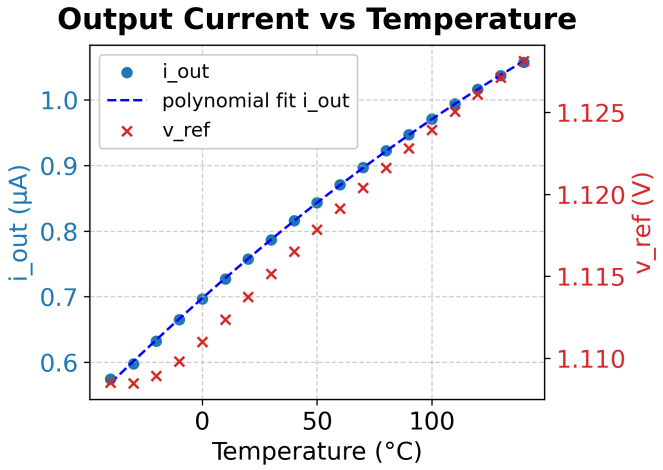

Fig. 8: Output current and voltage reference vs. temperature for a typical simulation.

The same simulation has been run for an extreme corner setup, and the results for the output current and the reference voltage are shown below in Figure 9 and Figure 10. The two problematic corners, with high and low temperature respectively, both show issues simulating slow NMOSes, slow PMOSes, and low supply voltage.

For the temperature-dependent current, we observe large variations in both, absolute values and slope in dependence of temperature. Therefore, we suggest trimming the two resistors, R_I and R_{ref}, based on lab measurement after fabrication.

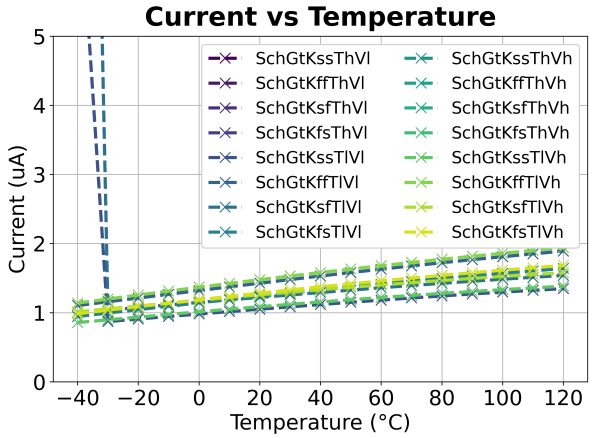

Fig. 9: Corner simulation results for the current-dependent current.

For the reference voltage, we observe noticeable variations in absolute values and minor deviations regarding the slope. We propose to tackle this also via trimming.

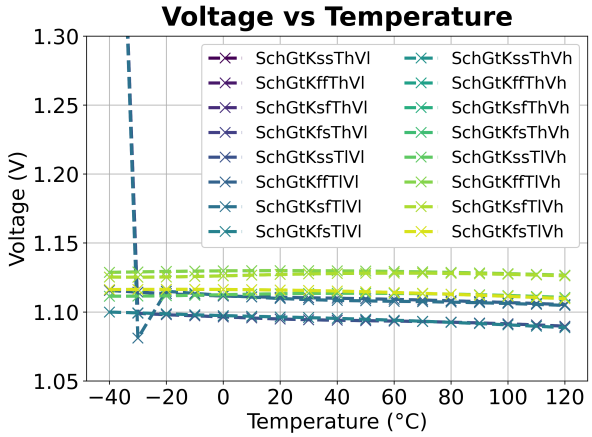

Fig. 10: Corner simulation results for the reference voltage.

In addition, Monte-Carlo simulations have been run to account for mismatch resulting from the IC fabrication process. These issues can be addressed by trimming as well.

D. PCM signal to Digital Conversion

We connect the output of the comparator to a digital module written in System Verilog to emulate the counter. The counting time is derived from the number of clock cycles required to trigger a counter overflow for the current at $-40\,^{\circ}\mathrm{C}$, thus mapping the digital output to 0 at this temperature. The scatter plot obtained from a transient simulation with a $5\,^{\circ}\mathrm{C}$ spacing can be seen below in Figure 11. We observe piecewise linearity, whereas there are significant steps, e.g. at $-10\,^{\circ}\mathrm{C}$.

In addition, we observe two temperatures, $90\,^{\circ}\mathrm{C}$ and $95\,^{\circ}\mathrm{C}$, being mapped to the same digital value. This may be due to insufficient high clock speed for the charging times at high currents, see problem description for Figure 7.

We also notice that the output at the maximum temperature of $125\,^{\circ}\mathrm{C}$ is not resulting in a digital output of 256, thus we do not use the full range of an 8-bit interface. This may be improved in a new design iteration by adapting the widths of the transistors in the feedback loop from the OTA to the currents in the BJTs.

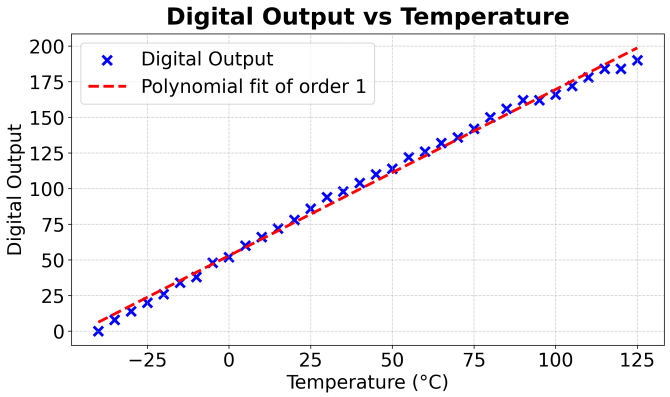

Fig. 11: Digital sensor output vs. temperature.

Given a conversion time of $650\,\mu\mathrm{s}$ and an average current draw of $60\,\mu\mathrm{A}$ from a $1.8\,\mathrm{V}$ supply, the energy used per conversion cycle evaluates to $70.2\,\mathrm{nJ}$. Note that the power consumption of the digital circuitry emulated by System Verilog is not included here. Hence, our design shows at least a 23,000-fold increase over the $2.98\,\mathrm{pJ}$ reported in [5], highlighting the significant power draw. Numerous charge-discharge cycles of the capacitor contribute to the current consumption, as well as a non-optimized OTA design with respect to supply current. In addition, the authors have compensation circuitry on-chip which is already included in the evaluation.

V. Outlook on Future Work

The next task is generating the digital layout and combining it with the already existing analog design. Then, parasitic parameters need to be extracted and all simulations shown in the results section need to be run again. In addition, we recommend fine-tuning of the current-vs-temperature curve in terms of linearity and absolute range. The latter should ensure a digital output close to 0 and 256 for the lowest and highest temperature of interest, respectively. Likewise, the reference voltage needs to be more stabilized so the voltage swing does not introduce any error on an 8-bit referred resolution. Ideally, the need for trimming vanishes with a redesign as well. Regarding the interface, we also aim to generate a digital output buffer that features a serial interface such as SPI. Moreover, it may be feasible to reduce the clock rate, in which case the comparator may be replaced by a continuous time implementation to ensure fast detection of the capacitor voltage reaching the reference voltage. Lastly, the sensor needs to be equipped with ESD protection and power-up circuitry.

VI. Conclusion

In this paper, we present a temperature sensor concept based on a temperature-dependent current source, as described in [1]. This current charges a capacitor, and the capacitor voltage is compared to an on-chip reference voltage to generate a time-based measurement. The final 8-bit digital output is determined by counting the number of charge cycles within a fixed time window. While our results demonstrate the fundamental functionality of the circuit, we also identify several limitations, including energy efficiency, limited resolution, output non-linearity, and significant sensitivity to process variations. These issues show need for further optimization prior to a potential tapeout.

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