

Diagram illustrating the pinout for the **Conn_02x17_Odd_Even** connector, labeled **J1**.

The connector has 17 pins, numbered 1 through 17. The pins are organized into two columns: pins 1 through 17 on the left, and pins 18 through 34 on the right.

Pin 17 (Left Column): Labeled **Audio** and **2V5 Levels**. It is connected to **CLK0** and **GND** (via **100R/R0402**).

Pins 1 through 16 (Left Column): Labeled **Buttons** and **2V5 Levels**. They are connected to **+2V5** and **+1V8** (via **100R/R0402**).

Pins 18 through 34 (Right Column): Labeled **1V8 Levels LEDs**. They are connected to **+1V8** and **GND** (via **100R/R0402**).

Signal Connections:

- Pins 1 through 16 (Left Column):**
 - 1: **FPGA_SPL_FWD**
 - 3: **EA_A8**
 - 5: **EA_B8**
 - 7: **WB_A8**
 - 9: **WB_B8**
 - 11: **SB_B3**
 - 13: **SB_A3**
 - 15: **SB_B2**
 - 17: **SB_A2**
 - 19: **SB_B1**
 - 21: **SB_A1**
 - 23: **SB_B0**
 - 25: **SB_A0**
 - 27: **FPGA_RESET_IN**
 - 29: **CLK0**
 - 31: **R1131**
 - 33: **100R/R0402**
- Pins 18 through 34 (Right Column):**
 - 18: **WC_B3**
 - 20: **WC_A3**
 - 22: **WC_B2**
 - 24: **WC_A2**
 - 26: **WC_B1**
 - 28: **WC_A1**
 - 30: **WC_B0**
 - 32: **WC_A0**
 - 34: **SER_CLK_N**
 - 36: **SER_CLK_P**
 - 38: **SER_TX_P**
 - 40: **SER_TX_N**
 - 42: **SER_RX_N**
 - 44: **SER_RX_P**
 - 46: **33R112**
 - 48: **100R/R0402**
 - 50: **CLK3**

Power and Ground Connections:

- +2V5:** Connected to pins 1, 3, 5, 7, 9, 11, 13, 15, 17.
- +1V8:** Connected to pins 18, 20, 22, 24, 26, 28, 30, 32, 34.
- GND:** Connected to pins 16, 18, 20, 22, 24, 26, 28, 30, 32, 34.

The diagram illustrates an 8-bit LED display driver circuit. It consists of 8 LEDs (LED0 to LED7) connected to an 8-bit data bus (WC_A0 to WC_B3). Each LED is connected to a 1V8 supply through a 2.2K resistor (R0 to R7). The LEDs are connected to the data bus through a 2.2K resistor (R0 to R7). The data bus is labeled '1V8 Levels'.

[illegible]

The image contains three separate circuit diagrams, each representing a different IC pin configuration for decoupling:

- Diagram 1 (Left):** Shows a pin labeled **AUDIO_CPVDD** with a **+3V3A** supply. A **10uF** capacitor (C5) is connected between the pin and **GND**. A **100nF** capacitor (C6) is connected between the pin and the **+3V3A** supply.
- Diagram 2 (Middle):** Shows a pin labeled **AUDIO_3V3A** with a **+3V3A** supply. A **10uF** capacitor (C11) is connected between the pin and **GND**. A **100nF** capacitor (C14) is connected between the pin and the **+3V3A** supply.
- Diagram 3 (Right):** Shows a pin labeled **AUDIO_DVDD** with a **+3V3** supply. A **10uF** capacitor (C15) is connected between the pin and **GND**. A **100nF** capacitor (C16) is connected between the pin and the **+3V3** supply.

Below the diagrams, the text reads: "Decoupling capacitors. Place as close as possible to the affected IC pin."

The diagram illustrates the input stage of a 4-channel audio amplifier. It features four input channels, each with a 22R/R0402 input resistor (R9, R11, R13, R15) connected to a 10K/R0402 feedback resistor (R8, R10, R12, R14). The feedback resistors are connected to the non-inverting inputs of the op-amp buffers. The op-amp buffers are configured with a 100nF/10V/20%/X5R/C0402 capacitor in parallel with the feedback resistor. The output of each channel is connected to a 10K/R0402 resistor, which is then connected to a 22R/R0402 resistor, and finally to a 100nF/10V/20%/X5R/C0402 capacitor.

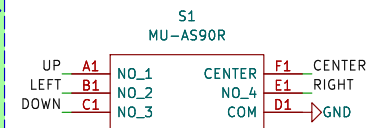
JACK pinout for SJ-43516-SMT-TR
<http://www.cui.com/product/resource/sj-4351x-smt-series.pdf>
 pin 1 - sleeve (GND)
 pin 2 - tip (left channel)
 pin 3 - ring1 (right channel)
 pin 4 - ring2 (video)
 pin 5 - tip switch
 pin 6 - ring1 switch

Line Out impedance: 470 Ohm.
 Typical Line In impedance (load): 1K to 10K Ohm.

Decoupling capacitors.
 Place as close as possible to the affected IC pin.

3-Wire I ² S audio source			
SCK	Low	MCLK from internal PLL	
FLT	Low	Normal filter latency	
FMT	Low	I ² S Audio data format	
DEMP	Low	44.1 Khz De-emphasis disabled	

In systems where XSMT is not required, it can be directly connected to AVDD.



CAP_JOY — CAP1

CAP_BTN — CAP2



H1
MountingHole

Up to 300-mA Output Current
1-MHz Fixed-Frequency PWM Operation

The diagram shows the TLV61225DC converter configured for 1-MHz fixed-frequency PWM operation. The input is +2V5, connected to the VIN pin (pin 1) through a 10µF capacitor (C27). The EN pin (pin 3) is connected to GND. The feedback pin (FB, pin 2) is connected to the output through a divider consisting of a 10K resistor (R20) and a 10µF capacitor (C28). The output is +3V3. The switching node (VOUT, pin 4) is connected to the output and has a 4.7µH inductor (L2) connected to the SW pin (pin 5). The SW pin is also connected to the SB pin (pin 6) through a 10K resistor (R20). The SB pin is connected to GND. The GND pins (pins 2, 3, 4, 5, 6) are all connected to a common GND.

The diagram shows a red rectangular component with four pins. The pins are labeled from top to bottom: I2S1_TX_WS, I2S1_TX_SDA, I2S1_TX_SCK, and AUDIO_MUTE. The I2S1_TX_WS pin is connected to a green line labeled SB_B1. The I2S1_TX_SDA pin is connected to a green line labeled SB_A1. The I2S1_TX_SCK pin is connected to a green line labeled SB_B0. The AUDIO_MUTE pin is connected to a green line labeled SB_A0. The AMP_EN pin is connected to a green line labeled SB_B2.

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