Olimex Extension ethIO v0.1

2024-12-09

Intergalaktik d.o.o.
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Year: 2024.

Change project informations under.
File>>Schamatic Setup>>Text Variables

!!
Olimex board is delivering MAX 2.5V on connector.
You can use 2.5V output signals for 3.3V.
Be carefull FPGA input only tolerate MAX 2.5V!
!!

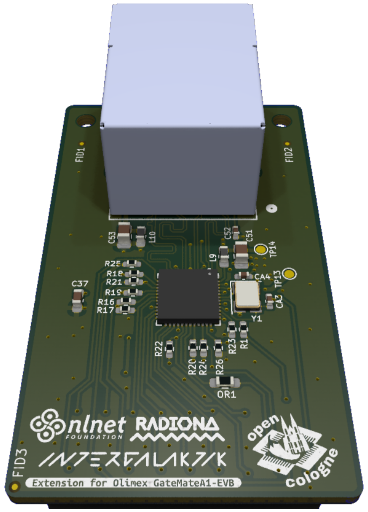
!!
VCC input is connected over 500mA resetable fuse!
Maximum current for VCC is set to 500mA.
It may be possible to drain more current but
you will need add different FUSE and use it at your own risk!
3.3V step up is limited to 400mA
Idea behind limits is that you can use all 3 extensions slots
at once without any risk od draining to much!
!!

A1 Dedicated clock input pins are:
IO_SB_A8: CLK0
IO_SB_A7: CLK1
IO_SB_A6: CLK2
IO_SB_A5: CLK3
You can use them all as differential inputs.

We are not able to use any on extension boards.

It is also possible to use any GPIO as a clock input.
The only thing to note here is that the signal must be
routed via the routing structure to the entry point
of the global clock mesh. These paths are longer than
via the dedicated clock pins, which is why it is
essential to pay attention to clock skew.

TOP VIEW



Dimension
File: dimension.kicad_sch

Main Sheet
File: main.kicad_sch

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Sheet: /
File: ethIO.kicad_sch
Title: Olimex Extension ethIO v0.1
Size: A4 | Date: 2024-12-02 | **Rev: v0.1**
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Main Page

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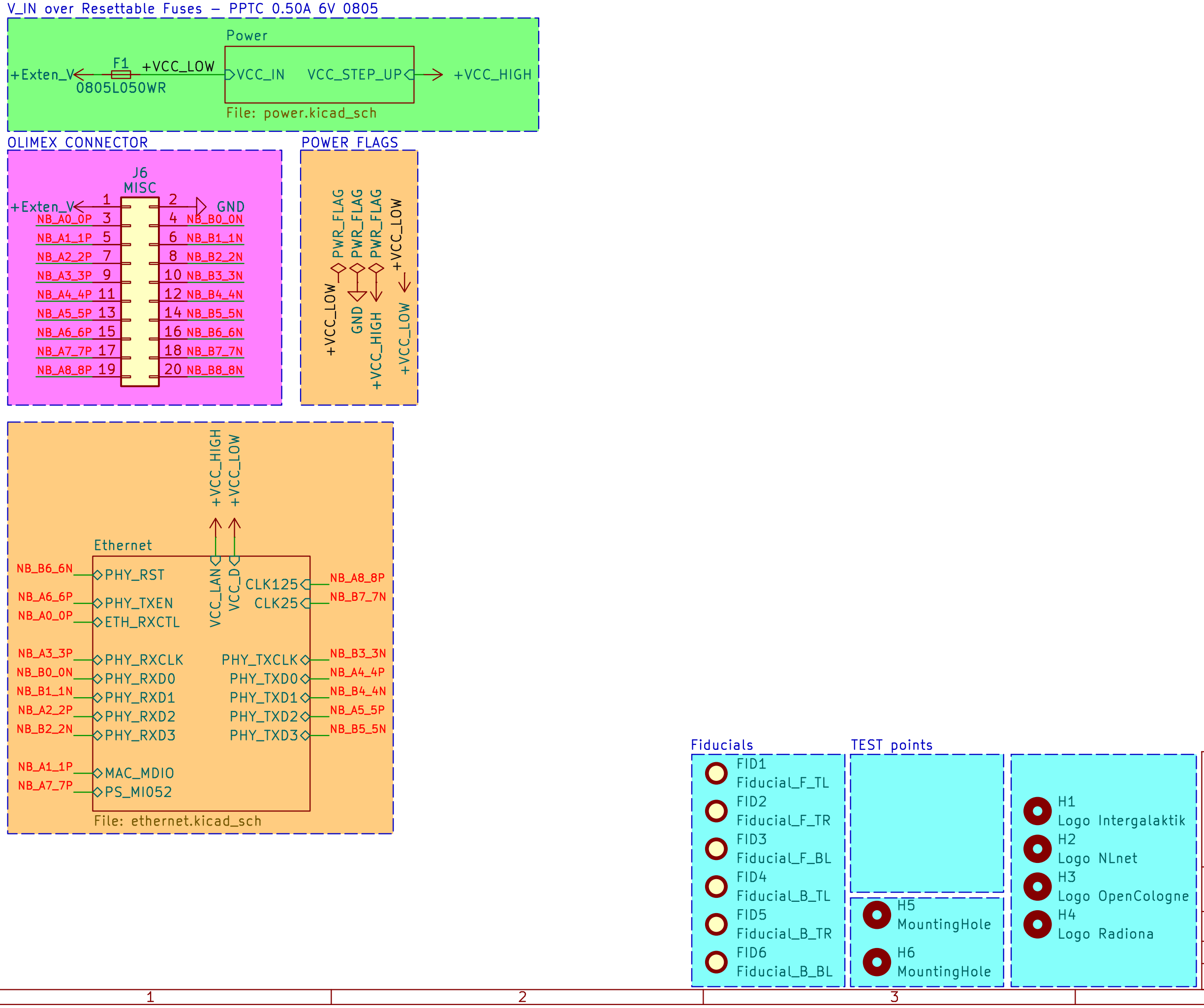
!!

!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
Set and Voltage on BANK 1.2V/1.8V/2.5V
STEP UP can boost any of those voltages
to 3.3V/5V depending on selected chip
!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!



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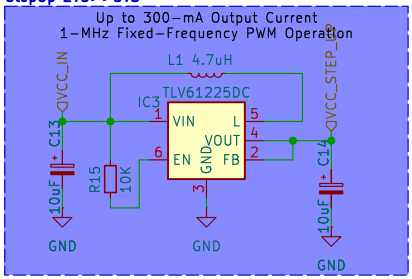
Power Page

StepUp 2V5>>3V3



Use TPS61225DC for 2.5V>>3.3V
Use TPS61222DC for 2.5V>>5V

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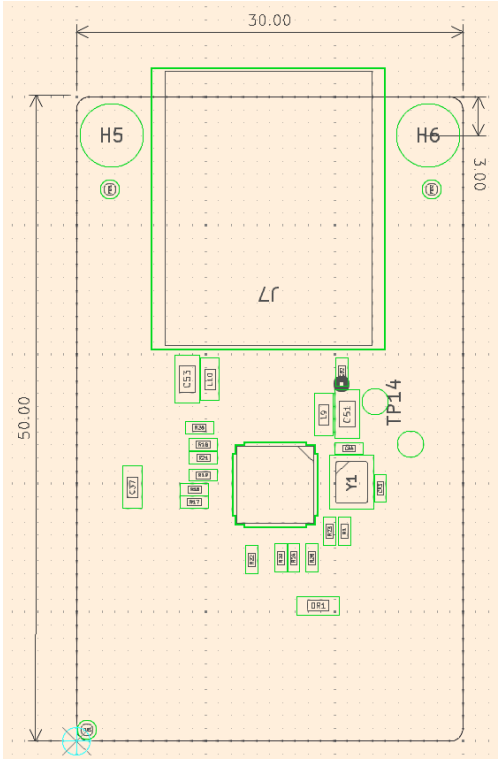
Dimension Page



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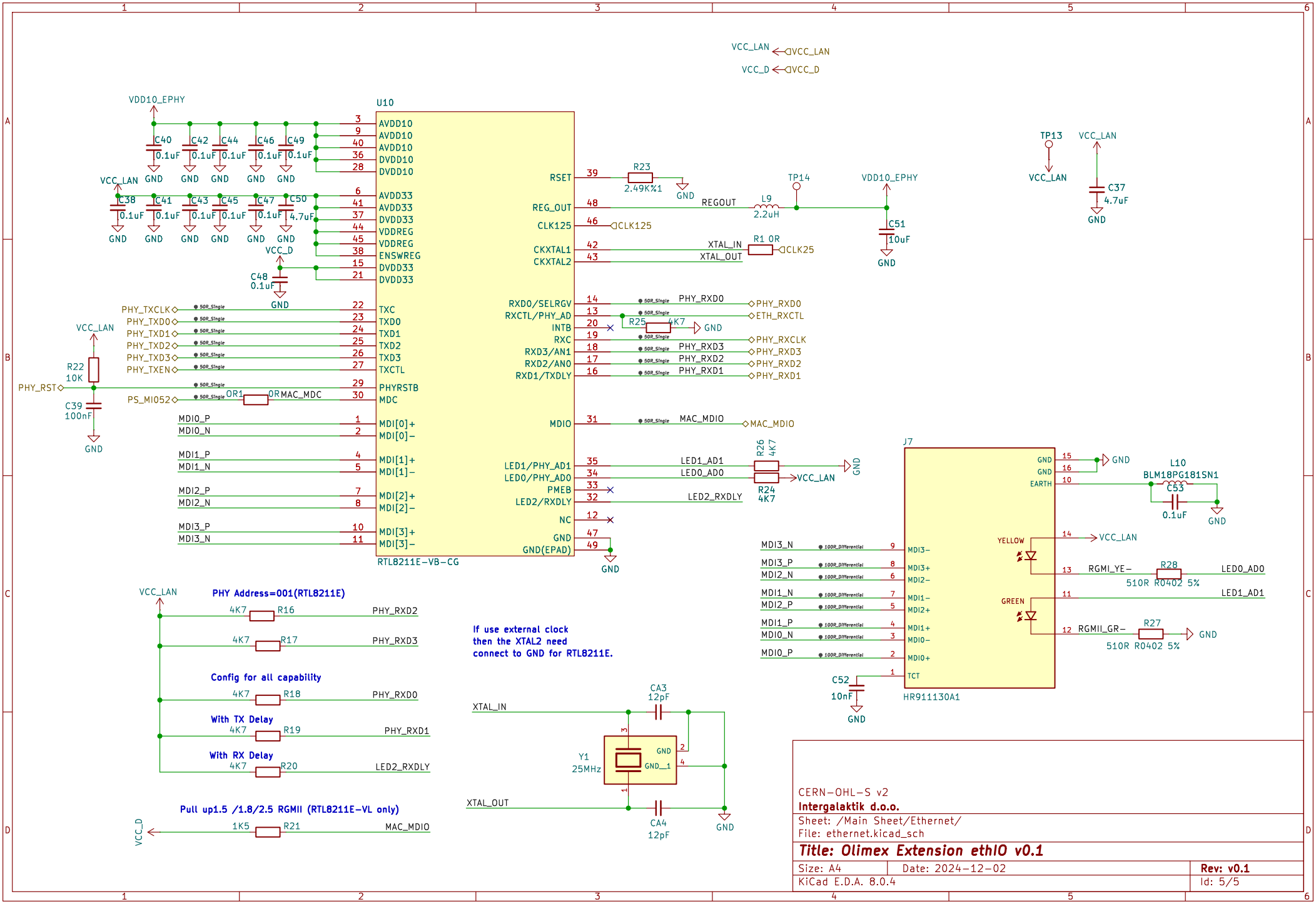
VCC_LAN
VCC_D
U10
RTL8211E-VB-CG
VDD10_EPHY
C40 0.1uF
C42 0.1uF
C44 0.1uF
C46 0.1uF
C49 0.1uF
C38 0.1uF
C41 0.1uF
C43 0.1uF
C45 0.1uF
C47 0.1uF
C50 4.7uF
C48 0.1uF
AVDD10
AVDD10
AVDD10
DVDD10
DVDD10
AVDD33
AVDD33
DVDD33
VDDREG
VDDREG
ENSWREG
DVDD33
DVDD33
RSET
R23 2.49K%1
REG_OUT
REGOUT
L9 2.2uH
TP14
C51 10uF
CLK125
CKXTAL1
CKXTAL2
XTAL_IN
XTAL_OUT
R1 0R
TP13
C37 4.7uF
PHY_TXCLK
PHY_TXD0
PHY_TXD1
PHY_TXD2
PHY_TXD3
PHY_TXEN
PHY_RST
PS_MI052
R22 10K
C39 100nF
OR1
0R
MAC_MDC
TXC
TXD0
TXD1
TXD2
TXD3
TXCTL
PHYRSTB
MDC
RXD0/SELRGV
RXCTL/PHY_AD
INTB
RXC
RXD3/AN1
RXD2/AN0
RXD1/TXDLY
PHY_RXD0
ETH_RXCTL
R25 4K7
PHY_RXCLK
PHY_RXD3
PHY_RXD2
PHY_RXD1
MDIO
MAC_MDIO
MDI0_P
MDI0_N
MDI1_P
MDI1_N
MDI2_P
MDI2_N
MDI3_P
MDI3_N
MDI[0]+
MDI[0]−
MDI[1]+
MDI[1]−
MDI[2]+
MDI[2]−
MDI[3]+
MDI[3]−
LED1/PHY_AD1
LED0/PHY_AD0
PMEB
LED2/RXDLY
LED1_AD1
LED0_AD0
LED2_RXDLY
R26 4K7
R24 4K7
NC
GND
GND(EPAD)
J7
HR911130A1
L10 BLM18PG181SN1
C53 0.1uF
EARTH
YELLOW
GREEN
R28 510R R0402 5%
R27 510R R0402 5%
RGMI_YE−
RGMII_GR−
C52 10nF
PHY Address=001(RTL8211E)
R16 4K7
R17 4K7
Config for all capability
R18 4K7
With TX Delay
R19 4K7
With RX Delay
R20 4K7
Pull up1.5 /1.8/2.5 RGMII (RTL8211E-VL only)
R21 1K5
If use external clock
then the XTAL2 need
connect to GND for RTL8211E.
CA3 12pF
CA4 12pF
Y1 25MHz
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