

J1
Conn_02x17_Odd_Even

Pin	Signal
1	FPGA_SPL_FWD
2	WC_B3
3	EA_A8
4	WC_A3
5	EA_B8
6	WC_B2
7	WB_A8
8	WC_A2
9	WB_B8
10	WC_B1
11	SB_B3
12	WC_A1
13	SB_A3
14	WC_B0
15	SB_B2
16	WC_A0
17	SB_A2
18	WC_B0
19	SB_A1
20	SER_CLK_N
21	SB_A0
22	SER_CLK_P
23	SER_TX_P
24	SER_TX_N
25	SER_RX_N
26	SER_RX_P
27	FPGA_RESET_IN
28	CLK0
29	CLK3
30	GND
31	GND
32	GND
33	GND
34	GND
35	GND
36	GND
37	GND
38	GND
39	GND
40	GND
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	GND
49	GND
50	GND
51	GND
52	GND
53	GND
54	GND
55	GND
56	GND
57	GND
58	GND
59	GND
60	GND
61	GND
62	GND
63	GND
64	GND
65	GND
66	GND
67	GND
68	GND
69	GND
70	GND
71	GND
72	GND
73	GND
74	GND
75	GND
76	GND
77	GND
78	GND
79	GND
80	GND
81	GND
82	GND
83	GND
84	GND
85	GND
86	GND
87	GND
88	GND
89	GND
90	GND
91	GND
92	GND
93	GND
94	GND
95	GND
96	GND
97	GND
98	GND
99	GND
100	GND

Diagram illustrating the connection of an 8-bit LED display driver. The circuit shows 8 LEDs (LED0 to LED7) connected to an 8-bit data bus. Each LED is connected to a data line through a 2.2K resistor. The LEDs are also connected to a common ground. The data lines are labeled WC_B3, WC_A3, WC_B2, WC_A2, WC_B1, WC_A1, WC_B0, and WC_A0. The LEDs are labeled LED7, LED6, LED5, LED4, LED3, LED2, LED1, and LED0. The resistors are labeled R0, R1, R2, R3, R4, R5, R6, and R7. The diagram is labeled "1V8 Levels" on the right side.

[illegible]

The image contains three separate circuit diagrams, each illustrating the placement of decoupling capacitors for a specific IC pin. Each diagram shows a power supply line (labeled +3V3A) connected to a pin (AUDIO_CPVDD, AUDIO_3V3A, and AUDIO_DVDD respectively). A 10uF capacitor (C5, C11, C15) is connected in parallel with a 100nF capacitor (C6, C14, C16) between the power supply line and ground (GND). The capacitors are represented by their standard electronic symbols.

Decoupling capacitors.
Place as close as possible to the affected IC pin.

The diagram illustrates the input stage of a 4-channel audio amplifier. It features four input channels, each with a 22R/R0402 input resistor (R9, R11, R13, R15) connected to a 10K/R0402 feedback resistor (R8, R10, R12, R14). The feedback resistors are connected to the non-inverting input of the op-amp and to a +2V5 supply. The inverting input of each op-amp is connected to ground through a 100nF/10V/20%/X5R/C0402 capacitor (C0, C1, C3, C2). The output of each op-amp is connected to a 10K/R0402 feedback resistor (R18, R25, R19, C26) and a 100nF/10V/20%/X5R/C0402 capacitor (C25, C26) connected to ground. The output of each op-amp is also connected to a 10K/R0402 feedback resistor, which is also connected to a +2V5 supply. The output of each op-amp is also connected to a 100nF/10V/20%/X5R/C0402 capacitor, which is connected to ground.

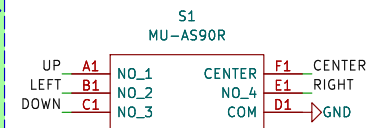
JACK pinout for SJ-43516-SMT-TR
<http://www.cui.com/product/resource/sj-4351x-smt-series.pdf>
 pin 1 - sleeve (GND)
 pin 2 - tip (left channel)
 pin 3 - ring1 (right channel)
 pin 4 - ring2 (video)
 pin 5 - tip switch
 pin 6 - ring1 switch

Line Out impedance: 470 Ohm.
 Typical Line In impedance (load): 1K to 10K Ohm.

Decoupling capacitors.
 Place as close as possible to the affected IC pin.

3-Wire I ² S audio source	
SCK	Low MCLK from internal PLL
FLT	Low Normal filter latency
FMT	Low I2S Audio data format
DEMP	Low 44.1 Khz De-emphasis disabled

In systems where XSMT is not required, it can be directly connected to AVDD.



CAP_JOY — CAP1

CAP_BTN — CAP2



H1
MountingHole

Up to 300-mA Output Current
1-MHz Fixed-Frequency PWM Operation

The diagram shows the TLV61225DC converter in a 1-MHz fixed-frequency PWM mode. The input is +2V5, connected to the VIN pin (pin 1) through a 10µF capacitor (C27). The EN pin (pin 3) is connected to GND. The feedback pin (FB, pin 2) is connected to the output through a voltage divider consisting of a 10K resistor (R20) and a 10µF capacitor (C28). The output is +3V3. The switching node is connected to the L pin (pin 5) through an inductor L2 (4.7µH). The GND pins (pins 4 and 6) are connected to GND. The SB, A2 pin (pin 6) is also connected to GND.

The diagram shows a set of five I2S1_TX signals connected to a set of five SB signals:

- I2S1_TX_WS is connected to SB_B1.
- I2S1_TX_SDA is connected to SB_A1.
- I2S1_TX_SCK is connected to SB_B0.
- AUDIO_MUTE is connected to SB_A0.
- AMP_EN is connected to SB_B2.

4

Id: 1/1