CMPE-530/630 Digital IC Design Project Rubric

Component	Description	Percentage
Design Methodology	Group has proposed a detailed design methodology (algorithm, architecture) and has justified decisions with analysis of tradeoffs between complexity, area, power, speed, etc.	30%
Functional Results and Analysis	Group proves that their design works by showing the qualitative (edges) and quantitative (accuracy) results of all test images for i.) MATLAB, ii.) pre-layout, and iii.) post-layout designs	25%
Timing, power, and area results/analysis	Group has analyzed the timing, power consumption, and area (post-layout only) of their design for i.) pre-layout and ii.) post-layout designs.	20%
Project Report	Group has documented their project using the lab report template.	25%

Demo checkoff:

Component	Comments	Checkoff
Detailed block diagram of design. Be prepared to discuss justifications for design choices such as • Handling of fixed-point • Architecture • Activation function implementation • Challenges • Optional design feature (grad students)		
Quickly discuss all HDL code, approach to making it generic, style (behavioral, structural, etc.), testbench, and any custom scripts.		
All functional results on test images from MATLAB, pre-layout HDL (synthesized) • Show edge-detected images • Show accuracy		
Show schematic and layout of synthesized design.		
Show latency, throughput, power consumption, and area (post-layout only) for i.) pre-layout and ii.) post-layout designs.		