UNIT-03

REGISTERS

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* Register :-

Register is one of the small seat of data holding place, that are part of the computer processor or computer memory. A register may hold an instruction, a storage address or any kind of data. It holds the binary data.

↳ Register is a data storage device that are more sophisticated than latch. A register is a group of binary cells suitable for holding binary information.

* Shift Register :- A register that is used to assemble and store information arriving from a serial source called shift register. Each flip-flop of shift register is connected to the output of the previous flip-flop and common clock pulse is applied to the all flip-flop.

↳ There are four types of shift register :-

i) Serial in Serial out (SISO)
ii) Serial in Parallel out (SIPO)
iii) Parallel in Parallel out (PIPO)
iv) Parallel in Serial out (PISO)

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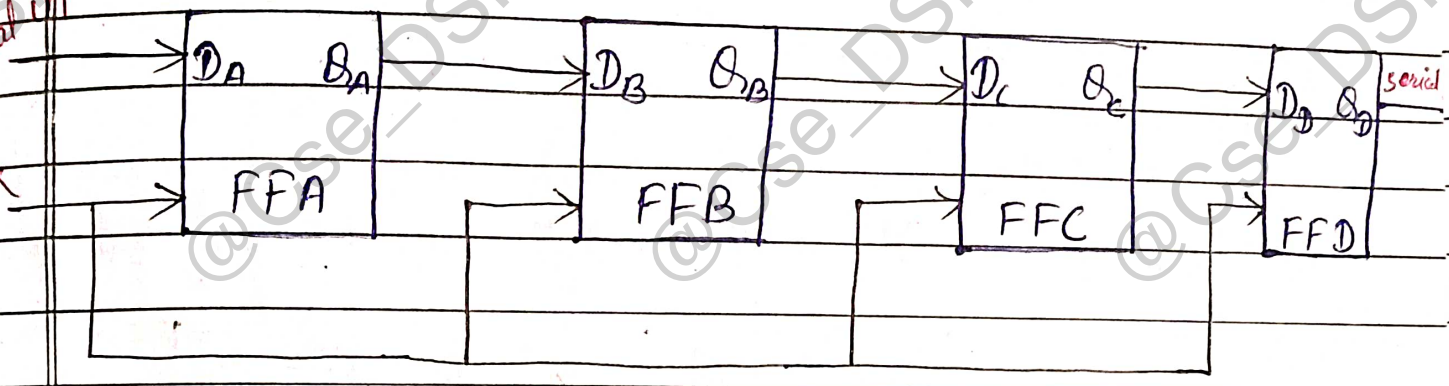
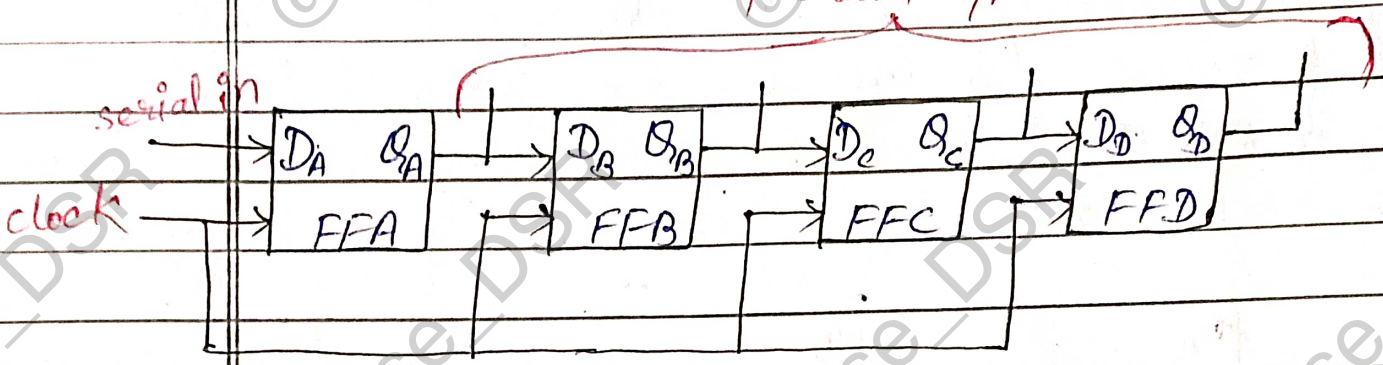
i) SISO shift register :— In SISO shift register serial input data is applied at the input of first flip-flop. Serial output data can be constructed at the output of last flip-flop. All flip-flop are connected in synchronous manner and transfer data from D_A to Q_D



Eg:- Assume 1011 data to be stored and transfer.

Clock	Data (1011)		Q_A	Q_B	Q_C	Q_D	
0th	1		0	0	0	0	
1st	0	I/P	1	0	0	0	
2nd	1		1	1	0	0	
3rd	1		0	1	1	0	
4th	0		1	0	1	1	
5th	0		0	1	0	1	O/P
6th	0		0	0	1	0	
7th	0		0	0	0	1	

ii) SIPO shift register :- In this type of register input data is applied serially and O/P is connected parallely.



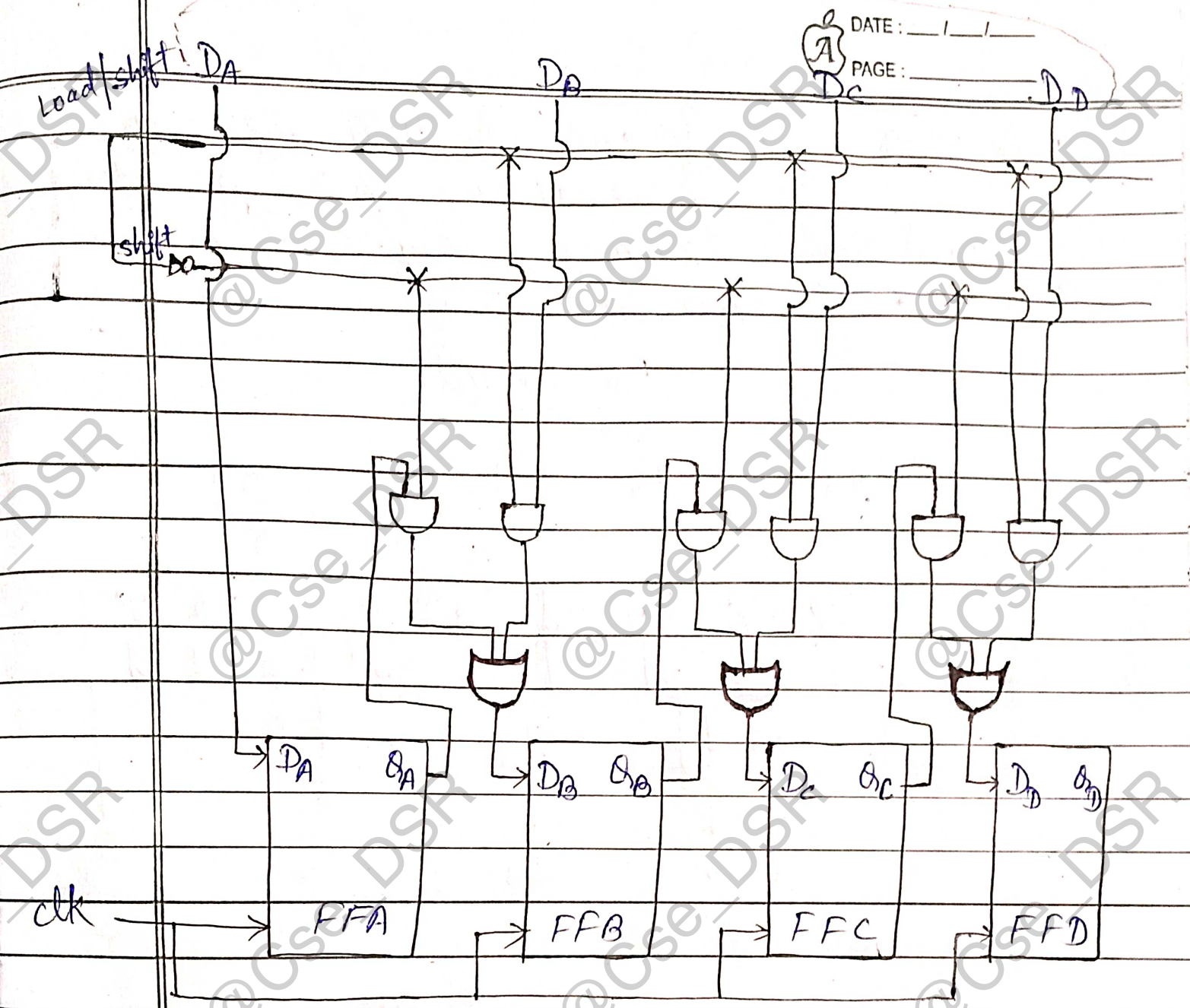
Eg:- Assume 1011 data to be stored and transfer.

Clock	Data (1011)		Q_A	Q_B	Q_C	Q_D
0th	1		0	0	0	0
1st	1	I/P	1	0	0	0
2nd	0		1	1	0	0
3rd	1		0	1	1	0
4th	0		1	0	1	1

Parallel O/P

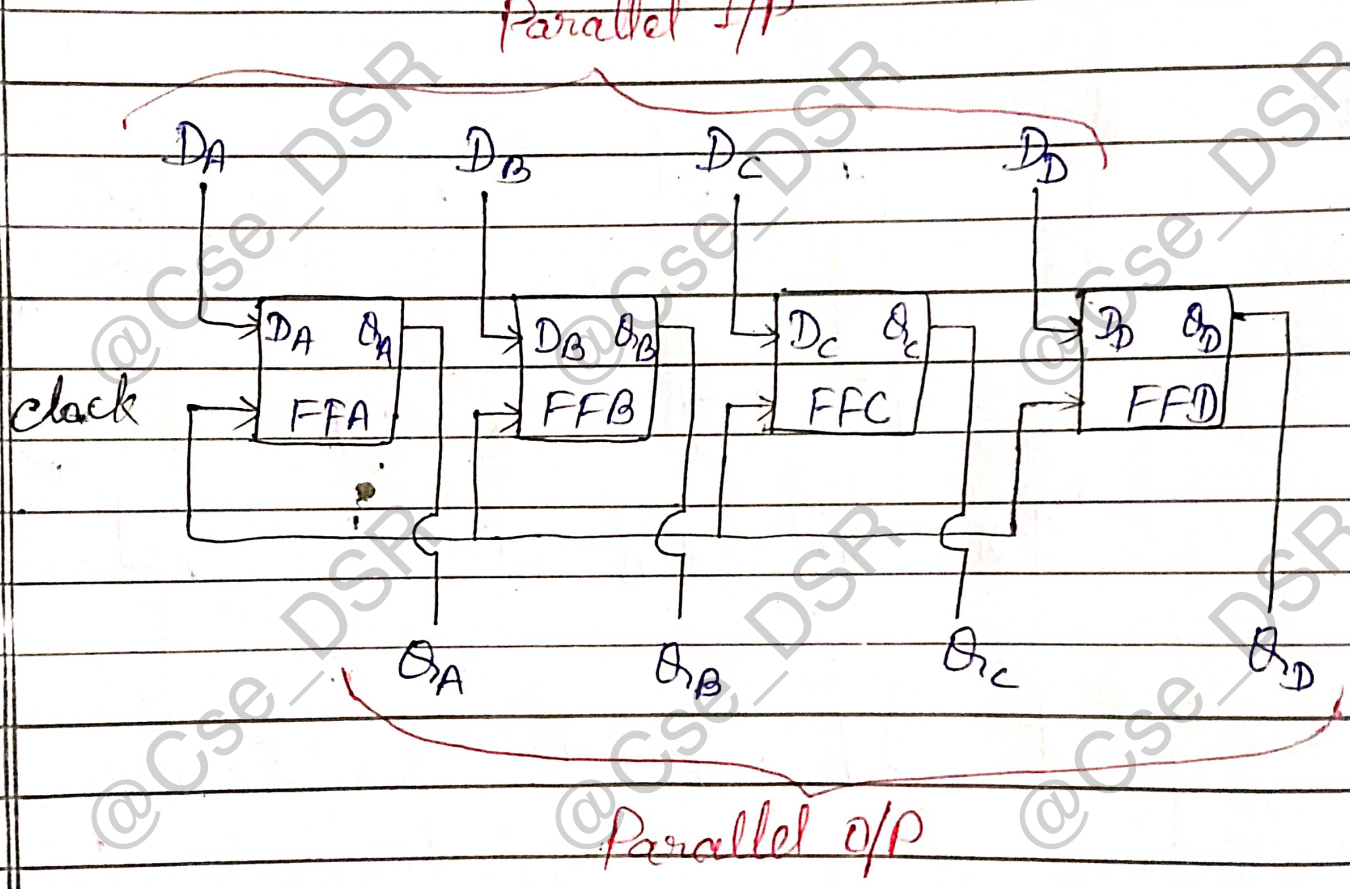
iii) PISO shift register :- In PISO shift register I/P is applied parallely and O/P is taken serially.

Parallel in



Clock	Load	$\overline{Load}$	D_A D_B D_C D_D	Q_A Q_B Q_C Q_D
0th	1	0	1	0 0 0 0
1st	1	0	1 1	1 0 0 0
2nd	1	0	1 1 0	1 1 0 0
3rd	1	0	1 1 0 1	0 1 1 0
4th			0 0 0 0	1 0 1 1
5th			0 0 0 0	0 1 0 1
6th			0 0 0 0	0 0 1 0
7th			0 0 0 0	0 0 0 1

iv) PIPO shift register :- In PIPO shift register I/P is applied parallely and O/P is taken parallely. This is also called "Buffer Register".



Clock	Data (1011)	Q_A Q_B Q_C Q_D
0th	1	0 0 0 0
1st	1 1	1 0 0 0
2nd	1 1 0	1 1 0 0
3rd	1 1 0 1	0 1 1 0
4th	0 0 0 0	1 0 1 1

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* Bidirectional shift register :-

Bidirectional shift register are the storage device capable of shifting the data either right or left depending on the mode selected.