Aim: To design and simulate 6-T SRAM using CADENCE and compute the delay between input and output waveforms

Tool & Apparatus Used: Cadence Virtuoso 6.1.3

Theory: SRAM consists of simple latch with 2 stable states. Based on the preserved state of the 2 inverters, the data being held in the memory cell is represented as logic 0 or logic 1. To read and write the data we need at least one switch, which is controlled by corresponding word line.

Access to SRAM memory is enabled by WL (Word Line) Line. It controls the 2 access transistors which control whether the cell should be connected o bit lines. These 2 lines are used to transfer data for both read and write. Data is stored in the Q and Q' inverters.

In the following circuit, nmos N1 provides the read current path for discharging a bit line(BL) or complementary bit line(BL') , depending on the stored value of Q and Q' respectively.

Read Operation:-

We need to pre charge both bit lines (BL=1 and BL'=1) and then we need to turn on word line(WL=1). One of the two bit lines will be pulled down by the cell.

Write Operation:-

We need to drive one bit line as high and other as low (BL=1 and BL'=0) or (BL=0 and BL'=1)) and then we need to turn on Word line(WL=1). Bitline overpowers cell with new values.

Hold Operation:-

When Word line is is turned off (WL=0), It is called as Hold operation. N2, N4 are OFF. Previously stored data will be shown.

6T SRAM is used in most commercial chips.

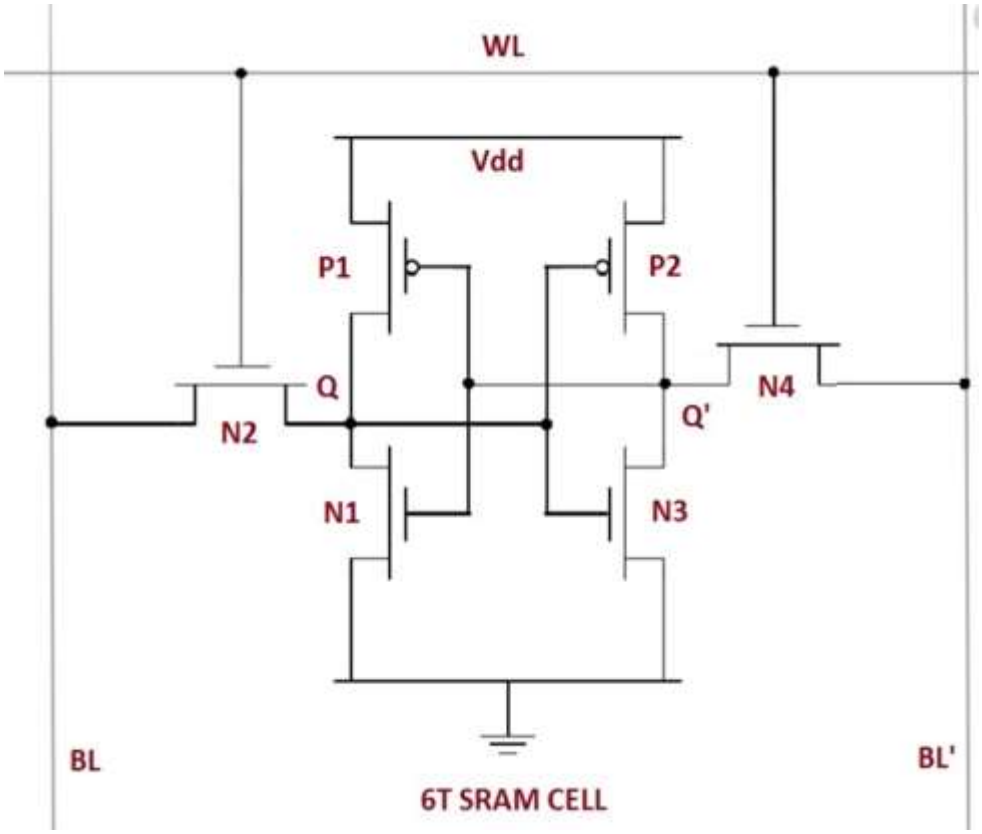

Fig.1 Circuit diagram of 6-T SRAM

Design and Simulation:

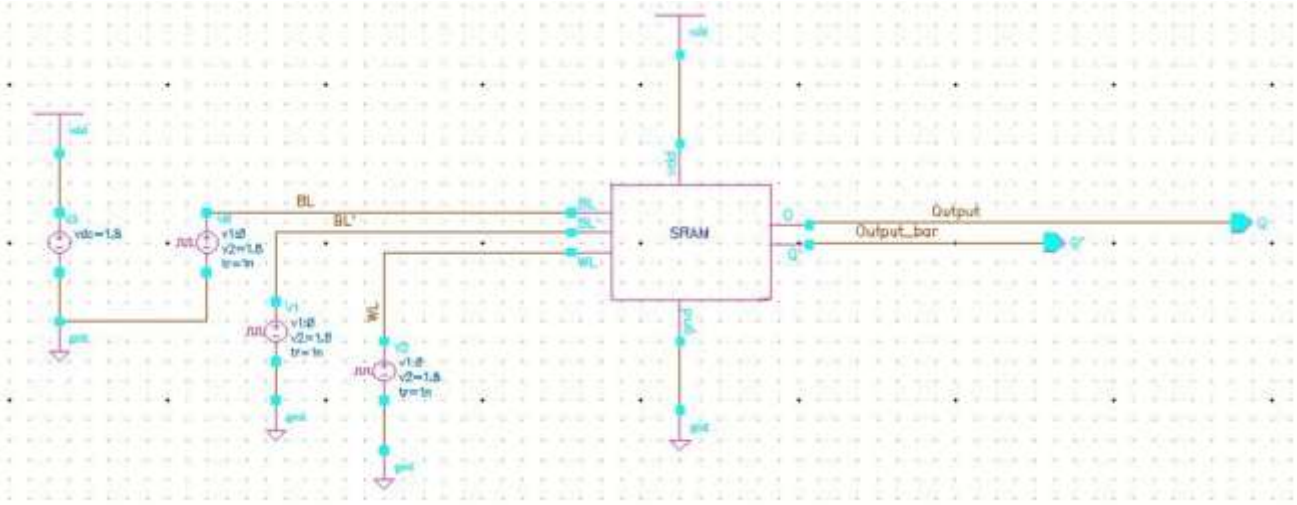

Figure 2 Symbol of 6-T SRAM

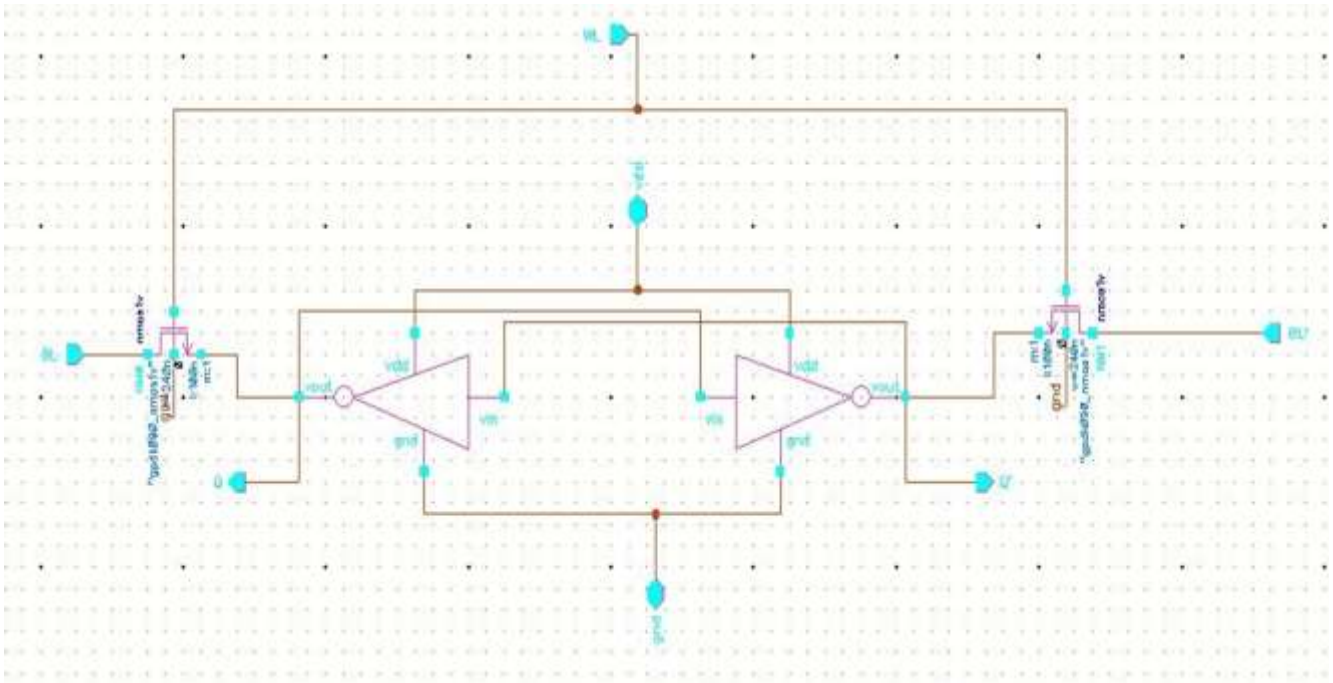

Figure 3 Schematic of 6-T SRAM

Table 1 Design specifications of 6-T SRAM

Parameters	**Values**
CMOS Technology	GPDK 90nm
NMOS: W/L	240nm/180nm
PMOS: W/L	720nm/180nm
V_{DD}	1.8V
Input signal BL (Pulse)	V1=1.8V, V2=0, Time Period=100ns, Pulse Width=49ns
Input signal BL'(Pulse)	V1=1.8V, V2=0, Time Period=200ns, Pulse Width=99ns
Input signal WL (Pulse)	V1=1.8V, V2=0, Time Period=300ns, Pulse Width=149ns

Observation:

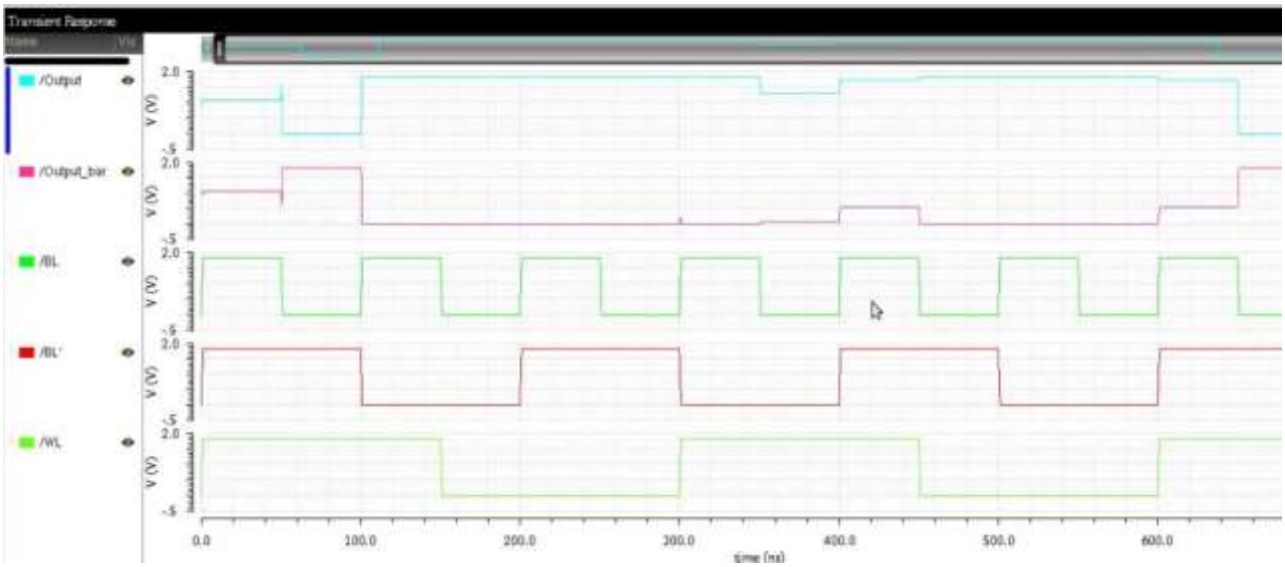

Figure 4 Transient results, Write Operation of 6-T SRAM

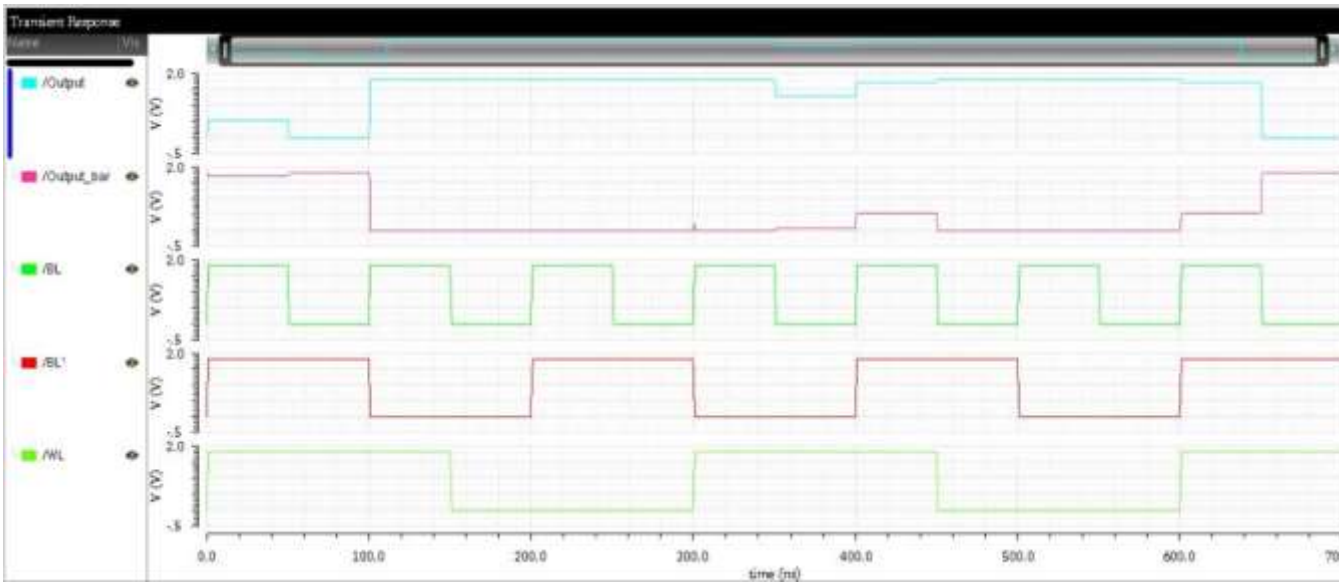

Figure 5 Transient results, Read Operation of 6-T SRAM

Calculated Average Power Dissipation: 186 µW

Result: 6T, SRAM is designed and simulated in Cadence virtuoso software. The transient result is obtained. The average power dissipation is 186 μW.