Design and Analysis of Low power 6T-SRAM Cell

Anand Kumar

Motilal Nehru National Institute of Technology
Allahabd, India
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***Abstract*-SRAM is the major data storage device due to its large storage density. Due to growth of low power digital service, there is a large demand of low voltage low power SRAM. The purpose of this paper is to design 6T SRAM cell with reduced read and write time, area and power consumption**

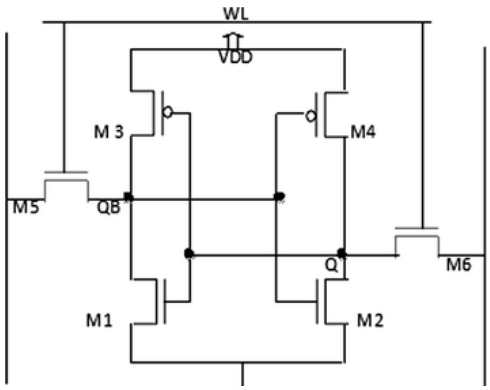
***Index Terms*— Cell ratio, delay, low power,CMOS**

I. Introduction

SRAM acts as a cache memory which providing interface with cpu at a very high speed. It requires less area and low power. It need less read and write time. It consumes less power. It has fast read and write operation. Reducing the width of pmos will reduce power consumption.

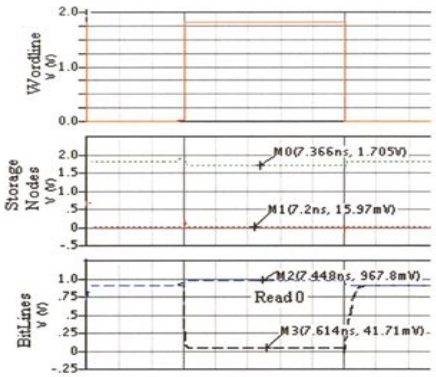
II. Reference Circuit details

6T-SRAM consists of flip flop connected with power supply and ground. It is designed with conventional bit lines It has two access nMOS transistors. The excess nmos transistor is designed larger than the pmos transistors. Four transistors form cross coupled inverters and it stores bits. The power dissipation is 186 µW.

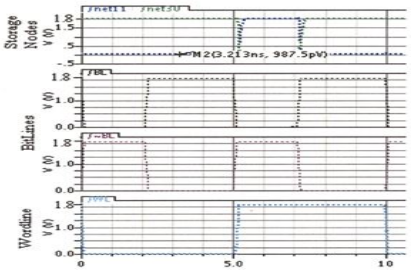


Schematic of 6-T SRAM

III . Reference Waveforms and Area Estimate



Read Operation of 6T-SRAM



Write Operation of 6T-SRAM

III. Reference Papers /Journals

[1] Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital integrated circuit A design perspective" second addition, Prentice Hall electronics and VLSI series. Berkley, Calistoga, Cambridge. 2003.

[2]Nilay Khare, Vijendra Kumar Kulhade, Pallavi Deshpande,"VLSI design and analysis of low power 6T SRAM cell using cadence tool",2008 IEEE International Conference on Semiconductor Electronics