Assignment 5 (EC39004: VLSI Laboratory)

Deadline: Upto 11th Feb, 2 pm

Instruction: You are required to submit in hard copy a neatly labeled circuit diagram of the scan flip-flop based pipelined left-right rotator, answer the associated questionnaire of Sec. 2 also in hard copy (one per group), and demonstrate the working of the Verilog codes and simulation outputs for the 4-bit left-right barrel shifter accepting unsigned inputs in your respective laptops or computer. Kindly zip your Verilog codes and test bench codes in a folder named by GROUP< *NO* :> and email it to < sudarshansharma04@gmail.com > , < harshit.roy30014@gmail.com >**and**< nitinkush16@gmail.com > **before coming to class on 11th Feb.**

1 Problem Statement

Consider a left right rotator that accepts two inputs: a 32-bit unsigned data input A, a second input B denoting the shift amount and a control signal R using **ONLY** 2:1 multiplexers as the sole circuit building block. When R = 0, the circuit performs the left rotate operation; otherwise when R = 1, it performs a right rotate operation on the same input data A. Pipeline the circuit such that only a single 2:1 multiplexer comes in the critical path. A second control input $TEST$ is introduced into the system. When $TEST$ = 0, the circuit performs the original functionality. However, when $TEST$ = 1, the FFs are stitched into scan chain(s), one chain for one bank of pipeline registers.

Write the Verilog Code for the above circuit description. For submission in hard copy, it is sufficient to draw a neatly labeled circuit diagram for the same considering A to be a 4-bit input only. Comment on the number of pipeline stages of the architecture if it was accepting a 64-bit input A.

2 Answer the following question

1. Draw a 4-bit UP counter with the scan chain functionality inserted within it, as discussed in the class..