

RTL to GDS II Physical Design of FA

Project summary



Submitted by

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Tools Used

Design Compiler

IC Compiler II

Prime Time

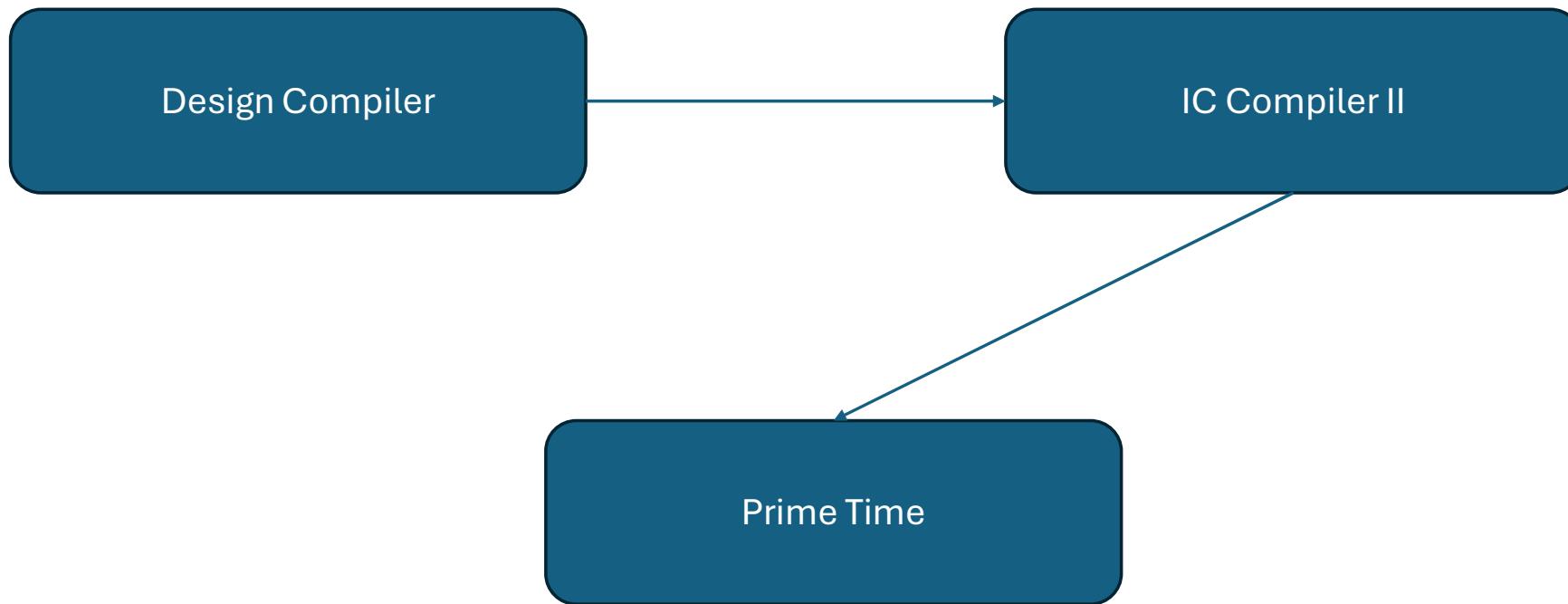
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Design Flow



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Design Compiler

```
ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/DC
login as: ws_ms2304102006_022
ws_ms2304102006_022@veo-1.trg.vlsiexpert.in's password:
Last login: Thu Mar  7 21:50:37 2024 from 103.159.214.187
[ws_ms2304102006_022@veo-1 ~]$ cd VE/VE_o1/IIT_4FA_FF/DC/
[ws_ms2304102006_022@veo-1 DC]$ dc_shell
Information: License queuing is enabled. (DCSH-18)

Design Compiler Graphical
  DC Ultra (TM)
  DFTMAX (TM)
  Power Compiler (TM)
  DesignWare (R)
  DC Expert (TM)
  Design Vision (TM)

DV Design Vision - TopLevel2
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power
Logical Hierarchy
Cell Name Ref Name
initializing gui preferences from file /ve/ws_home/ws_ms2304102006_022/.synopsys_dc_gui/preferences.tcl
_shell> start_gui
1
_shell> start_gui
_shell>
dc_shell>
```

```
ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/DC
login as: ws_ms2304102006_022
ws_ms2304102006_022@veo-1.trg.vlsiexpert.in's password:
Last login: Sun Mar  3 23:59:05 2024 from 103.159.214.186
[ws_ms2304102006_022@veo-1 ~]$ cd VE/VE_o1/IIT_4FA_FF/
[ws_ms2304102006_022@veo-1 IIT_4FA_FF]$ ls
CONSTRAINTS  DC  ICCII  PT  ref  rtl
[ws_ms2304102006_022@veo-1 IIT_4FA_FF]$ cd DC/
[ws_ms2304102006_022@veo-1 DC]$ ls
alib-52  default.svf  full_adder_netlist.v  paths.tcl  results  run_dc.tcl  WORK
command.log  filenames.log  newScript  reports  rm_setup  runNew_dc.tcl
[ws_ms2304102006_022@veo-1 DC]$ vim run_dc.tcl
Source ./paths.tcl
source -echo -verbose ./rm_setup/dc_setup.tcl
set RTL_SOURCE_FILES ../../full_adder_rtl.v

[ws_ms2304102006_022@veo-1 IIT_4FA_FF]$ cd ..
[ws_ms2304102006_022@veo-1 DC]$ ls
alib-52  default.svf  full_adder_netlist.v  paths.tcl  results  run_dc.tcl  WORK
command.log  filenames.log  newScript  reports  rm_setup  runNew_dc.tcl
[ws_ms2304102006_022@veo-1 DC]$
```

Running dc_shell and starting gui

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Design Compiler

The screenshot shows the Design Vision software interface. On the left, the 'Logical Hierarchy' pane displays a tree structure with a single node 'full_adder'. The main workspace shows a schematic diagram of a full adder. A terminal window on the right displays the command-line interface for running synthesis scripts. The terminal output includes:

```

ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/DC
}
set LIBRARY_DONT_USE_PRE_COMPILE_LIST "./rm_dc_scripts/snpss1_hpdu_synth.tcl";# Tcl file
for Synopsys Logic Library don't use list before first compile
}
./rm_dc_scripts/snpss1_hpdu_synth.tcl
purge -nW -info CompilerAnd_synth_info_script\n"
RM DC Design Vision - TopLevel2 (full_adder)
se
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power
dc full_adder Create Path Slack Histogram
Cell Name Ref Name Cell Path Dont Touch
Elaborated 1 design.
Current design is now 'full_adder'.
1
Current design is 'full_adder'.
dc_shell>
Log History
dc_shell> Create Path Slack Histogram.
No Selection
reg1_Reg | Flip-flop | 4 | Y | N | N | N | N | N | N | N |
reg2_Reg | Flip-flop | 4 | Y | N | N | N | N | N | N |
Q_Reg | Flip-flop | 4 | Y | N | N | N | N | N | N |
C_out_Reg | Flip-flop | 1 | N | N | N | N | N | N | N |
c_in_Reg | Flip-flop | 1 | N | N | N | N | N | N | N |
=====
Presto compilation completed successfully. (full_adder)
Elaborated 1 design.
Current design is now 'full_adder'.
1
Current design is 'full adder'.
dc_shell> dc_shell> [REDACTED]

```

**Imported Verilog coded
design of full adder**

Submitted by

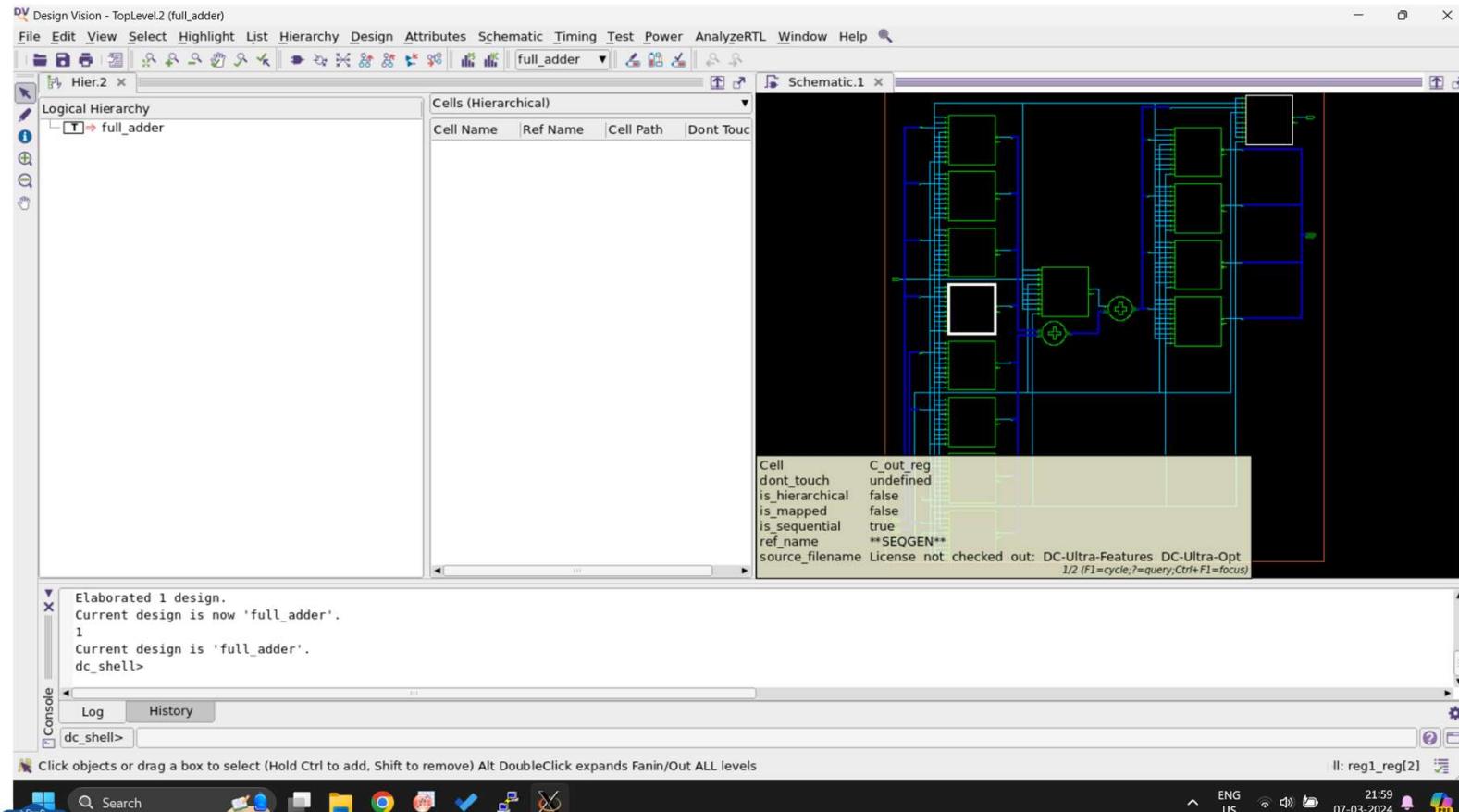
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Design Compiler



FA without reading sdc file

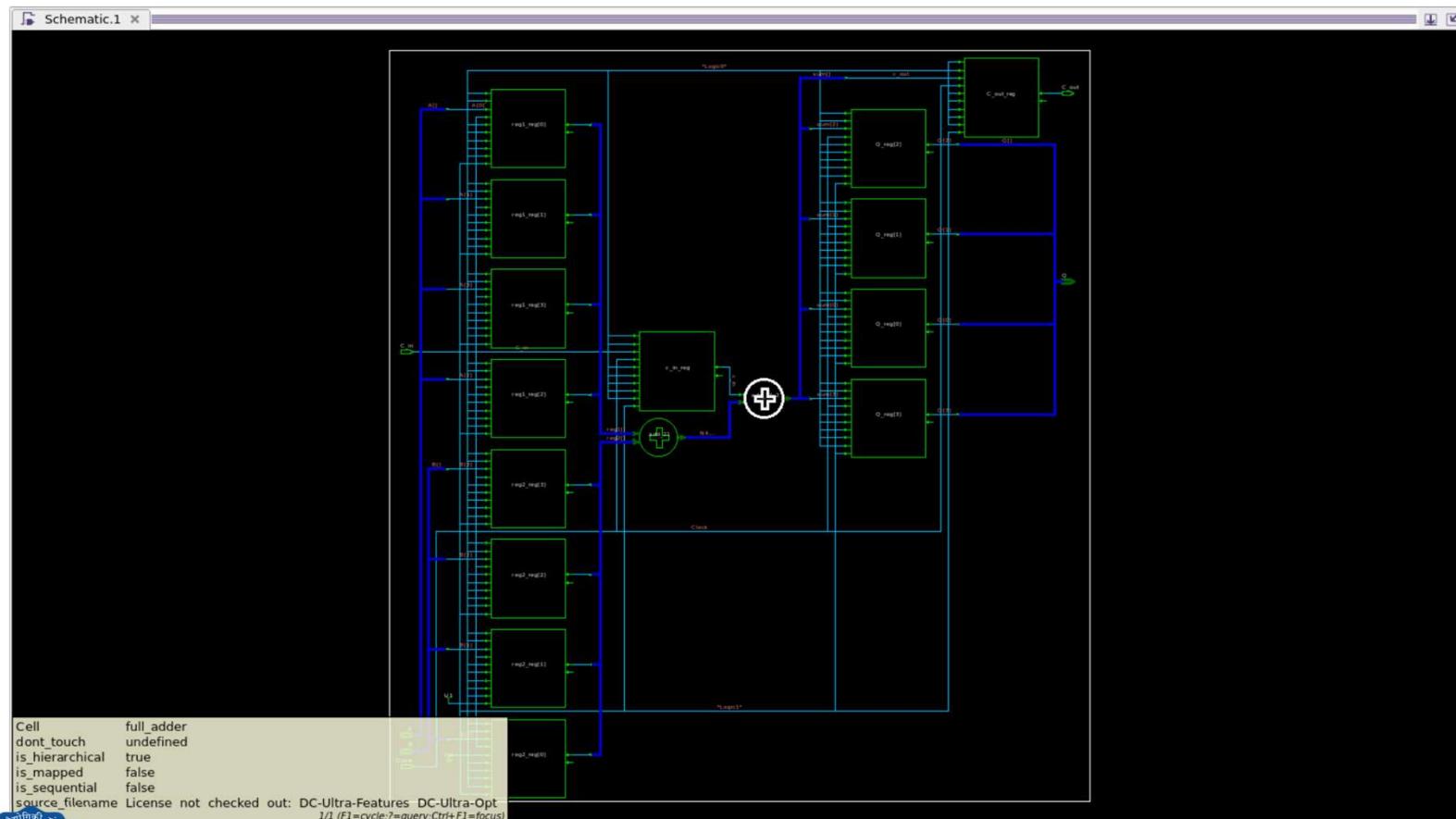
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Design Compiler



FA without reading sdc file

Submitted by

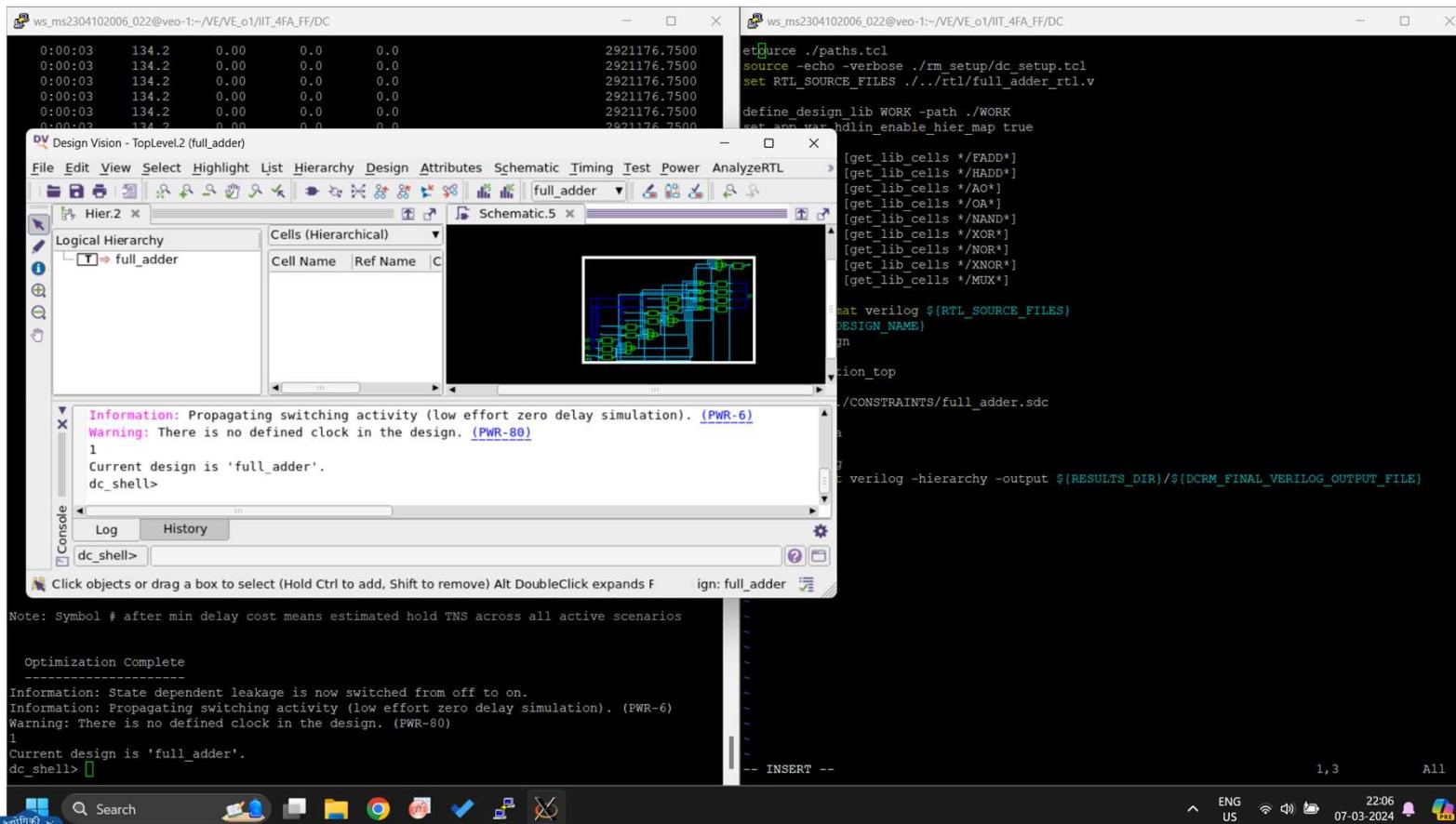
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Design Compiler



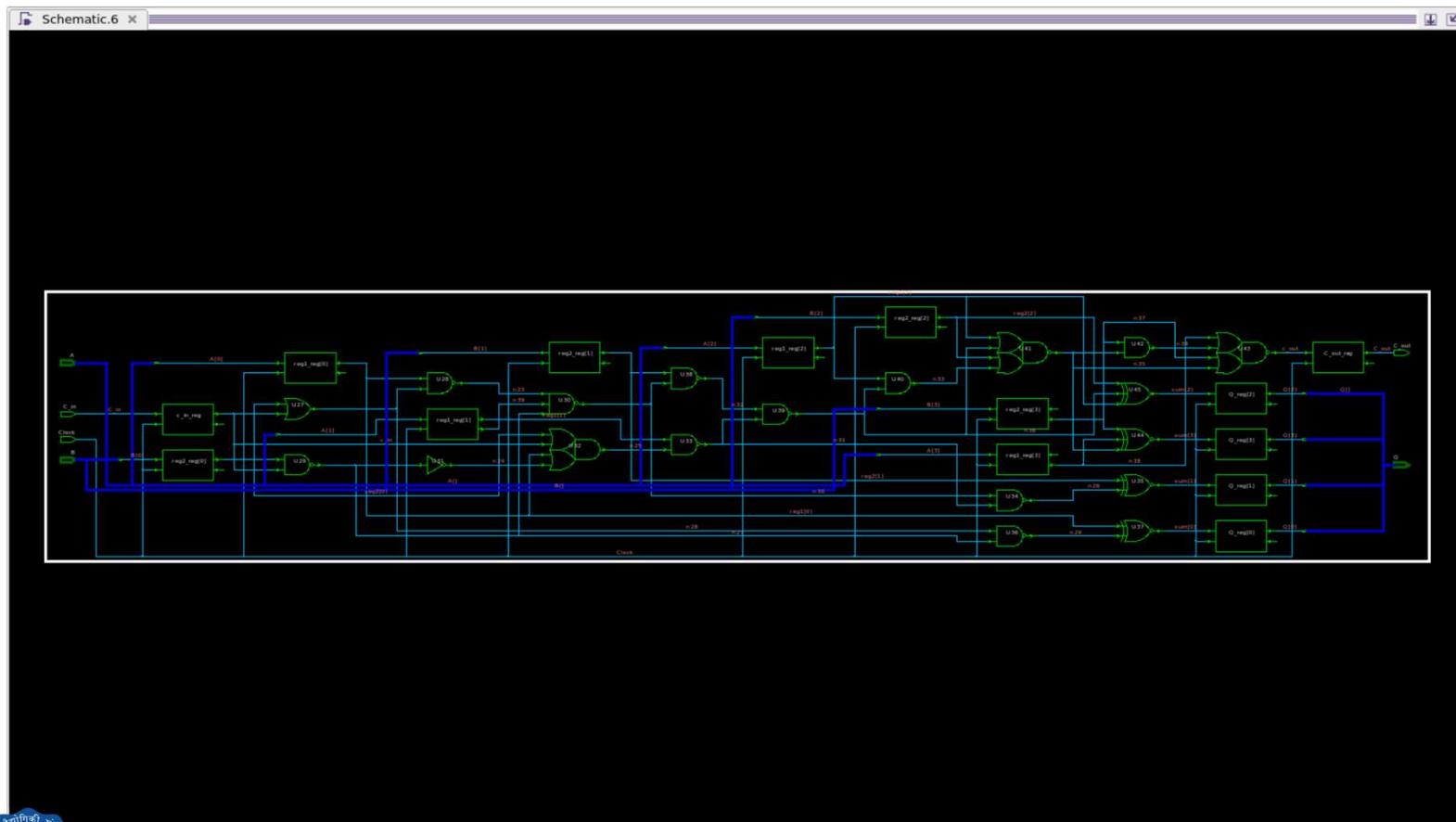
set dont FA
set dont HA

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Design Compiler



set dont FA
set dont HA
set dont AO

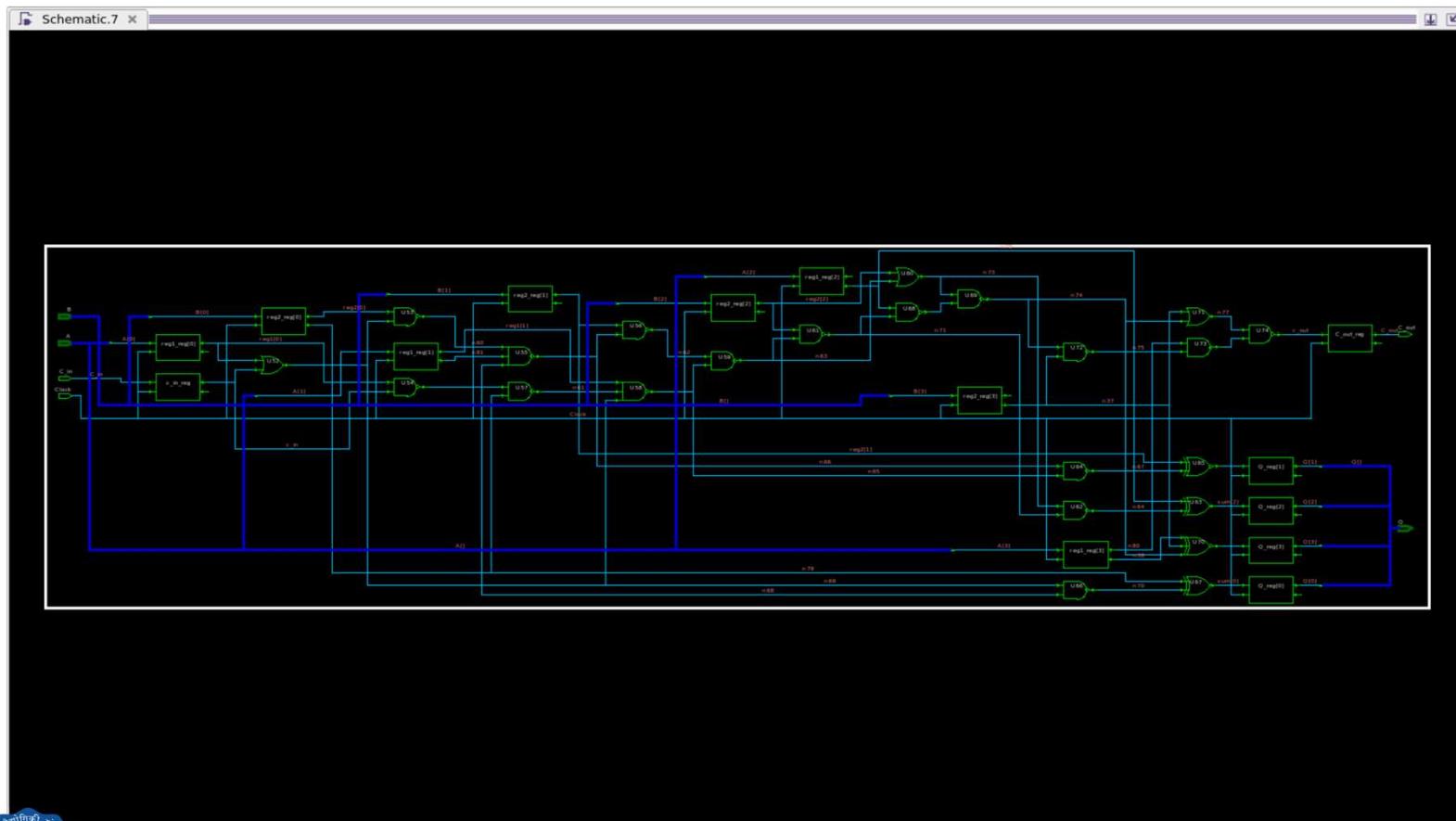
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Design Compiler



set dont FA
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set dont OA

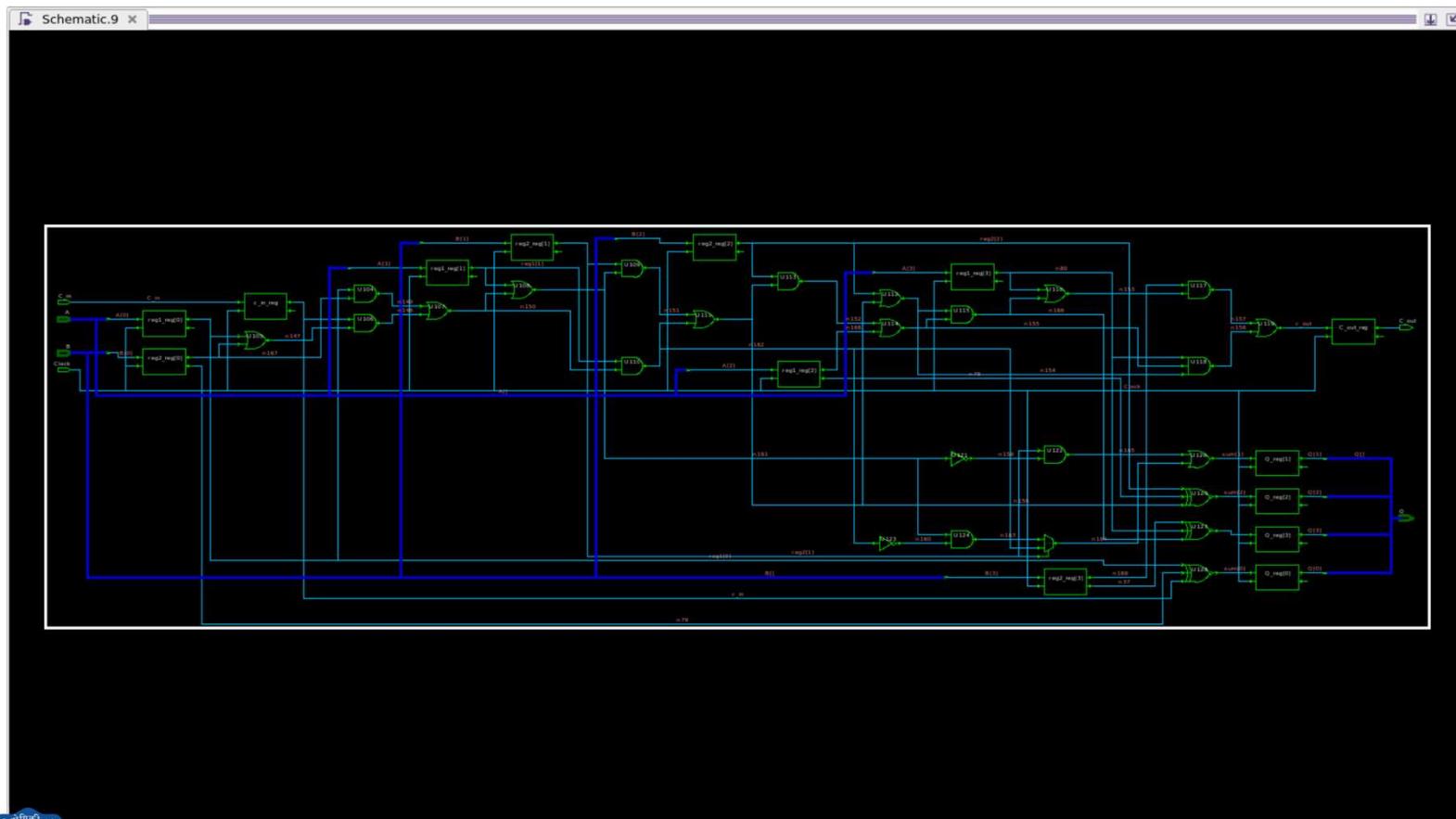
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Design Compiler



set dont FA
set dont HA
set dont AO
set dont OA
set dont NAND
set dont NOR

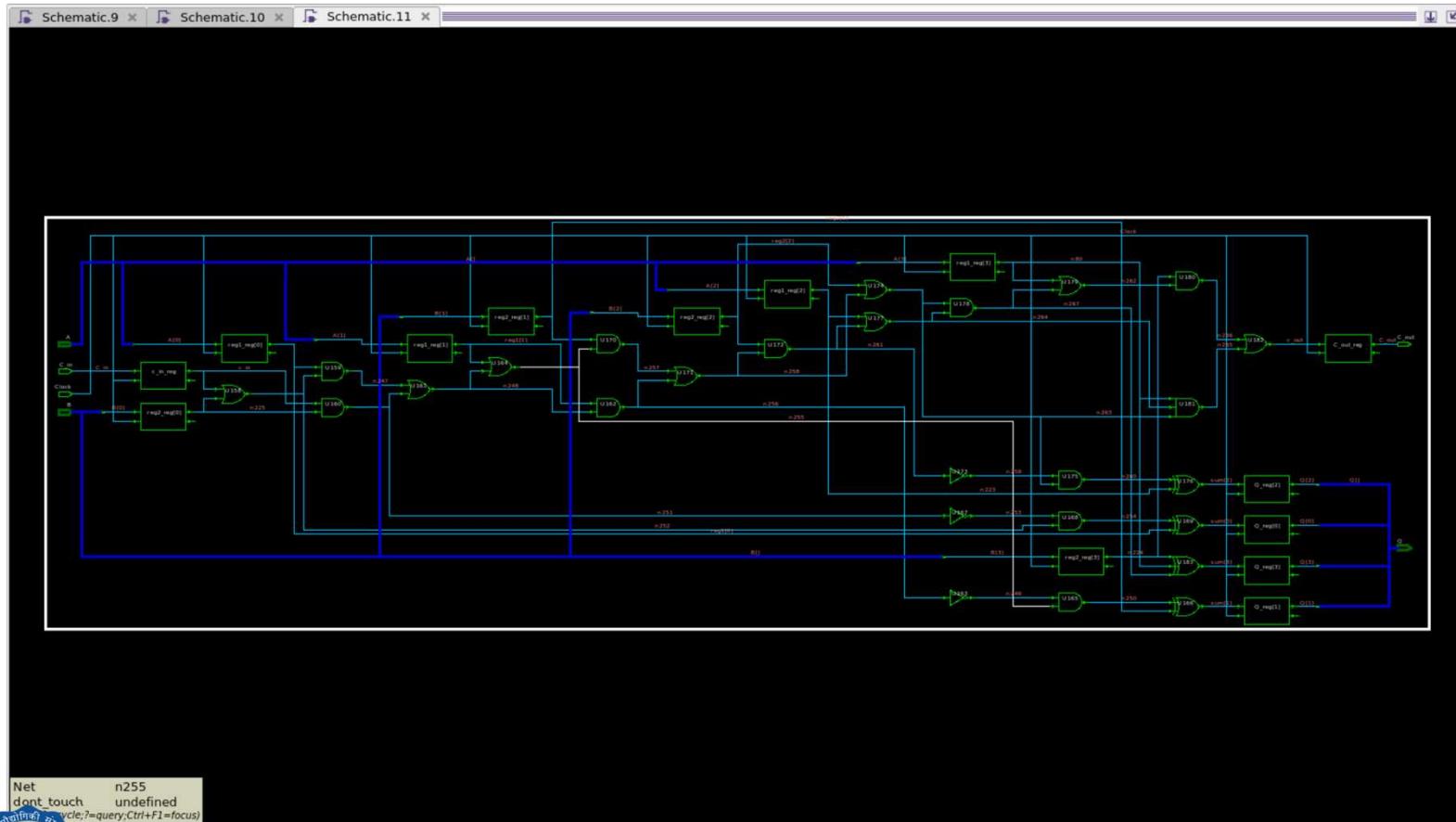
Submitted by

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Design Compiler



set dont FA
set dont HA
set dont AO
set dont OA
set dont NAND
set dont NOR
set dont MUX
set dont EXNOR

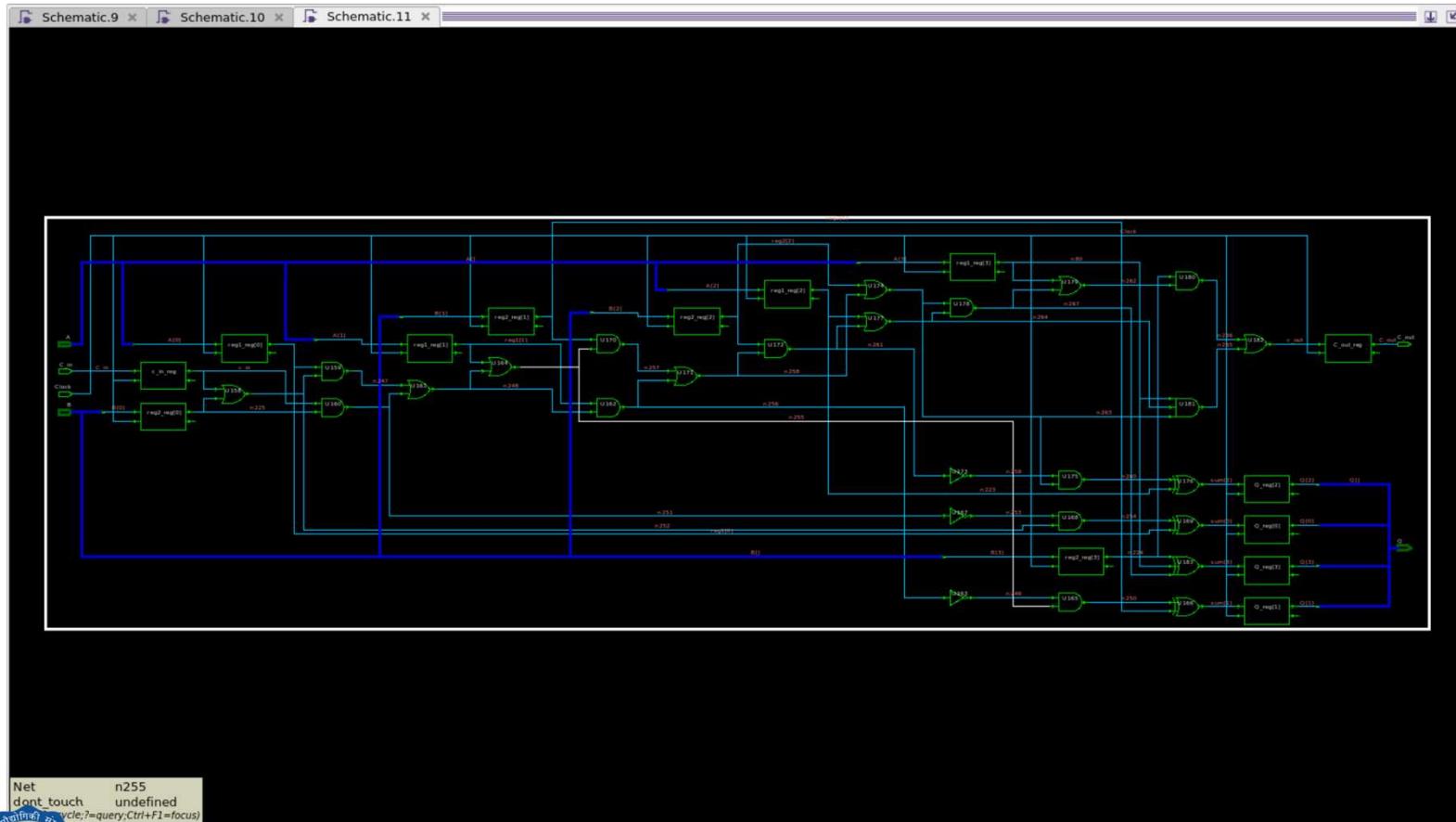
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Design Compiler



set dont FA
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Design Compiler

```

ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/DC
Operating Conditions: tt0p78vn40c Library: saed32rvt_tt0p78vn40c
Wire Load Model Mode: enclosed

Startpoint: c_in_reg (rising edge-triggered flip-flop clocked by Clock)
Endpoint: C_out_reg (rising edge-triggered flip-flop clocked by Clock)
Path Group: Clock
Path Type: max

Des/Clust/Port      Wire Load Model      Library
-----              -----
full_adder          ForQA                saed32rvt_tt0p78vn40c

Point               Incr     Path
-----              -----
clock Clock (rise edge)    0.00    0.00
clock network delay (ideal) 0.00    0.00
c_in_reg/CLK (DFFX1_RVT)   0.00    0.00 r
c_in_reg/Q (DFFX1_RVT)    0.19    0.19 f
U158/Y (OR2X1_RVT)       0.11    0.30 f
U159/Y (AND2X1_RVT)      0.09    0.38 f
U161/Y (OR2X1_RVT)       0.10    0.48 f
U164/Y (OR2X1_RVT)       0.09    0.57 f
U170/Y (AND2X1_RVT)      0.09    0.66 f
U171/Y (OR2X1_RVT)       0.10    0.76 f
U172/Y (AND2X1_RVT)      0.09    0.85 f
U177/Y (OR2X1_RVT)       0.09    0.95 f
U178/Y (AND2X1_RVT)      0.10    1.04 f
U179/Y (OR2X1_RVT)       0.09    1.13 f
U180/Y (AND2X1_RVT)      0.08    1.21 f
U182/Y (OR2X1_RVT)       0.09    1.31 f
C_out_reg/D (DFFX1_RVT)  0.01    1.32 f
data arrival time        1.32

clock Clock (rise edge)    1.00    1.00
clock network delay (ideal) 0.00    1.00
clock uncertainty         -0.30   0.70
C_out_reg/CLK (DFFX1_RVT) 0.00    0.70 r
library setup time         -0.09   0.61
data required time         0.61

data required time          0.61
data arrival time           -1.32

slack (VIOLATED)          -0.70

1
dc_shell>

```

set dont FA
set dont HA
set dont AO
set dont OA
set dont NAND
set dont NOR
set dont MUX
set dont EXNOR

Timing report

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Design Compiler

```

ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/DC
Operating Conditions: tt0p78vn40c Library: saed32rvt_tt0p78vn40c
Wire Load Model Mode: enclosed

Startpoint: c_in reg (rising edge-triggered flip-flop clocked by Clock)
Endpoint: C_out reg (rising edge-triggered flip-flop clocked by Clock)
Path Group: Clock
Path Type: max

Des/Clust/Port      Wire Load Model       Library
-----              -----
full_adder          ForQA                 saed32rvt_tt0p78vn40c

Point               Incr     Path
-----              -----
clock Clock (rise edge)      0.00    0.00
clock network delay (ideal)   0.00    0.00
c_in_reg/CLK (DFFX1_RVT)     0.00    0.00 r
c_in_reg/Q (DFFX1_RVT)      0.19    0.19 f
U158/Y (OR2X1_RVT)          0.11    0.30 f
U159/Y (AND2X1_RVT)         0.09    0.38 f
U161/Y (OR2X1_RVT)          0.10    0.48 f
U164/Y (OR2X1_RVT)          0.09    0.57 f
U170/Y (AND2X1_RVT)         0.09    0.66 f
U171/Y (OR2X1_RVT)          0.10    0.76 f
U172/Y (AND2X1_RVT)         0.09    0.85 f
U173/Y (OR2X1_RVT)          0.09    0.95 f
U178/Y (AND2X1_RVT)         0.10    1.04 f
U179/Y (OR2X1_RVT)          0.09    1.13 f
U180/Y (AND2X1_RVT)         0.08    1.21 f
U182/Y (OR2X1_RVT)          0.09    1.31 f
C_out_reg/D (DFFX1_RVT)     0.01    1.32 f
data arrival time           0.00    1.32

clock Clock (rise edge)      1.00    1.00
clock network delay (ideal)   0.00    1.00
clock uncertainty            -0.30   0.70
C_out_reg/CLK (DFFX1_RVT)    0.00    0.70 r
library setup time            -0.09   0.61
data required time           -0.09   0.61

data required time           0.61
data arrival time             -1.32

slack (VIOLATED)            -0.70

1
dc_shell>

```

```

ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/DC
et
source ./paths.tcl
source -echo -verbose ./rm setup/dc_setup.tcl
set RTL_SOURCE_FILES ../../rtl/full_adder_rtl.v

define_design lib WORK -path ./WORK
set app_var hdlin_enable_hier_map true

set dont_use [get_lib_cells */FADD*]
set dont_use [get_lib_cells */HADD*]
set dont_use [get_lib_cells */AO*]
set dont_use [get_lib_cells */OA*]
set dont_use [get_lib_cells */NAND*]
set dont_use [get_lib_cells */XOR*]
set dont_use [get_lib_cells */NOR*]
set dont_use [get_lib_cells */XNOR*]
set dont_use [get_lib_cells */MUX*]

analyze -format verilog ${RTL_SOURCE_FILES}
elaborate ${DESIGN_NAME}
current_design

set_verification_top

read_sdc ../../CONSTRAINTS/full_adder.sdc

compile_ultra

report_timing
write -format verilog -hierarchy -output ${RESULTS_DIR}/${DCRM_FINAL_VERILOG_OUTPUT_FILE}
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-- INSERT --
2,1
All

```

set dont FA
 set dont HA
 set dont AO
 set dont OA
 set dont NAND
 set dont NOR
 set dont MUX
 set dont EXNOR

Timing report

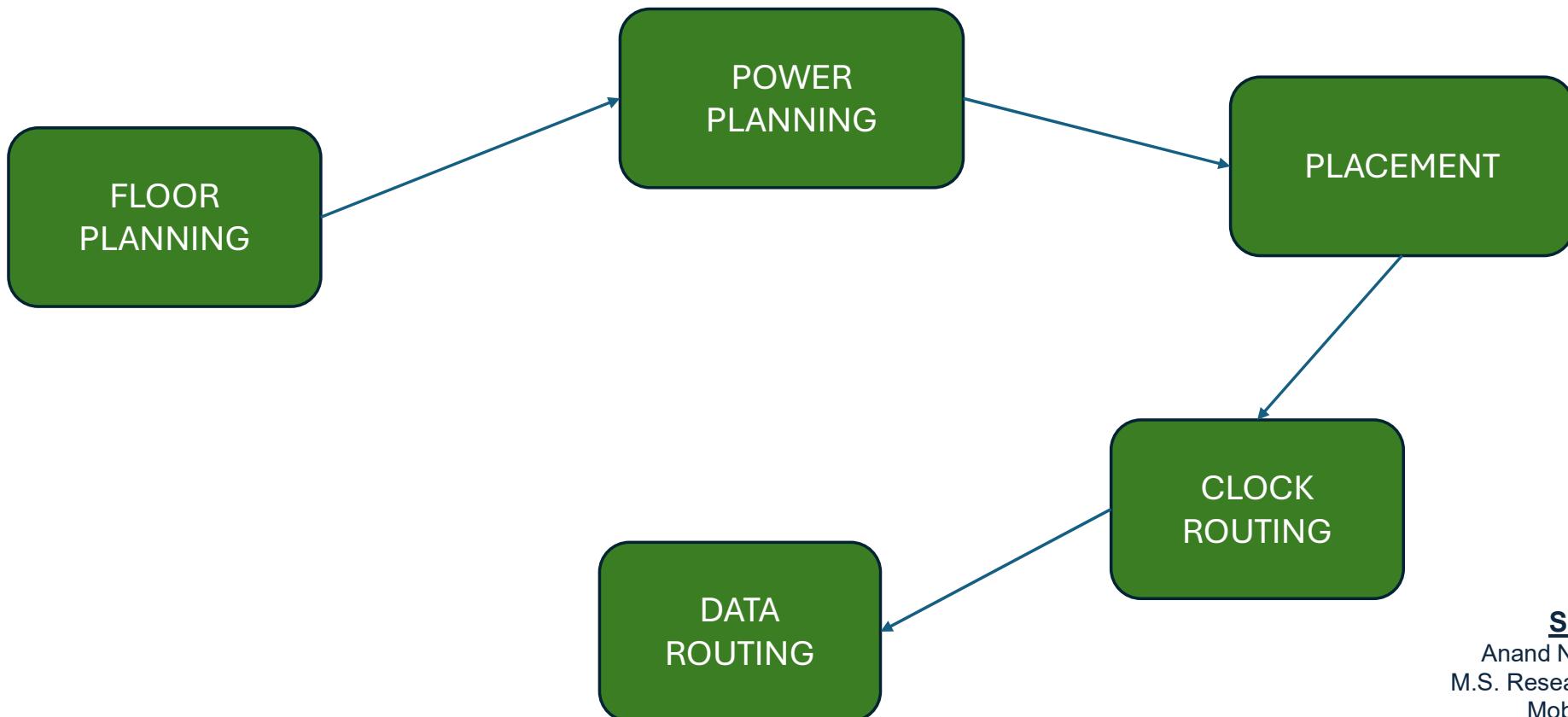
Submitted by

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ICC II



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ICC II

ICC II SHELL

The screenshot shows two windows of the IC Compiler II (ICC II) software. The left window is the command-line shell (icc2_shell) displaying the following text:

```
[ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/ICCI]$ icc2_shell
IC Compiler II (TM)
Version S-2021.06-SP5 for linux64 - Jan 14, 2022 -SLE
Copyright (c) 1988 - 2022 Synopsys, Inc.
This software and the associated documentation are proprietary to Synopsys, Inc. This software may only be used in accordance with the terms and conditions of a written license agreement with Synopsys, Inc. All other use, reproduction, or distribution of this software is strictly prohibited. Licensed Products communicate with Synopsys servers for the purpose of providing software updates, detecting software piracy and verifying Licensed Products in conformity with the Licensed Products. Synopsys will use information from this process to deliver software updates to infringers.
Inclusivity & Diversity - Visit SolvNetplus
Inclusivity and Diversity" (Refer https://solvnetplus.s...
```

The right window is the graphical user interface (BlockWindow.1) showing a floorplan setup. The command-line window contains the following TCL script:

```
source ../../DC/paths.tcl
create_lib -ref_libs $PDK_PATH/lib/stdcell_rvt/ndm/saed32rvt_c.ndm rvt_ndm_1
read_verilog (../../DC/results/full_adder.mapped.v) -library rvt_ndm_1 -design full_adder -top full_adder
# Floorplan settings
initialize_floorplan -core_utilization 0.7 -side_ratio {10 1}
set_individual_pin_constraints -ports [get_ports Clock] -sides 1
set_block_pin_constraints -self -sides "1 2"
create_placement -floorplan
```

The interface includes various toolbars, menus (File, Task, Edit, Create, View, Select, Highlight, Schematic, Window, Help), and a central workspace for placing and routing blocks.

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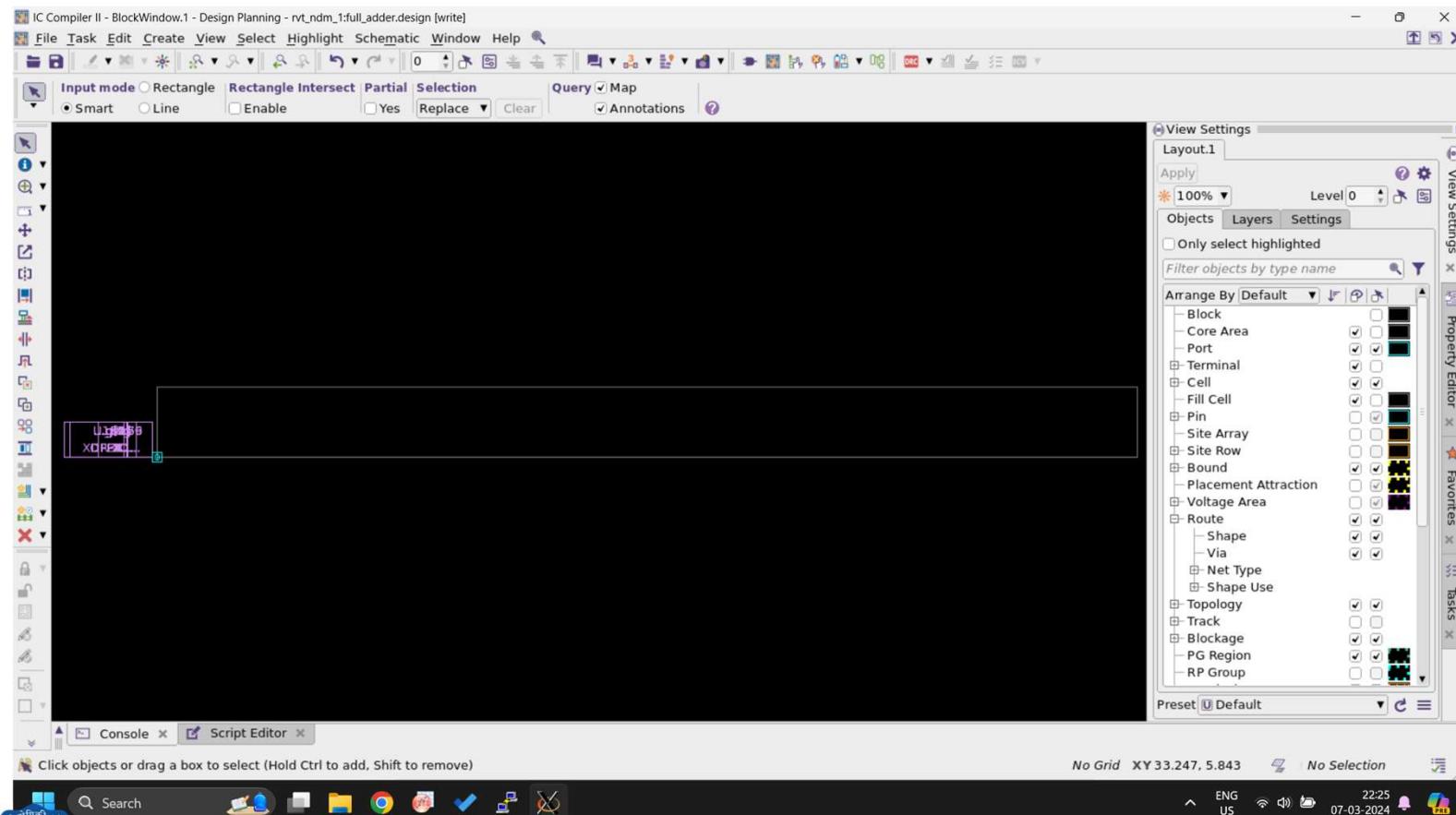
Email : anandkachale@gmail.com

LinkedIn : www.linkedin.com/in/anand-kachale-113a82108



ICC II

FLOOR PLANNING



RECTANGLE
cu 0.7 side ratio
10.1

Submitted by

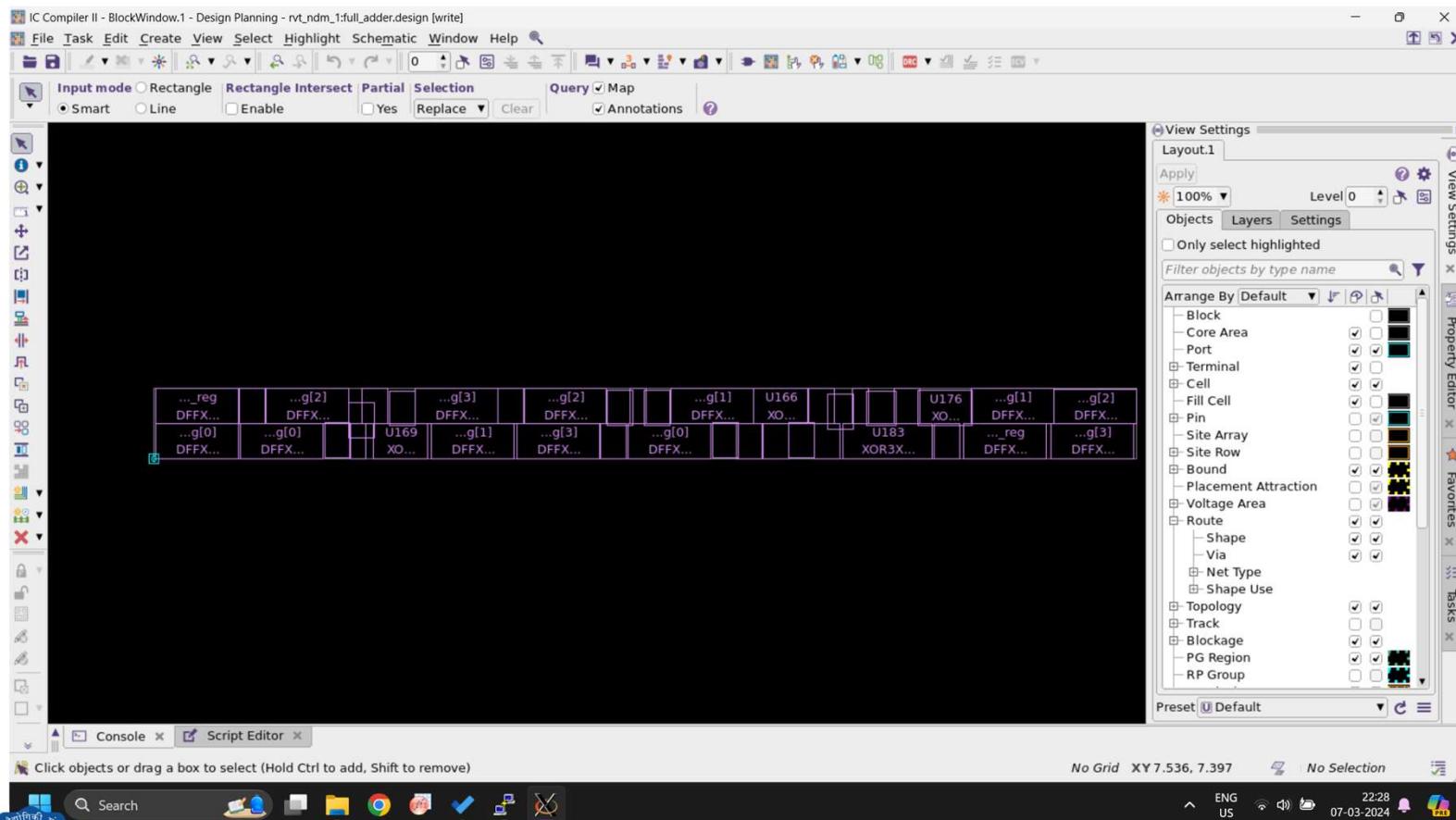
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ICC II

FLOOR PLANNING



RECTANGLE
individual pin
constraints and
block pin
constraints

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ICC II

FLOOR PLANNING

SQUARE
script

The image shows two terminal windows side-by-side. The left window displays the output of a Verilog simulation or synthesis process. It includes reports on block placement, wire length, physical hierarchy violations, voltage area violations, and hard macro overlaps. The right window shows a TCL script for floor planning, which initializes a floorplan with utilization constraints and creates placement scenarios for different shapes (U, T, L) with specific side ratios and orientations.

```
ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/ICCII
Running block placement.
Floorplan placement done.
*****
Report : report_placement
Design : full_adder
Version: S-2021.06-SPS
Date : Thu Mar 7 22:37:35 2024
*****
Wire length report (all)
=====
wire length in design full_adder: 181.496 microns.
 number of nets with unassigned pins: 15
wire length in design full_adder (see through blk pins): 181.496 microns.
-----
Total wire length: 181.496 microns.

Physical hierarchy violations report
=====
Violations in design full_adder:
 0 cells have placement violation.
-----
Total 0 cells have placement violation.

Voltage area violations report
=====
Voltage area placement violations in design full_adder:
 0 cells placed outside the voltage area which they belong to.
-----
Total 0 macro cells placed outside the voltage area which they belong to.

Hard macro to hard macro overlap report
=====
HM to HM overlaps in design full_adder: 0
-----
Total hard macro to hard macro overlaps: 0

Information: Default error view full_adder_dplace.err is created in GUI error browser. (DPP-054)
Information: Elapsed time for create_placement excluding pending time: 00:00:00.08. (DPUI-902)
)
Information: CPU time for create_placement : 00:00:00.08. (DPUI-903)
Information: Peak memory usage for create_placement : 514 MB. (DPUI-904)
Information: Ending 'create_placement' (FLW-8001)
Information: Time: 2024-03-07 22:37:35 / Session: 0.30 hr / Command: 0.00 hr / Memory: 515 MB (FLW-8100)
1
icc2_shell> 
```

```
ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/ICCII/scripts
source ../../DC/paths.tcl
open_lib full_adder
read verilog ../../DC/results/full_adder.mapped.v -library full_adder -design full_adder -top full_adder
# Floorplan settings
#
#scenarios:
#
initialize_floorplan -core_utilization 0.9
set_individual_pin_constraints -ports [get_ports Clock] -sides 1
set_block_pin_constraints -self -sides "0/0"
create_placement -floorplan
#
#
#scenario2:
#
initialize_floorplan -core_utilization 0.9 -shape U
set_individual_pin_constraints -ports [get_ports Clock] -sides 1 -location {0 0}
set_block_pin_constraints -self -sides "1.2"
create_placement -floorplan
#
#
#scenario3:
#
initialize_floorplan -core_utilization 0.5 -shape T -side_ratio {1 1 1 2 1 1} -orientation S
set_individual_pin_constraints -ports [get_ports Clock] -location {0 0}
set_block_pin_constraints -self -sides "4"
create_placement -floorplan
#
#
#scenario4:
#
initialize_floorplan -core_utilization 0.7 -boundary { {0 0} {0 100} {50 100} {50 0} }
set_individual_pin_constraints -ports [get_ports Clock] -sides 1
set_block_pin_constraints -self -sides "1.2"
create_placement -floorplan
#
#
#scenario5:
#
initialize_floorplan -core_utilization 0.8 -side_ratio {6 3}
set_individual_pin_constraints -ports [get_ports Clock] -sides 1
"floorplan.tcl" 53L, 1359C
1,1 Top
```

Submitted by

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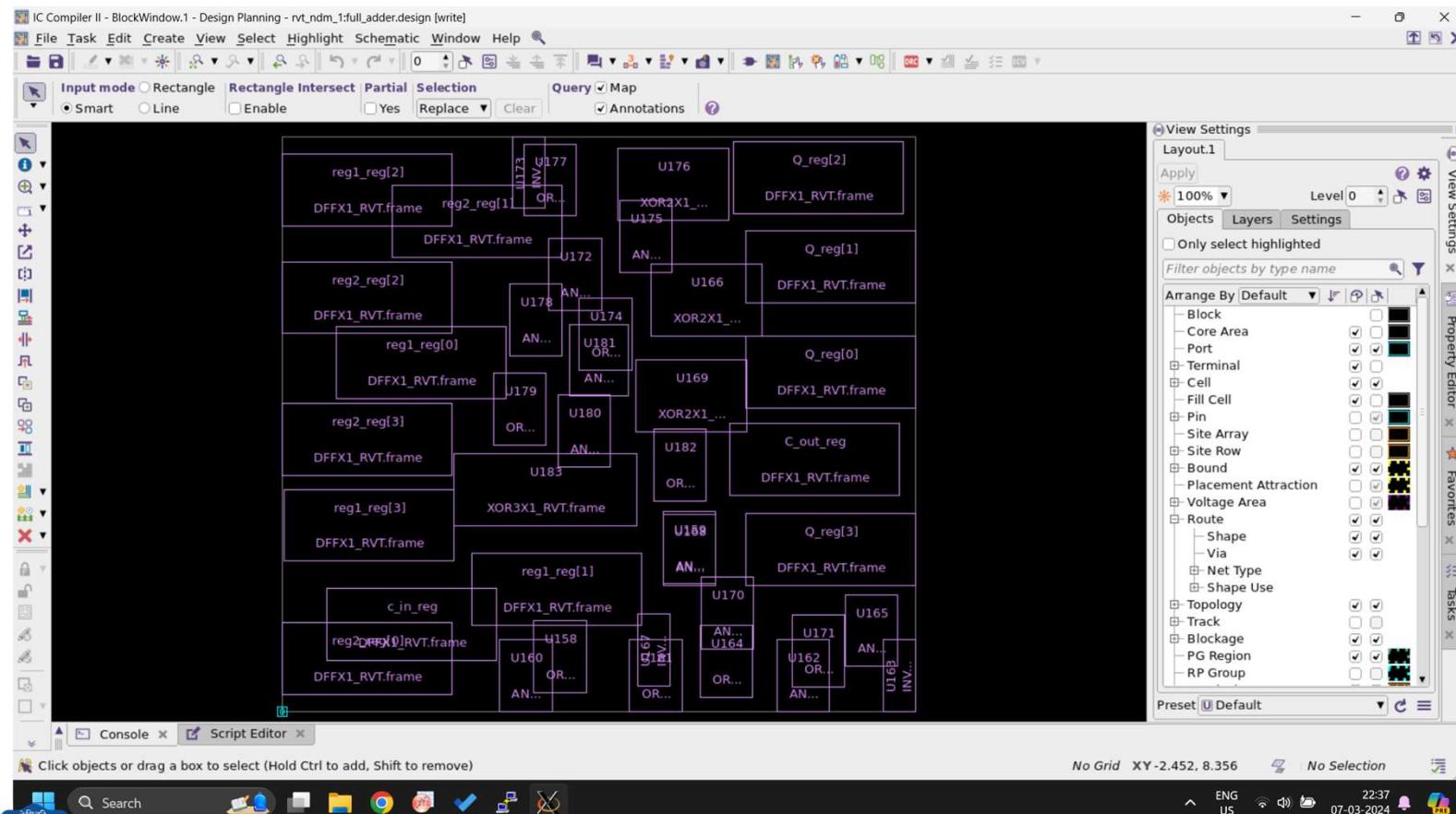
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ICC II

FLOOR PLANNING



SQUARE fp

Submitted by

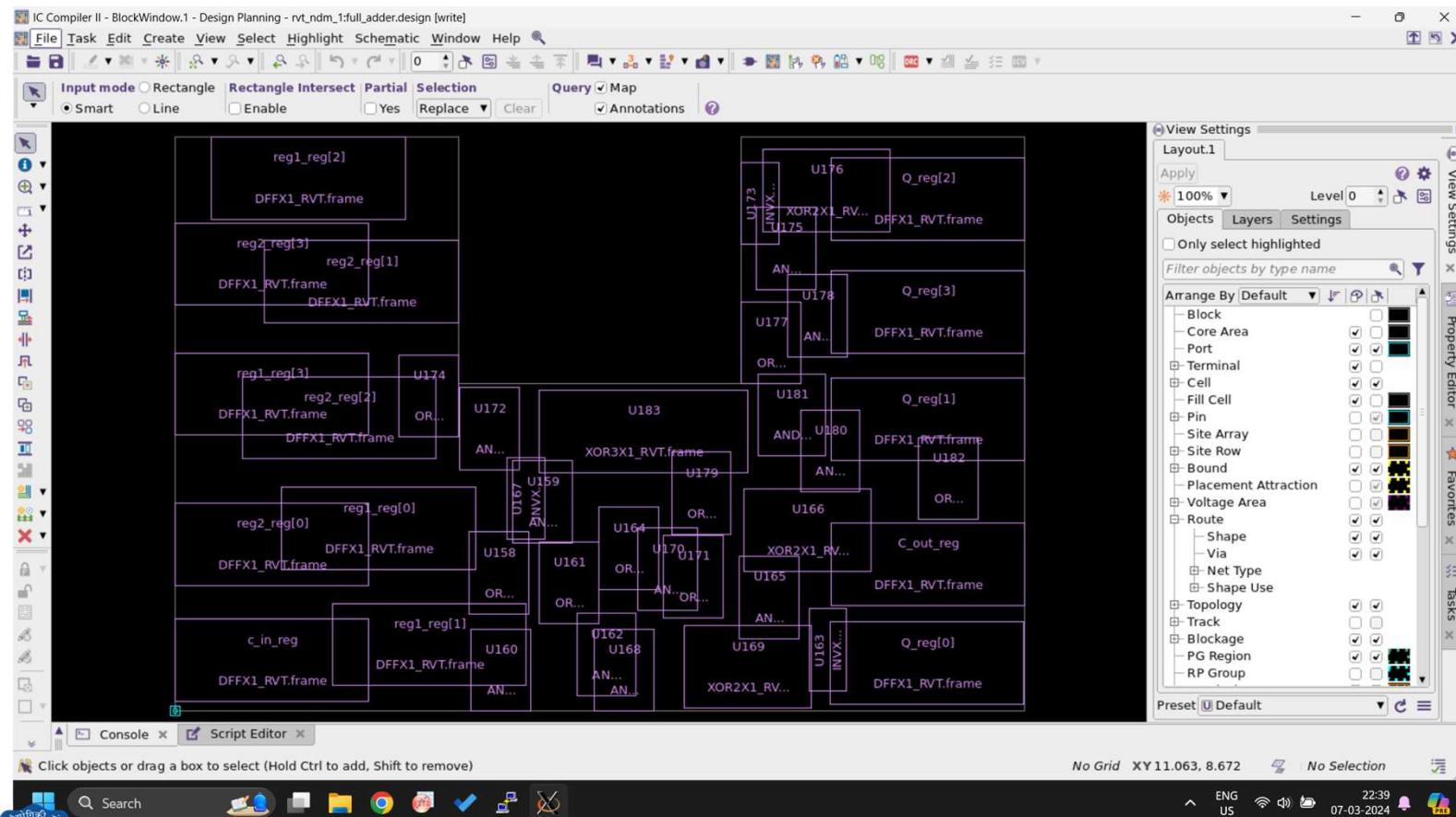
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ICC II

FLOOR PLANNING



U fp

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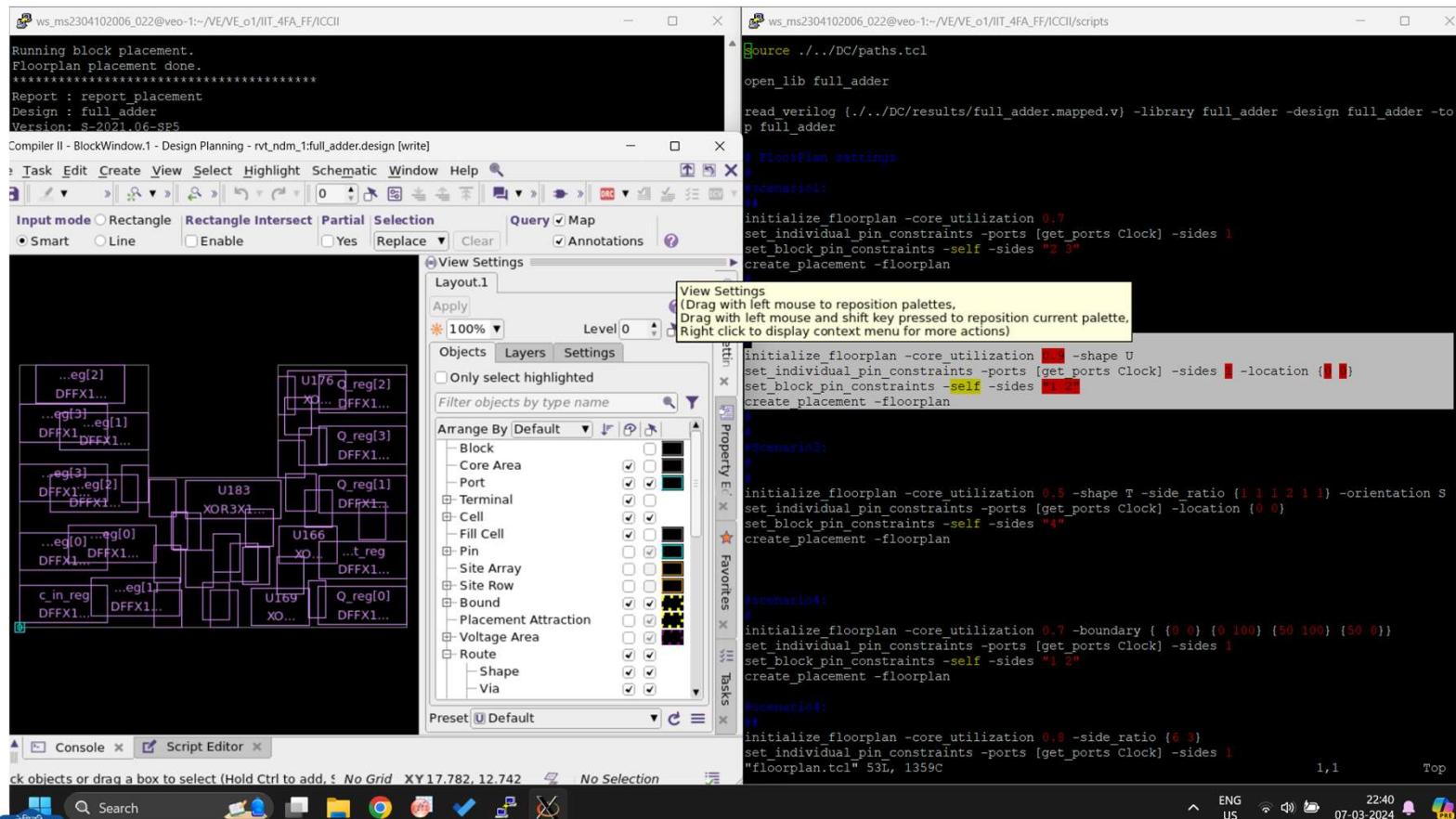
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ICC II

FLOOR PLANNING

U
script



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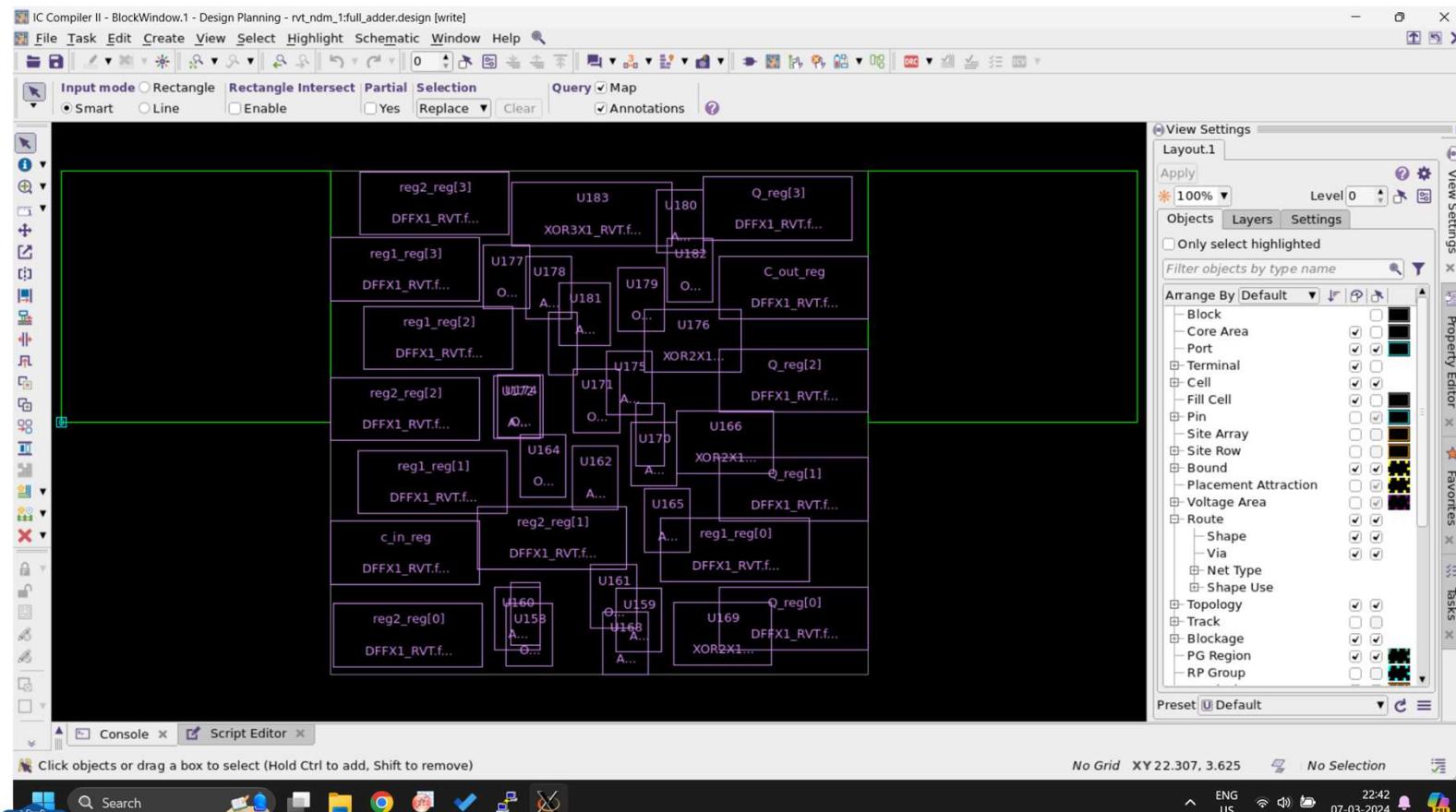
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ICC II

FLOOR PLANNING



T
NORTH
ORIENTATION
fp

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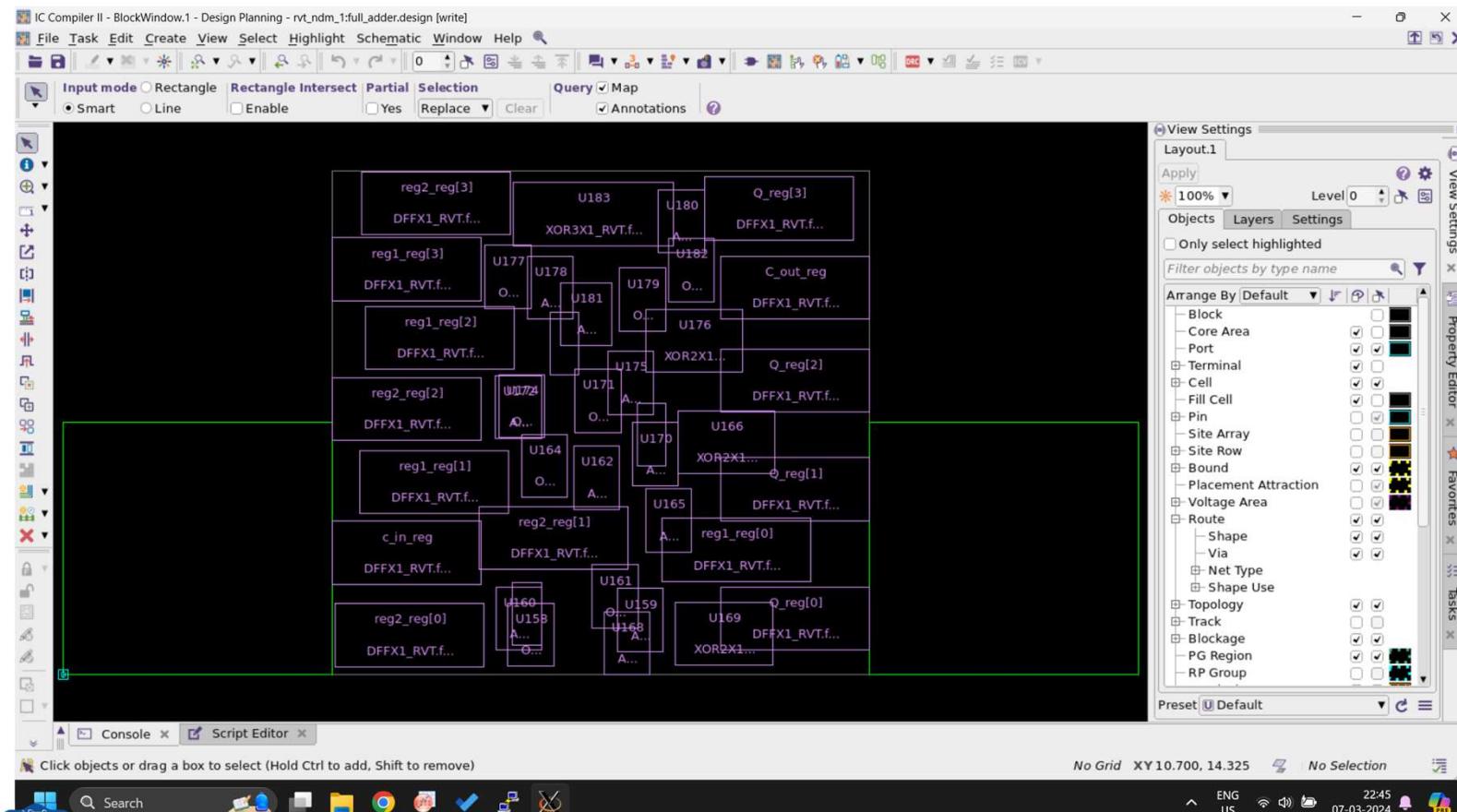
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ICC II

FLOOR PLANNING



T
SOUTH
ORIENTATION
fp

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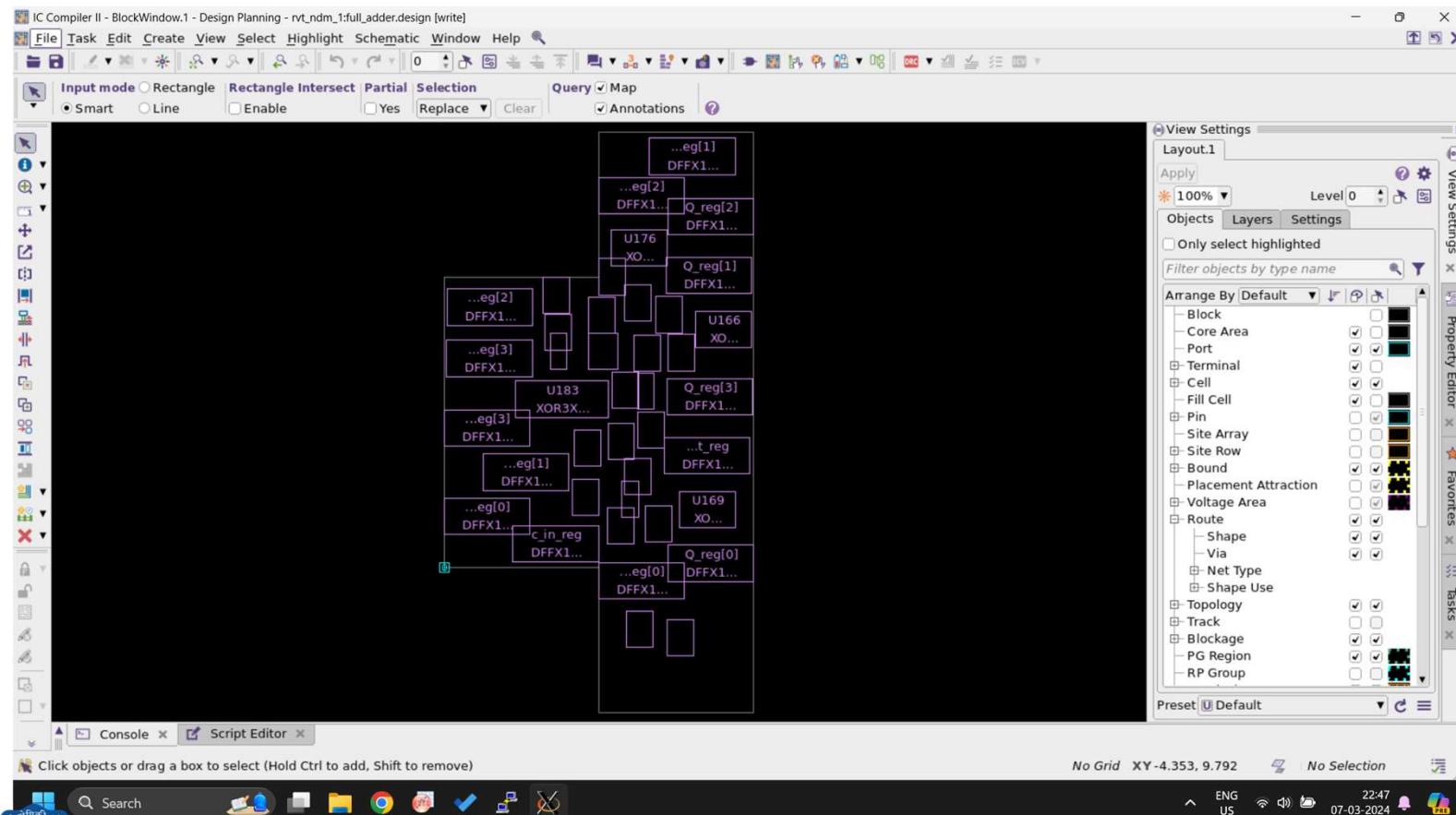
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ICC II

FLOOR PLANNING



T
EAST
ORIENTATION
fp

Submitted by

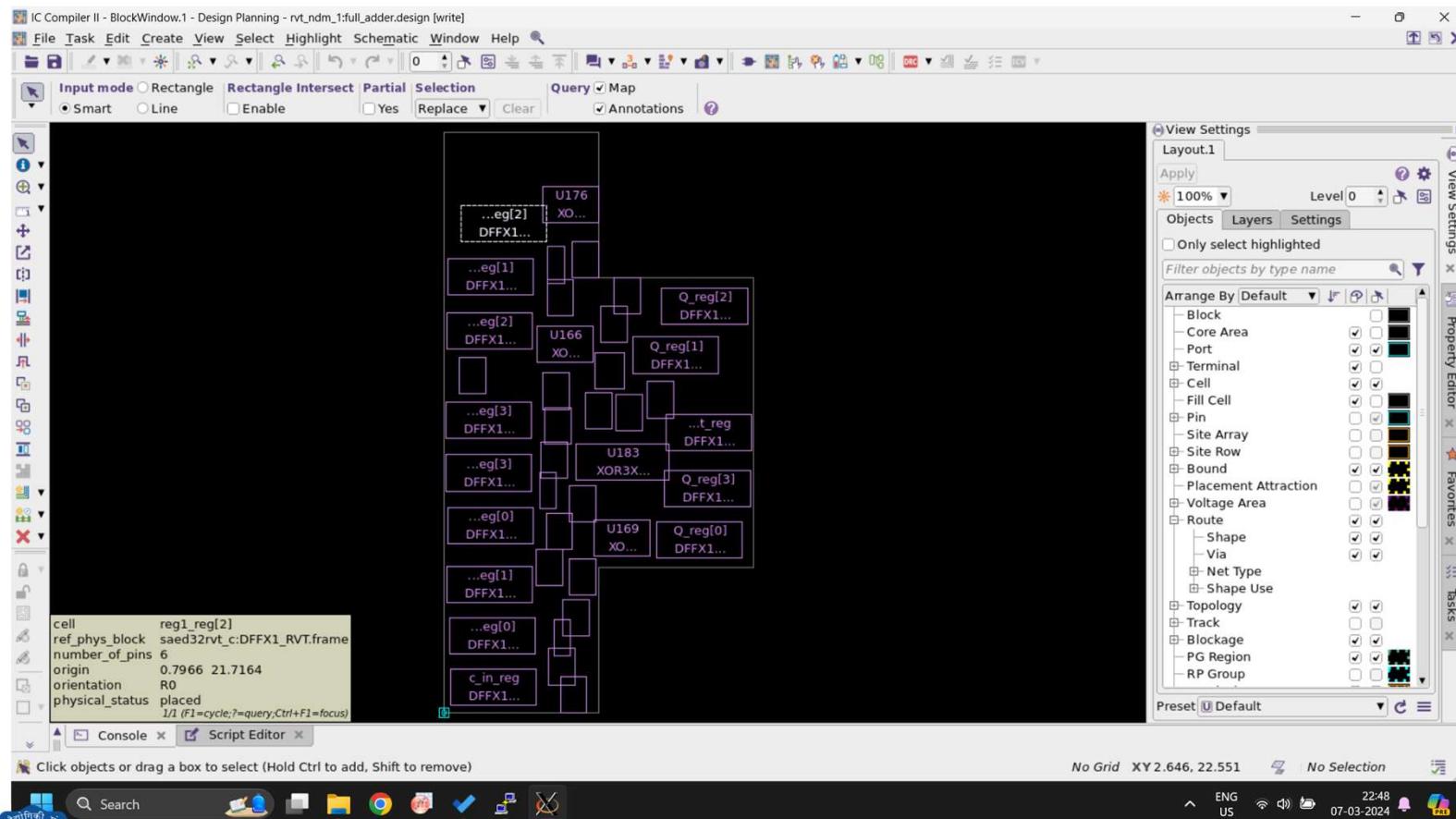
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ICC II

FLOOR PLANNING



T
WEST
ORIENTATION
fp

Submitted by

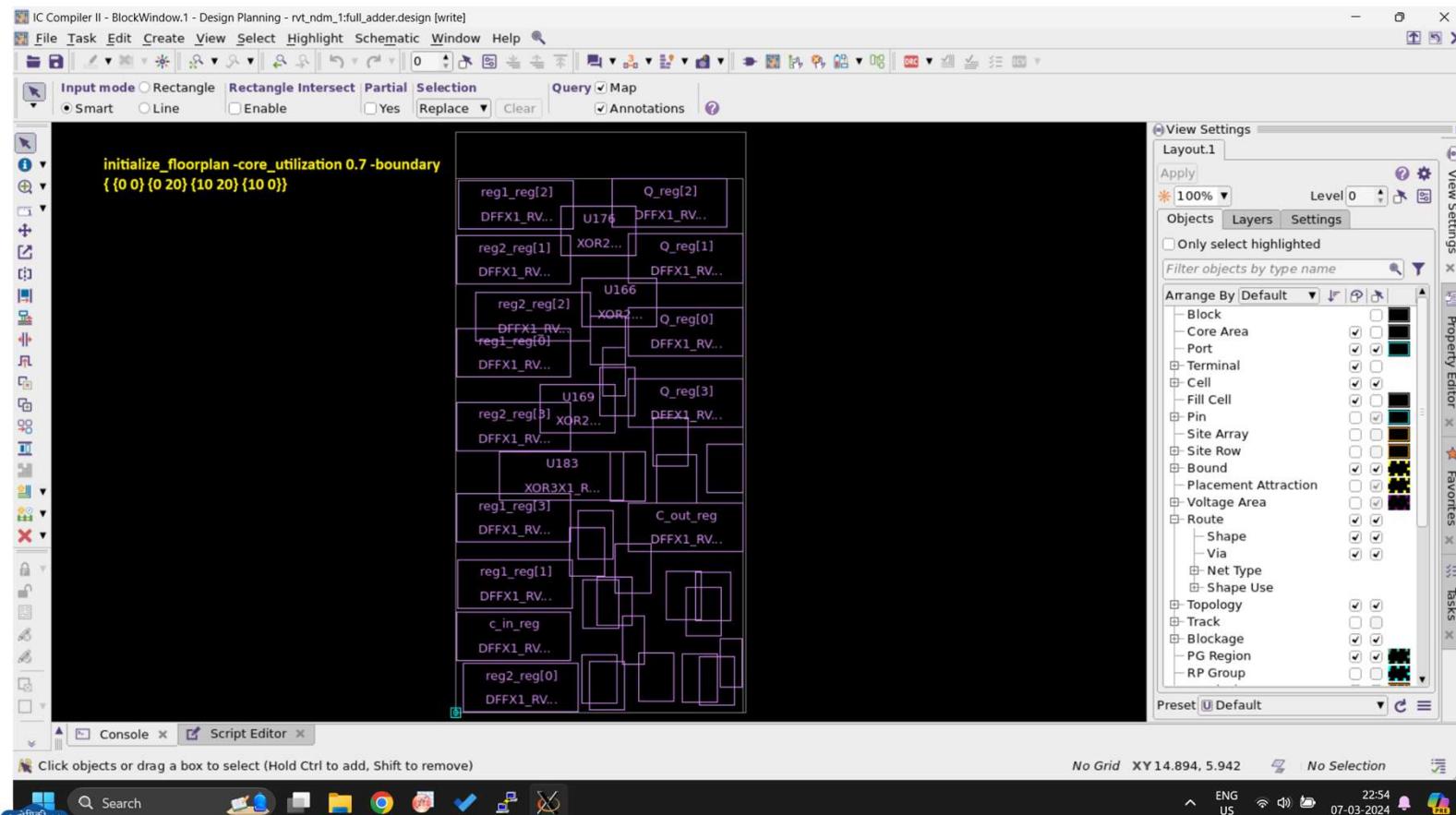
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ICC II

FLOOR PLANNING



DEFINING BY
BOUNDARY
COORDINATES

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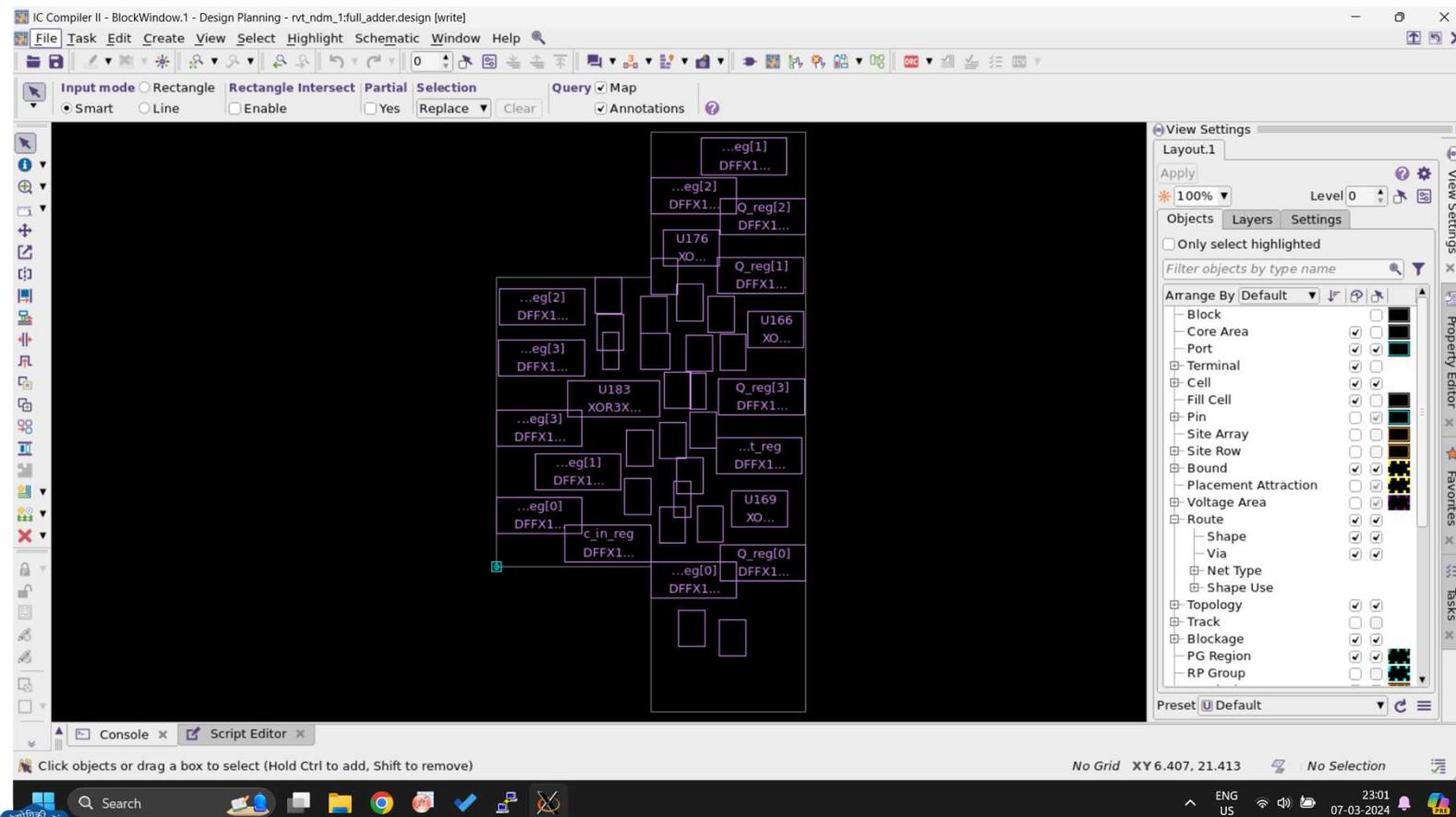
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ICC II

FLOOR PLANNING



FINAL
FLOORPLAN
FOR POWER
PLANNING

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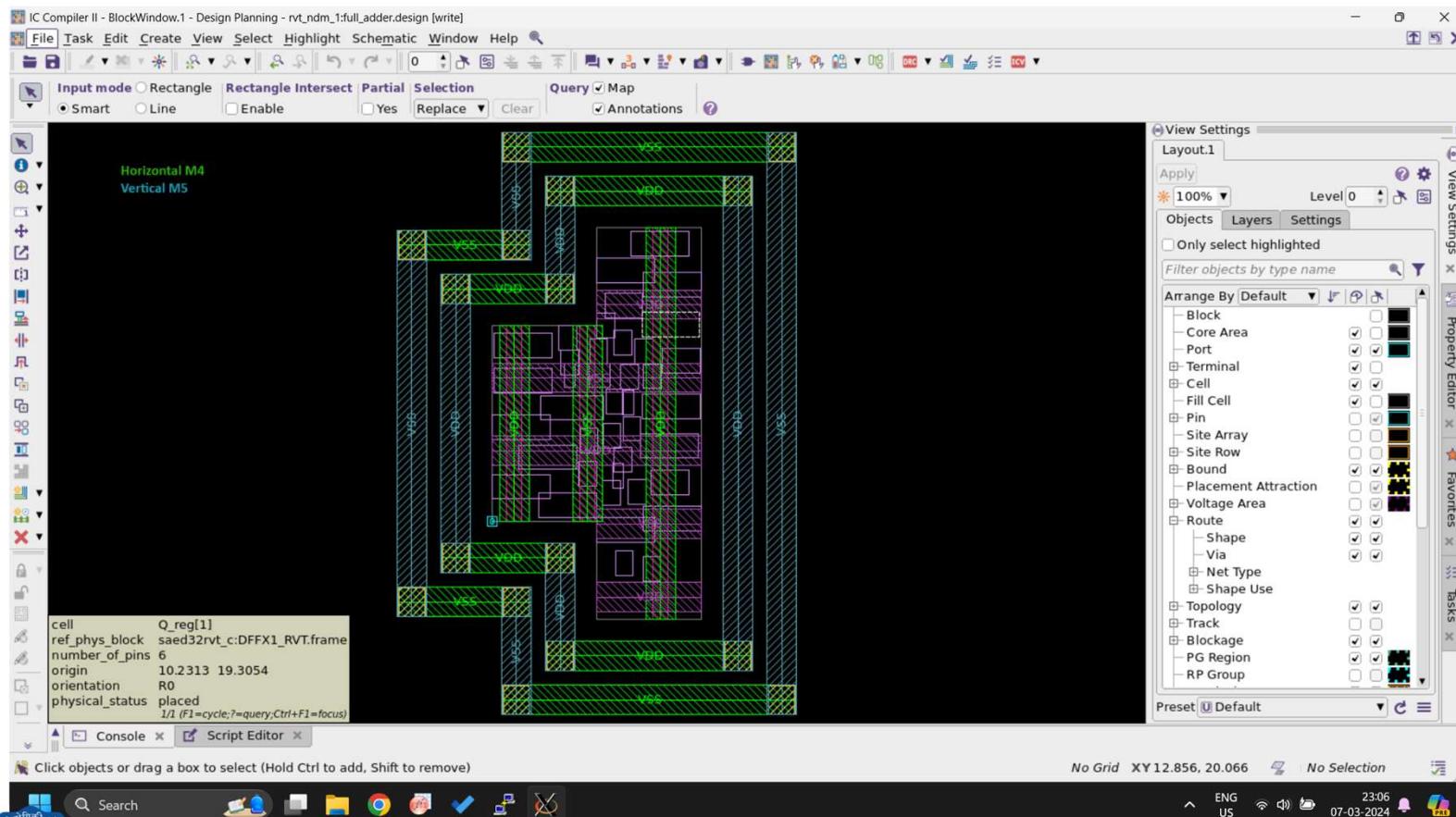
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ICC II

POWER PLANNING



CORE MESH
HORIZONTAL M4
VERTICAL M5

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ICC II

PLACEMENT

The image shows two terminal windows side-by-side. The left window displays the output of a chip routing script (icc2_shell). It provides detailed statistics about wire lengths across various layers (M1-M9, MRDL) and contact counts. The right window shows a TCL script for pin placement, which includes commands for setting models, corners, scenarios, and reading constraint files. Both windows are running on a Linux system with a standard desktop interface at the bottom.

```
ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/ICCI
```

Initial. Total Wire Length = 273.92
Initial. Layer M1 wire length = 49.72
Initial. Layer M2 wire length = 186.90
Initial. Layer M3 wire length = 20.28
Initial. Layer M4 wire length = 17.02
Initial. Layer M5 wire length = 0.00
Initial. Layer M6 wire length = 0.00
Initial. Layer M7 wire length = 0.00
Initial. Layer M8 wire length = 0.00
Initial. Layer M9 wire length = 0.00
Initial. Layer MRDL wire length = 0.00
Initial. Total Number of Contacts = 23
Initial. Via VIA12SQ_C count = 17
Initial. Via VIA23SQ_C count = 5
Initial. Via VIA34SQ_C count = 1
Initial. Via VIA45SQ_C count = 0
Initial. Via VIA56SQ_C count = 0
Initial. Via VIA67SQ_C count = 0
Initial. Via VIA78SQ_C count = 0
Initial. Via VIA89_C count = 0
Initial. Via VIA9RDL count = 0
Initial. completed.
[End of Whole Chip Routing] Elapsed real time: 0:00:00
[End of Whole Chip Routing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Whole Chip Routing] Stage (MB): Used 12 AllocTr 13 Proc 15
[End of Whole Chip Routing] Total (MB): Used 56 AllocTr 57 Proc 4511
[GR: Done] Elapsed real time: 0:00:00
[GR: Done] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[GR: Done] Stage (MB): Used 16 AllocTr 16 Proc 19
[GR: Done] Total (MB): Used 56 AllocTr 57 Proc 4511
Final total stats:
[End of Global Routing] Elapsed real time: 0:00:00
[End of Global Routing] Elapsed cpu time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Global Routing] Stage (MB): Used 8 AllocTr 8 Proc 19
[End of Global Routing] Total (MB): Used 48 AllocTr 48 Proc 4511
CPU Time for Global Route: 00:00:00.05u 00:00:00.06s 00:00:00.12e:
Number of block ports: 15
Number of block pin locations assigned from router: 15
CPU Time for Pin Preparation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Number of PG ports on blocks: 0
Number of pins created: 15
CPU Time for Pin Creation: 00:00:00.00u 00:00:00.00s 00:00:00.00e:
Total Pin Placement CPU Time: 00:00:00.05u 00:00:00.06s 00:00:00.13e:
Information: Ending 'place_pins' (FLW-8001)
Information: Time: 2024-03-07 23:30:42 / Session: 1.18 hr / Command: 0.00 hr / Memory: 549 MB (FLW-8100)
1
icc2_shell>

```
ws_ms2304102006_022@veo-1:~/VE/VE_o1/IIT_4FA_FF/ICCI
```

```
#mode func placement  
set model "func"  
set corner1 "nom"  
set scenario1 "${model}::${corner1}"  
remove_modes -all; remove_corners -all; remove_scenarios -all  
create mode $model  
create_corner $corner1  
create_scenario -name func::nom -mode func -corner nom  
current_mode func  
current_scenario func::nom  
source ../../CONSTRAINTS/full_adder.sdc  
set dont_use [get lib_cells */FADD*]  
set dont_use [get lib_cells */HADD*]  
set dont_use [get lib_cells */AO*]  
set dont_use [get lib cells */OA*]  
set dont_use [get lib cells */NAND*]  
set dont_use [get lib cells */XOR*]  
set dont_use [get lib cells */NOR*]  
set dont_use [get lib cells */XNOR*]  
set dont_use [get lib cells */MUX*]  
current corner nom  
current_scenario func::nom  
set parasitic1 "p1"  
set tluplus_file $parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmax.tluplus"  
set layer_map_file $parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"  
set parasitic2 "p2"  
set tluplus_file $parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmin.tluplus"  
set layer_map_file $parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"  
read_parasitic_tech -tlpu $tluplus_filep1 -layermap $layer_map_filep1 -name p1  
read_parasitic_tech -tlpu $tluplus_filep2 -layermap $layer_map_filep2 -name p2  
set_parasitic_parameters -late_spec $parasitic1 -early_spec $parasitic2  
set_app_options -name place.coarse.continue_on_missing_scandef -value true  
place_pins -self  
place_opt  
save_block -as full_adder_placement  
save lib  
"scripts/placement.tcl" 47L, 1472C
```

PIN PLACEMENT SCRIPT

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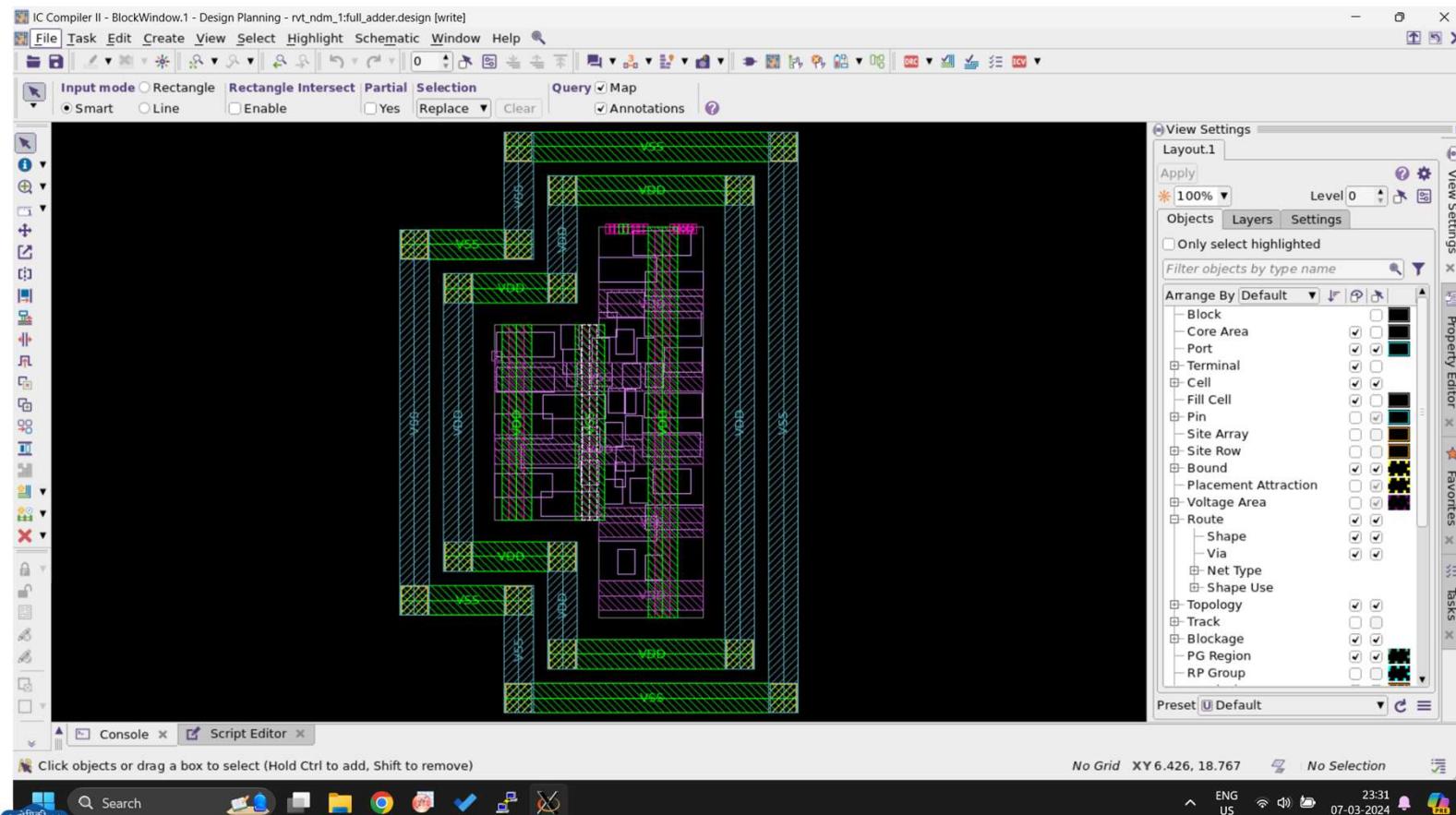
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ICC II

PLACEMENT



PIN PLACEMENT

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ICC II

PLACEMENT

The image shows two terminal windows side-by-side. The left window is titled 'ws_ms2304102006_022@veo-1:/VE/VE_o1/IIT_4FA_FF/ICCI' and contains Verilog code for an 'icc2_shell'. It includes commands like 'set parasitic1 "p2"', 'set tluplus_file\$p parasitic2 "PDK_PATH/tech/star_rcxt/saed32nm_ip9m_Cmin.tluplus"', and various 'read' commands for files such as 'ivm', 'lib_package', 'name_map', 'ocvm', 'parasitic_tech', 'physical_rules', and 'pin_constraints'. There are several error messages, notably about file paths and reading problems.

The right window is also titled 'ws_ms2304102006_022@veo-1:/VE/VE_o1/IIT_4FA_FF/ICCI' and contains Verilog code for 'mode func placement'. It includes commands like 'set model "func"', 'set corner1 "nom"', 'create mode \$model', 'create_corner \$corner1', and 'source ./CONSTRAINTS/full_adder.sdc'. It also lists 'set dont_use' entries for various logic cells like FADD, HADD, AO, OA, NAND, NOR, XOR, XNOR, and MUX. The code ends with 'place_pins -self' and 'scripts/placement.tcl'.

SOME ERRORS TO
BE RECTIFIED
DURING
PLACEMENT

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ICC II

PLACEMENT

The image shows two terminal windows side-by-side. The left window displays Verilog code for a full adder, including module definitions, port declarations, and logic assignments. The right window shows a command-line interface for the ICC II placement tool, with commands like 'set tluplus file\$parasitic1' and 'set layer_map_file\$parasitic1'. Both windows have a dark background with white text.

```
p1
icc2_shell> set tluplus file$parasitic1 "PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmax.tluplus"
PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmax.tluplus
icc2_shell> set layer_map_file$parasitic1 "PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map
icc2_shell> set parasitic2 "p2"
p2
icc2_shell> set tluplus file$parasitic2 "PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmin.tluplus"
PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmin.tluplus
icc2_shell> set layer_map_file$parasitic2 "PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"
PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map
icc2_shell> read_
read_aif          read_ivm          read_rde
read_app_options  read_lib_package  read_saf
read_block_connection_file  read_name_map  read_sdc
read_cell_expansion    read_net_estimation_rules  read_signal_em_constraints
read_def           read_ocvm         read_tech_file
read_design_io     read_parasitic_tech   read_tech_lef
read_dff_connections  read_parasitics  read_verilog
read_drc_error_file  read_physical_rules  read_verilog_outline
read_feature_tables  read_pin_constraints  read_virtual_pad_file
icc2_shell> read_para
read_parasitic_tech  read_parasitics
icc2_shell> read_parasitic_tech -tlup $tluplus filep1 -layermap $layer_map_filep1 -name p1
Error: File 'PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map' cannot be found using search
_path of: '...'. (FILE-002)
Error: Unable to open file 'PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map' for reading;
layer map file read problem (FILE-001)
icc2_shell> read_parasitic_tech -tlup $tluplus filep1 -layermap $layer_map_filep1 -name p1
Error: File 'PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map' cannot be found using search
_path of: '...'. (FILE-002)
Error: Unable to open file 'PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map' for reading;
layer map file read problem (FILE-001)
icc2_shell> read_parasitic_tech -tlup $tluplus filep2 -layermap $layer_map_filep2 -name p2
Error: File 'PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map' cannot be found using search
_path of: '...'. (FILE-002)
Error: Unable to open file 'PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map' for reading;
layer map file read problem (FILE-001)
icc2_shell> set_parasitic_parameters -late_spec $parasitic1 -early_spec $parasitic2
Error: cant find parasitic spec p1
Error: cant find parasitic spec p2
Error: 0
  Use error_info for more info. (CMD-013)
icc2_shell> set_app_options -name place.course.continue_on_missing_scandef -value true
Error: Invalid option name 'place.course.continue_on_missing_scandef'
  Use error info for more info. (CMD-013)
icc2_shell>

1,1      All
ENG US  23:30  07-03-2024
```

```
mode for placement
set model "func"
set corner1 "nom"
set scenario1 "${model}::${corner1}"
remove_modes -all; remove_corners -all; remove_scenarios -all
create mode $model
create_corner $corner1
Create_scenario -name func::nom -mode func -corner nom
current_mode func
current_scenario func::nom

source ../../CONSTRAINTS/full_adder.sdc

set dont_use [get lib cells */FADD*]
set dont_use [get lib cells */HADD*]
set dont_use [get lib cells */AO*]
set dont_use [get lib cells */OA*]
set dont_use [get lib cells */NAND*]
set dont_use [get lib cells */XOR*]
set dont_use [get lib cells */NOR*]
set dont_use [get lib cells */XNOR*]
set dont_use [get lib cells */MUX*]

current corner nom
current_scenario func::nom

set parasitic1 "p1"
set tluplus file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmax.tluplus"
set layer_map_file$parasitic1 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"

set parasitic2 "p2"
set tluplus file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_lp9m_Cmin.tluplus"
set layer_map_file$parasitic2 "$PDK_PATH/tech/star_rcxt/saed32nm_tf_itf_tluplus.map"

read_parasitic_tech -tlup $tluplus filep1 -layermap $layer_map_filep1 -name p1
read_parasitic_tech -tlup $tluplus filep2 -layermap $layer_map_filep2 -name p2

set_parasitic_parameters -late_spec $parasitic1 -early_spec $parasitic2
set_app_options -name place.coarse.continue_on_missing_scandef -value true

place_pins -self
place_opt

save_block -as full_adder_placement
save lib
"scripts/placement.tcl" 47L, 1472C
```

SOME MORE !!!

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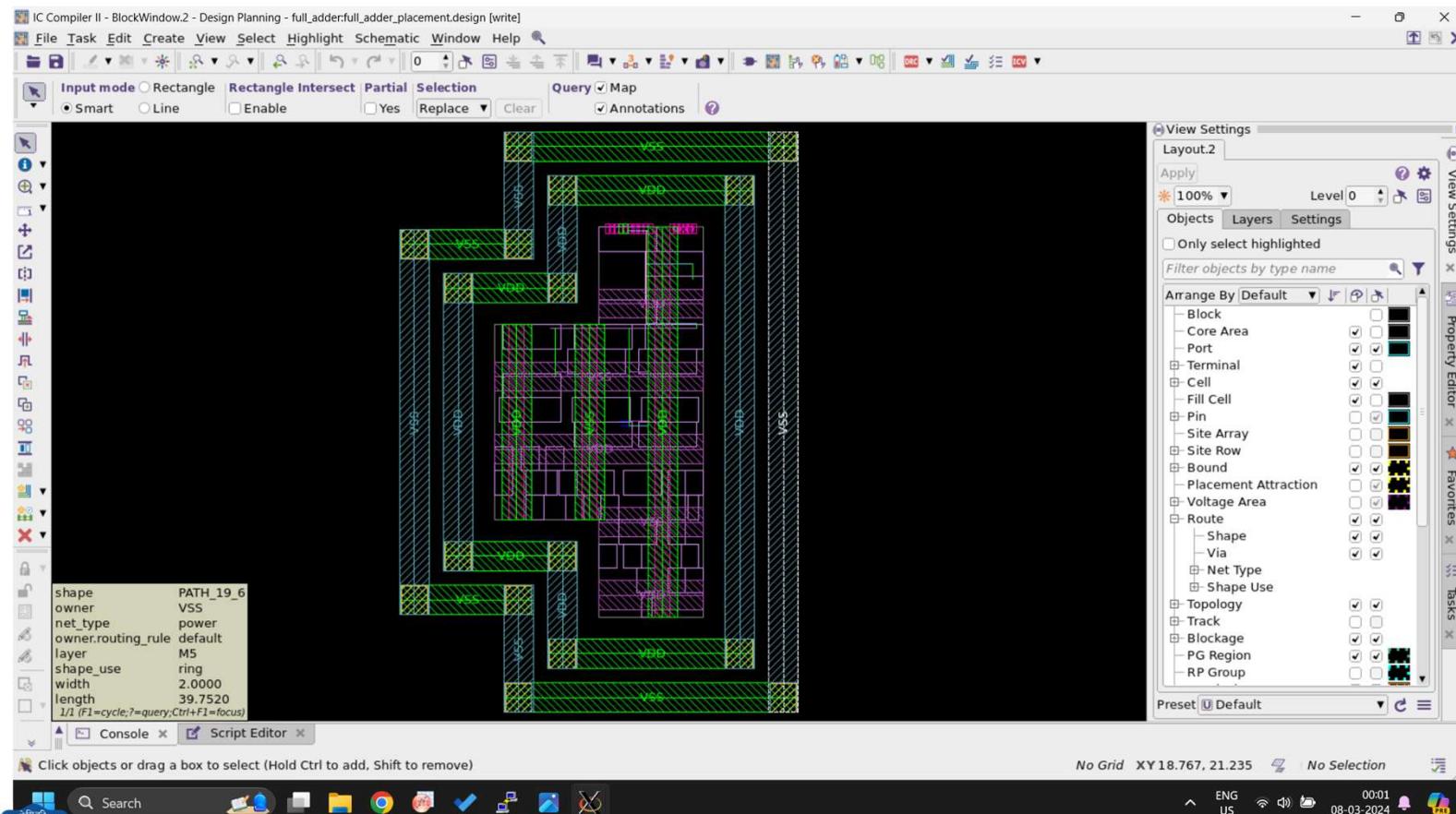
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ICC II

CLOCK SYNTHESIS



synthesizeClockTree

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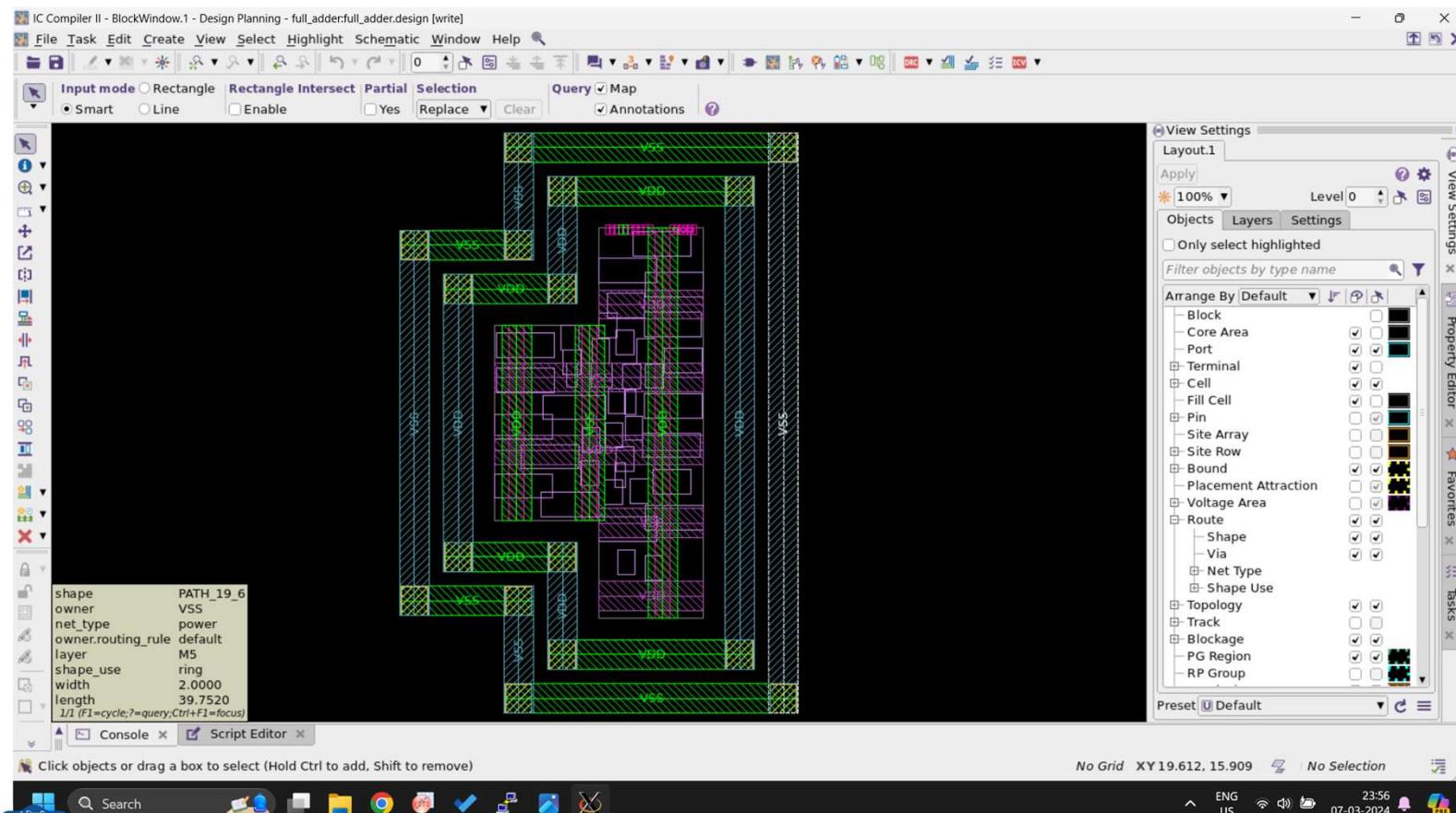
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ICC II

CLOCK SYNTHESIS



pinPlace

Submitted by

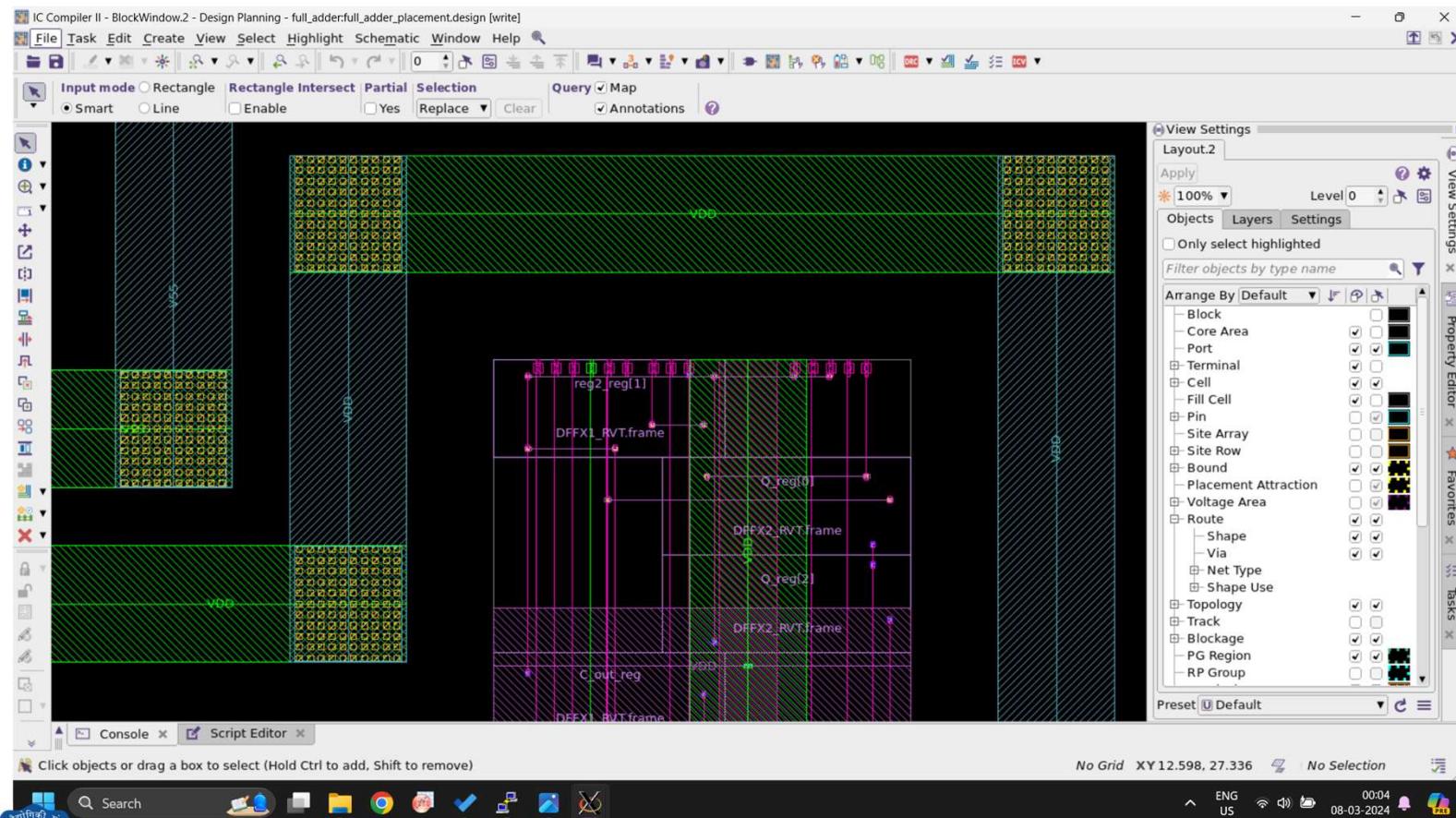
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ICC II

CLOCK SYNTHESIS



pins and clock
routing

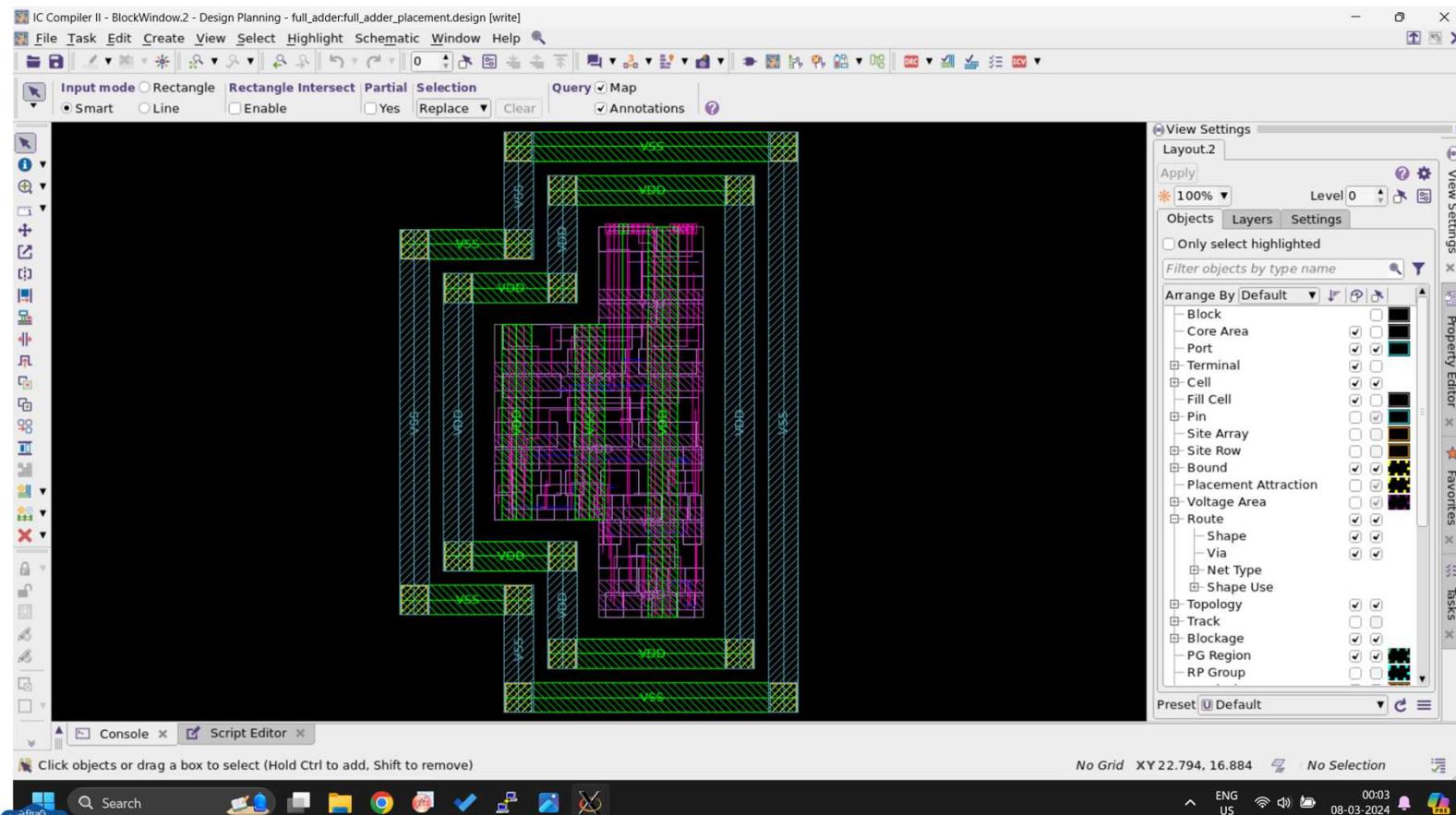
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ICC II

CLOCK SYNTHESIS



clock_opt -from
final_opto

Submitted by

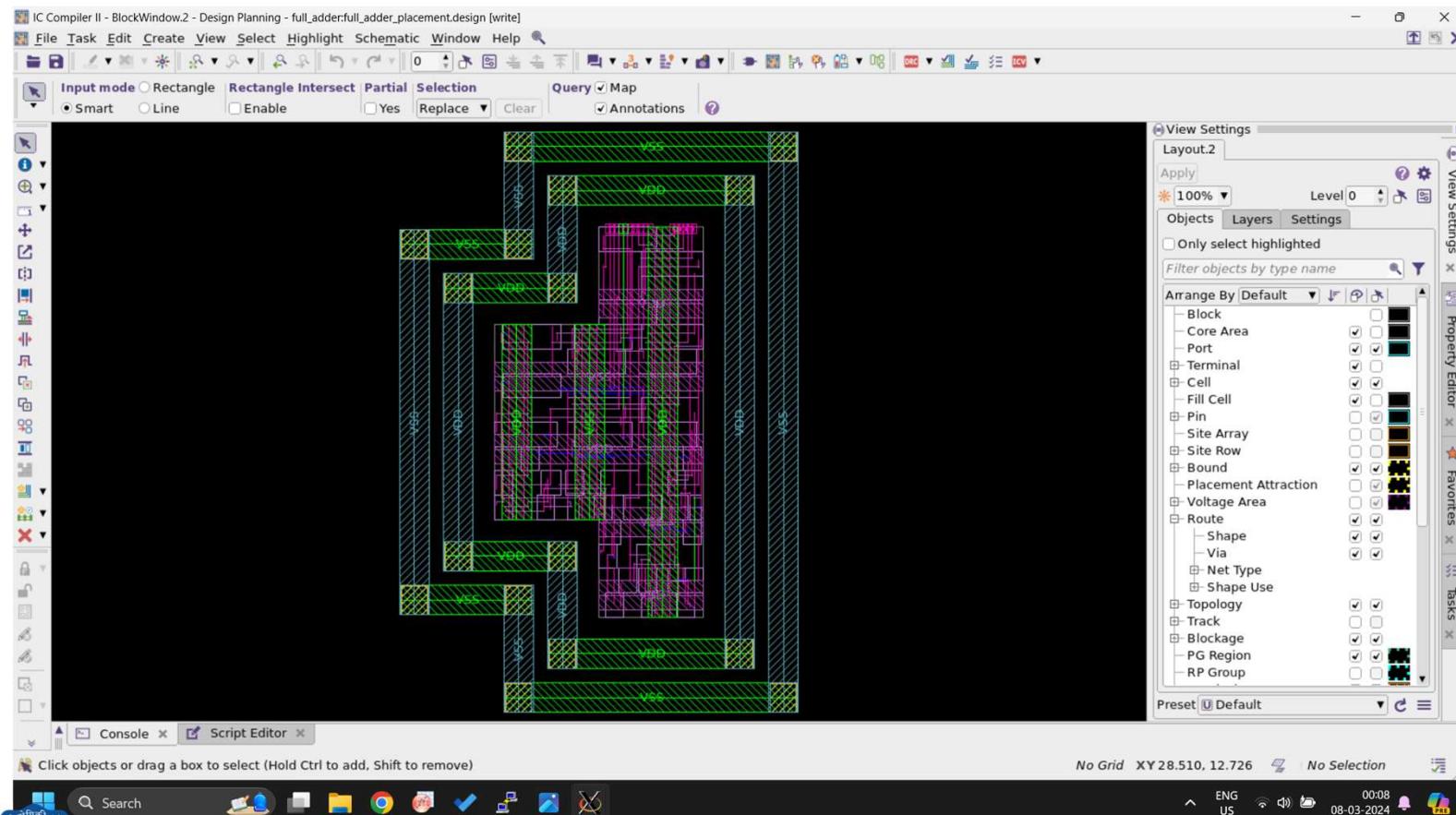
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ICC II

DATA ROUTING



route_track

Submitted by

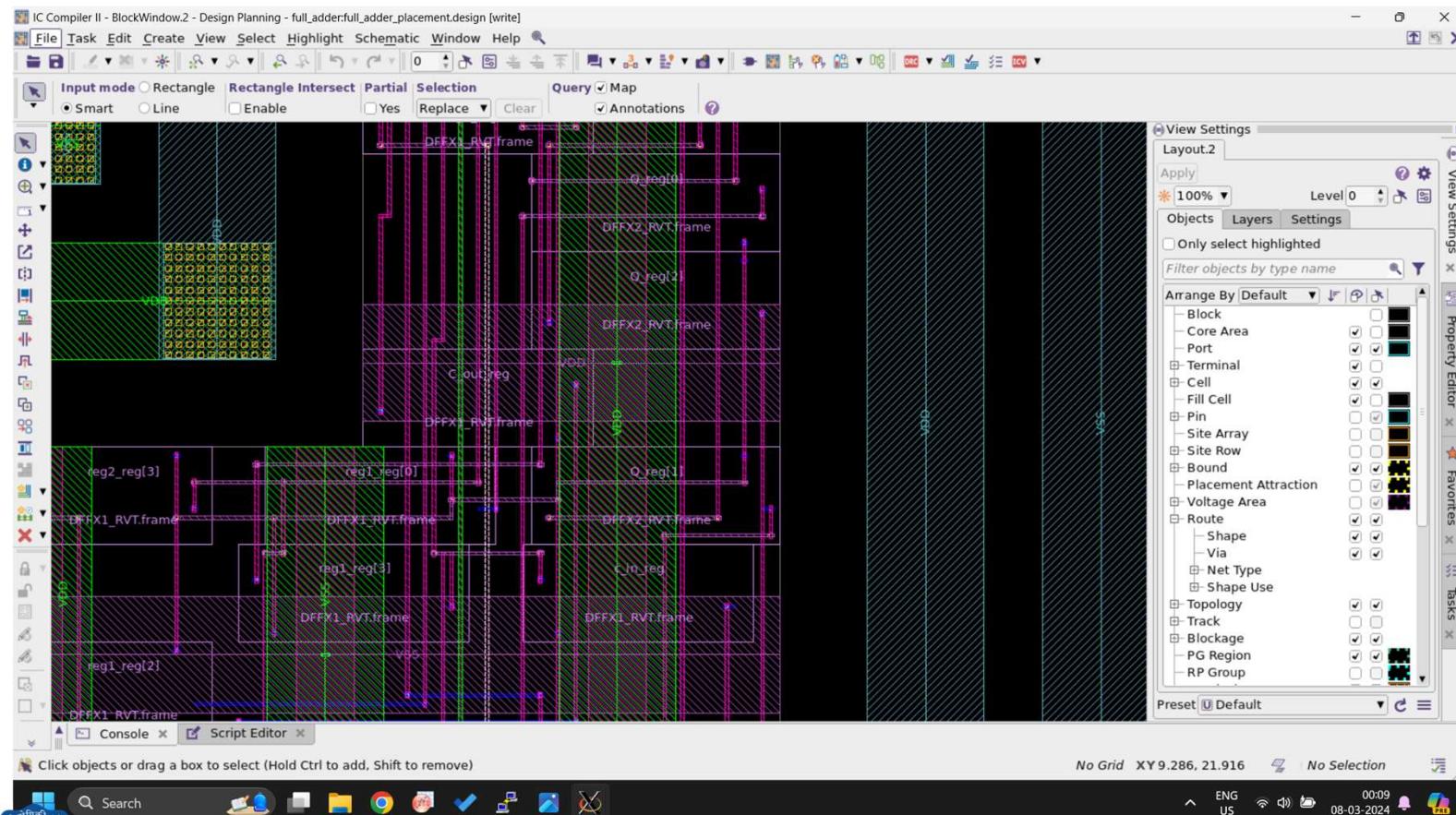
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ICC II

DATA ROUTING



route_track

Submitted by

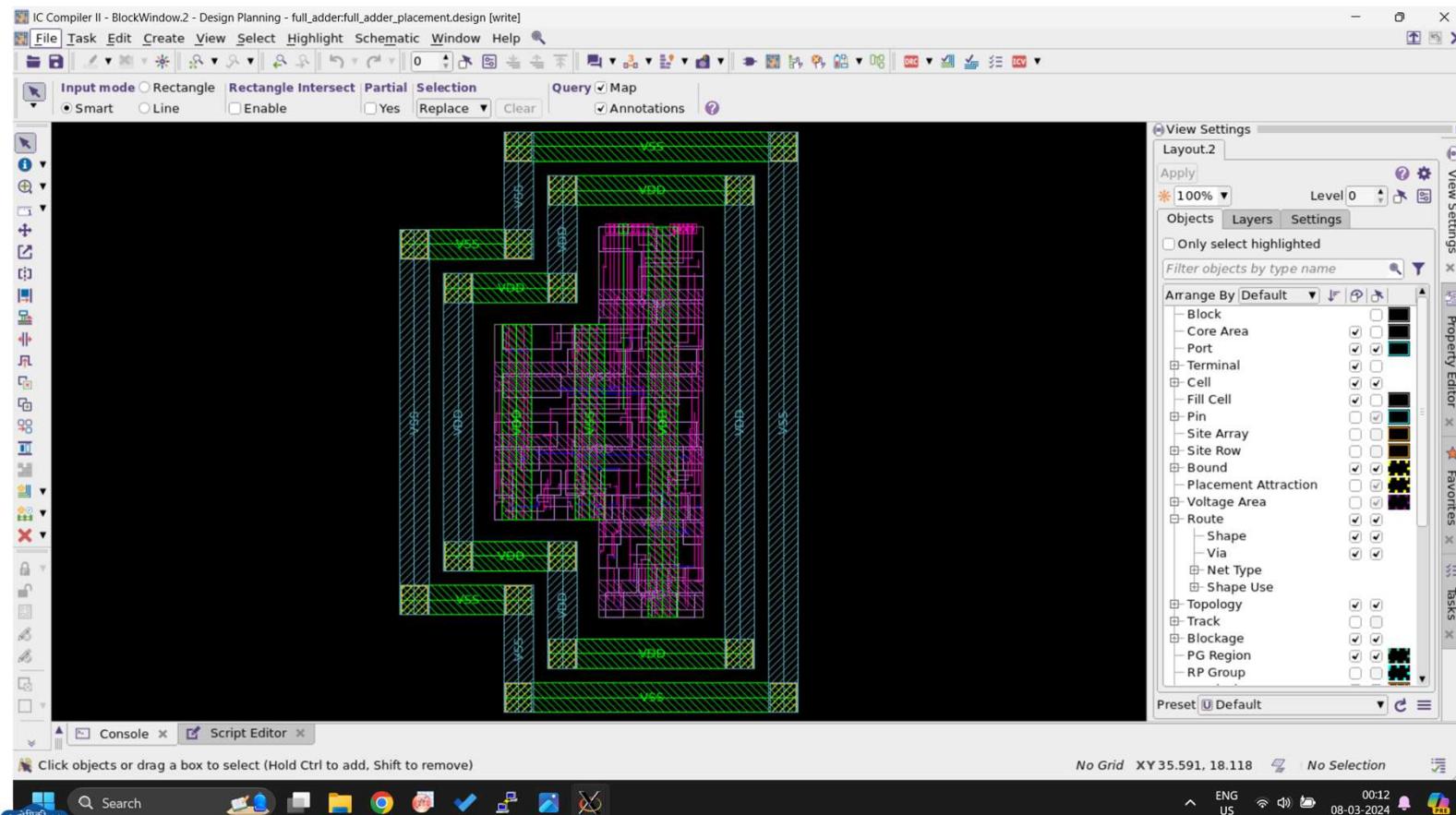
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ICC II

DATA ROUTING



route_global

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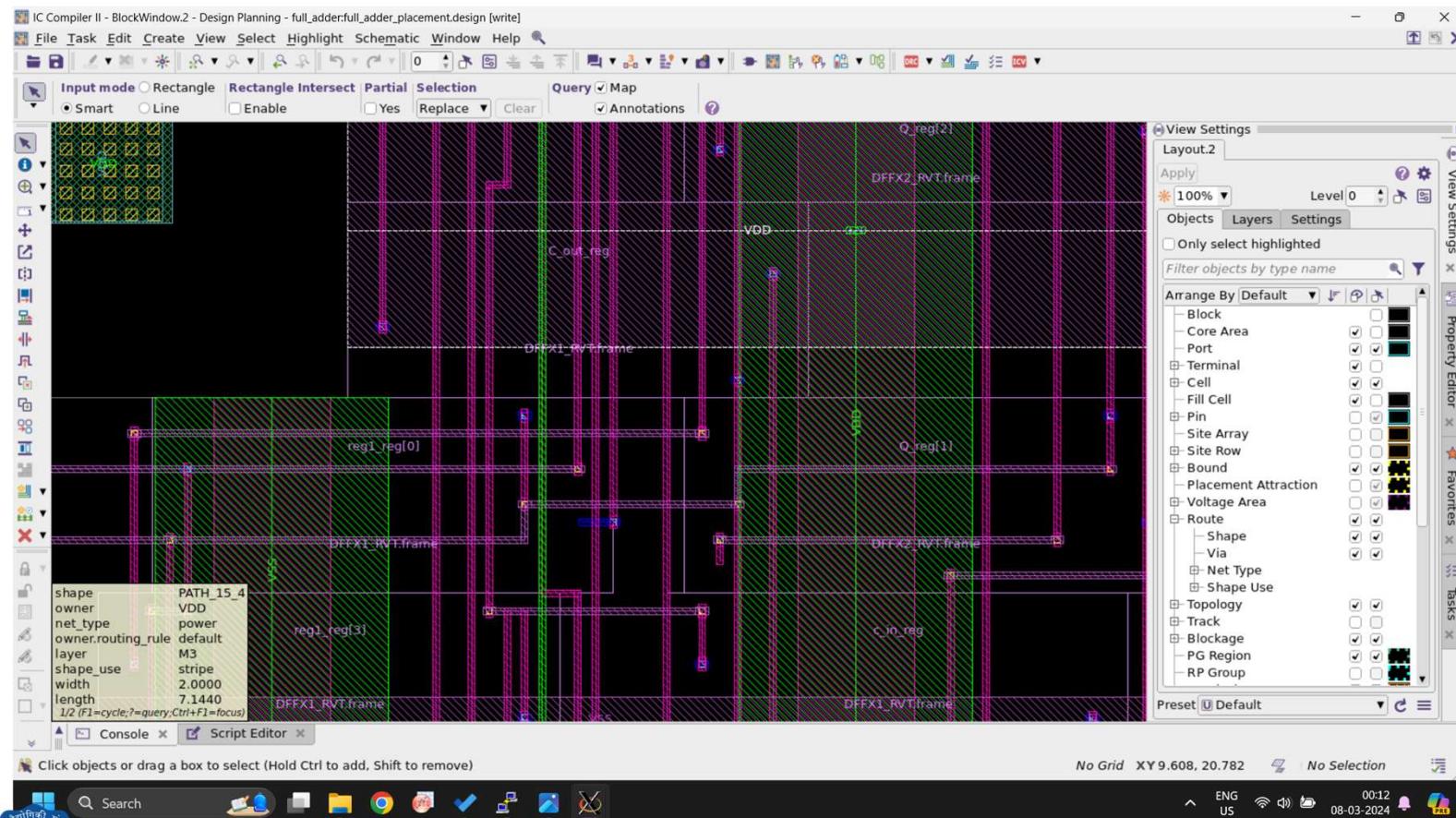
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ICC II

DATA ROUTING



route_global

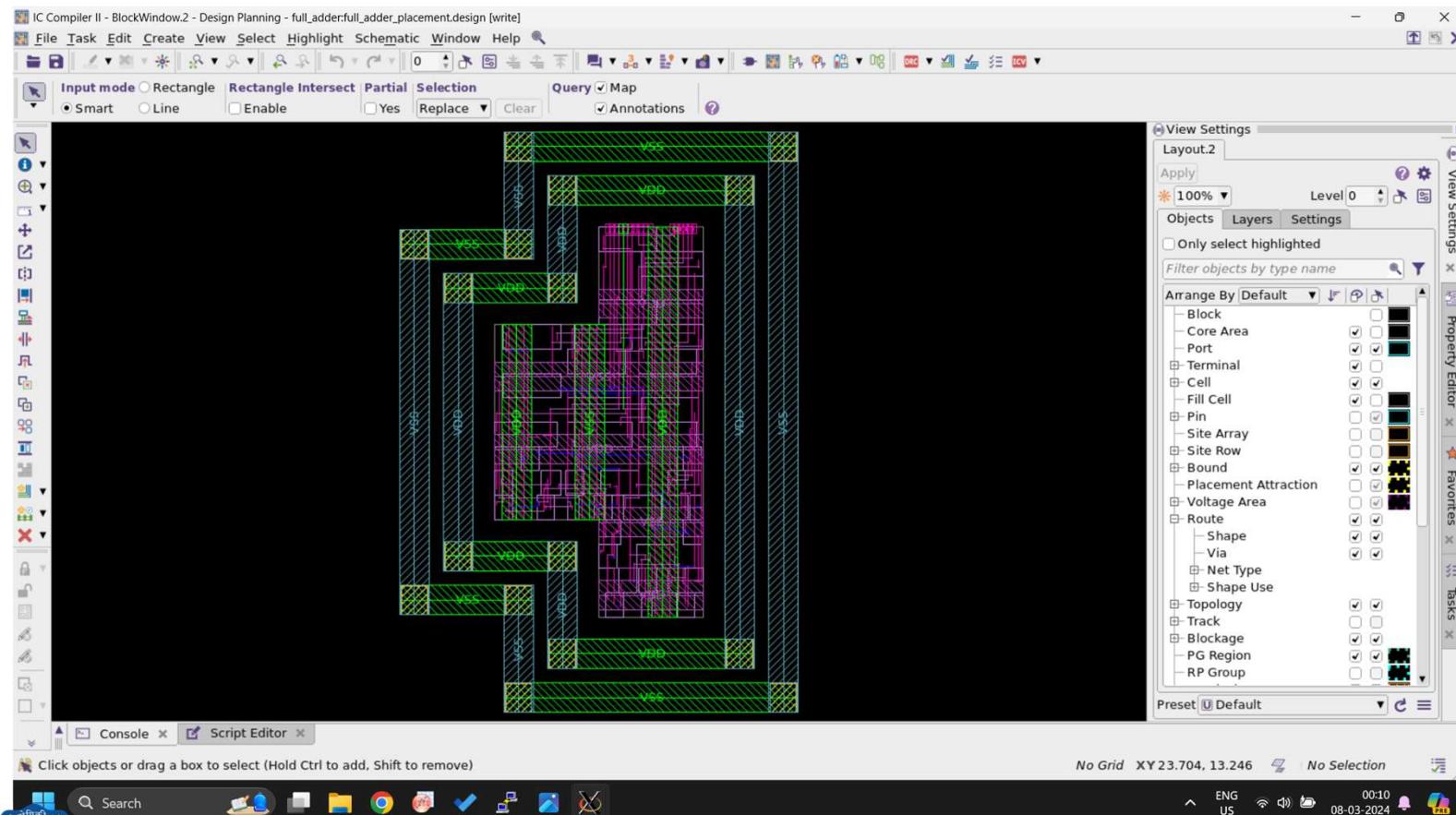
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ICC II

DATA ROUTING



route_detail

Submitted by

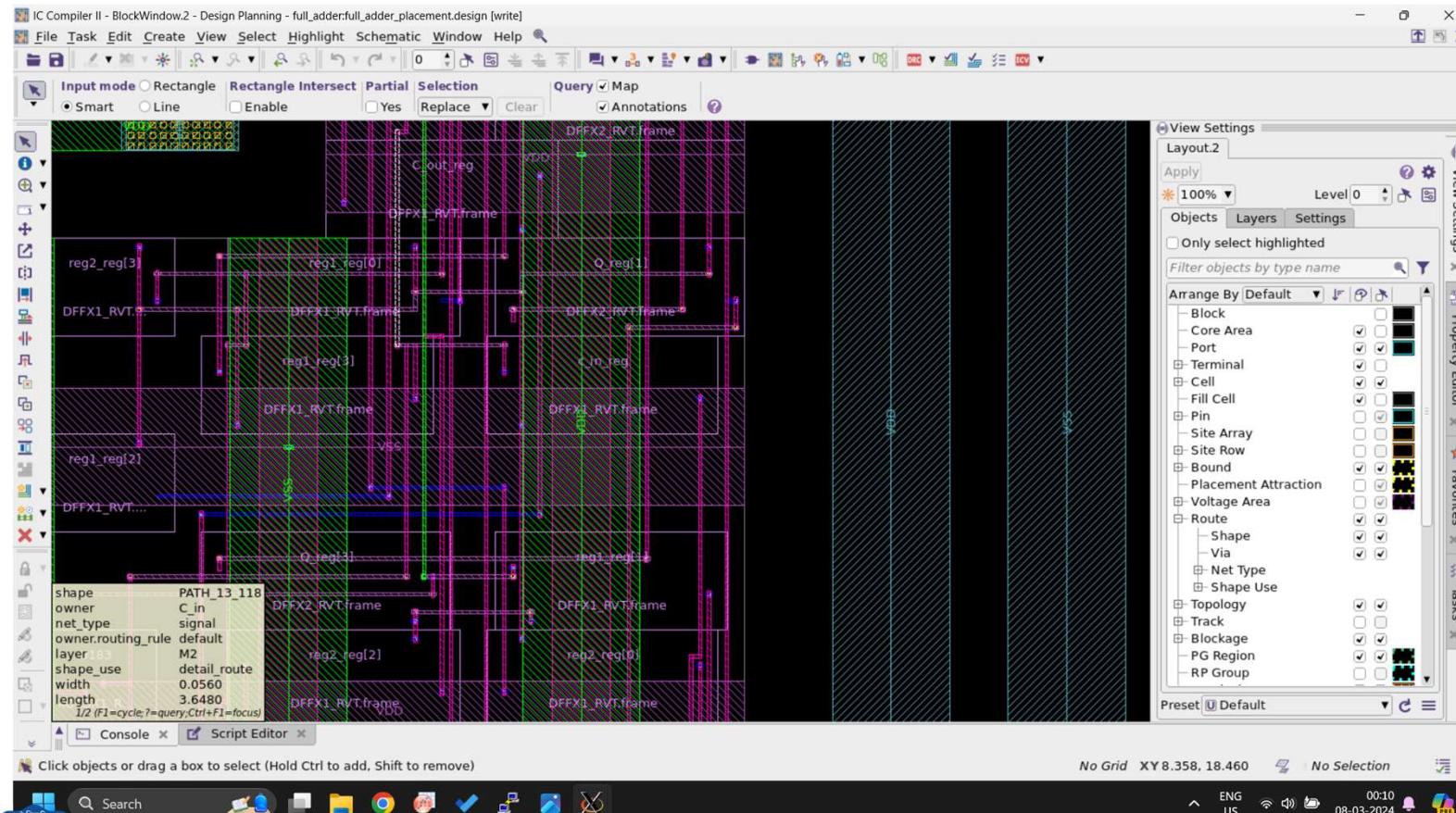
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ICC II

DATA ROUTING



route_detail

Submitted by

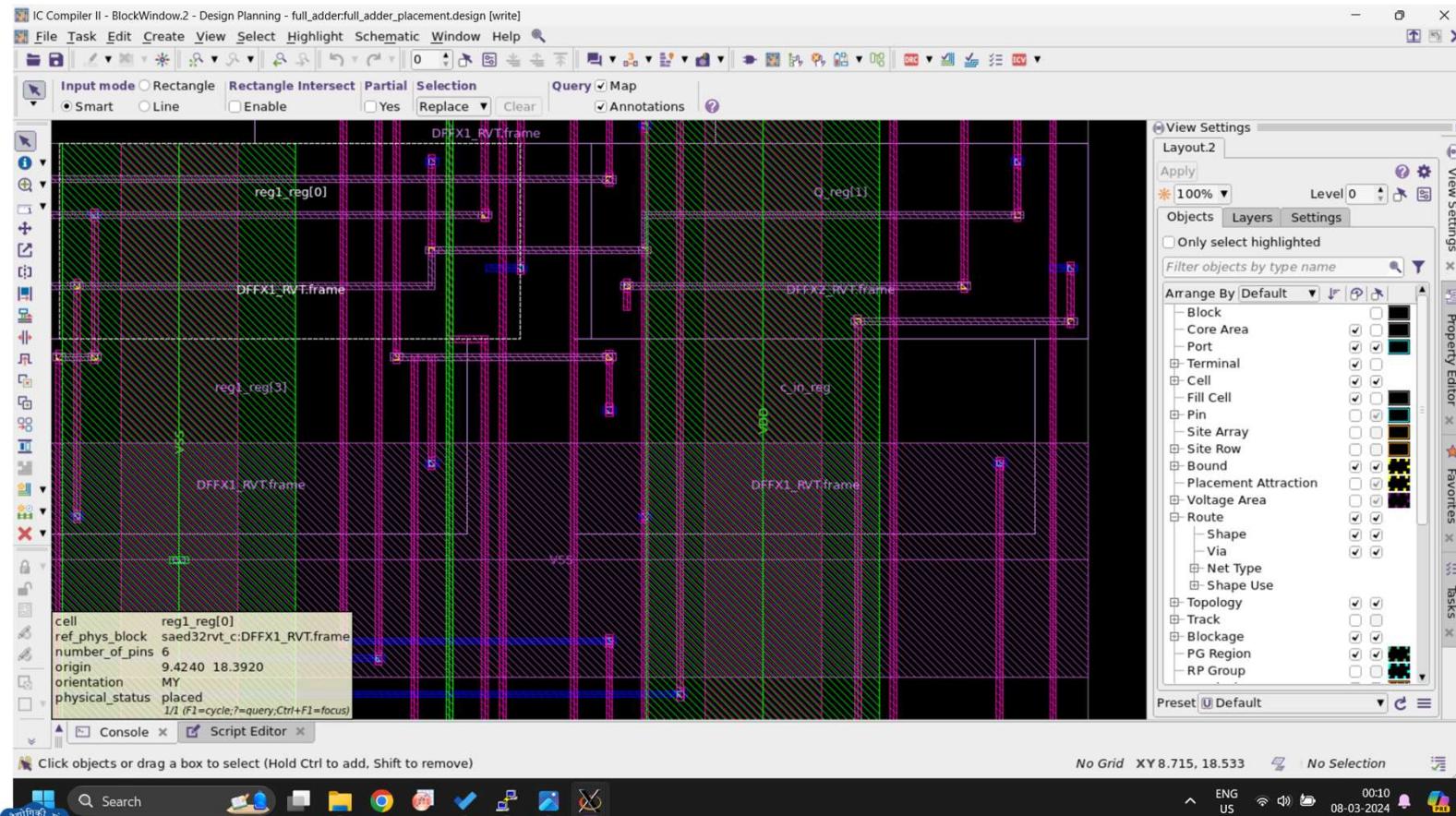
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ICC II

DATA ROUTING



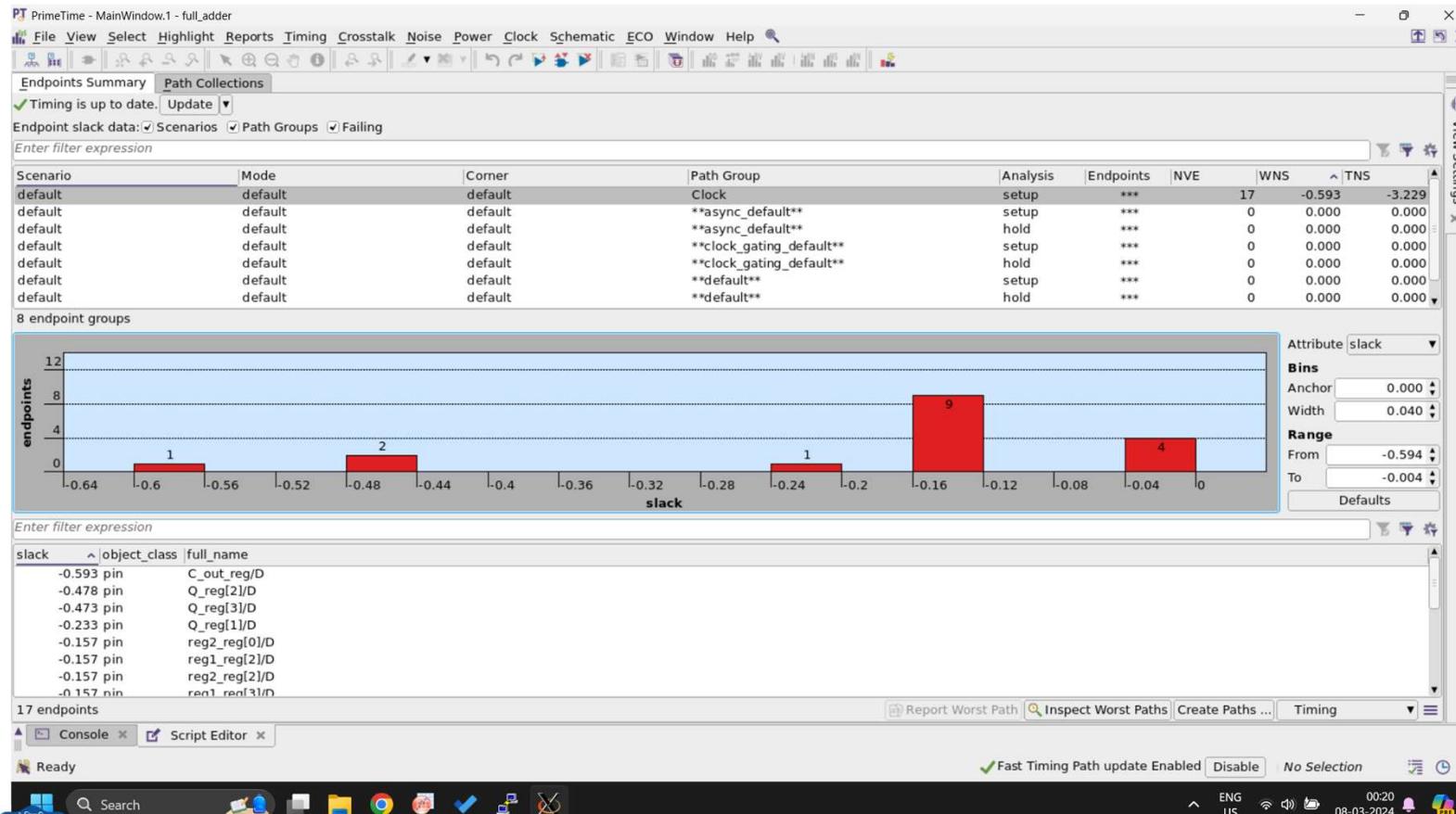
route_detail

Submitted by

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PRIME TIME



TYPICAL TIMING
REPORT

Submitted by

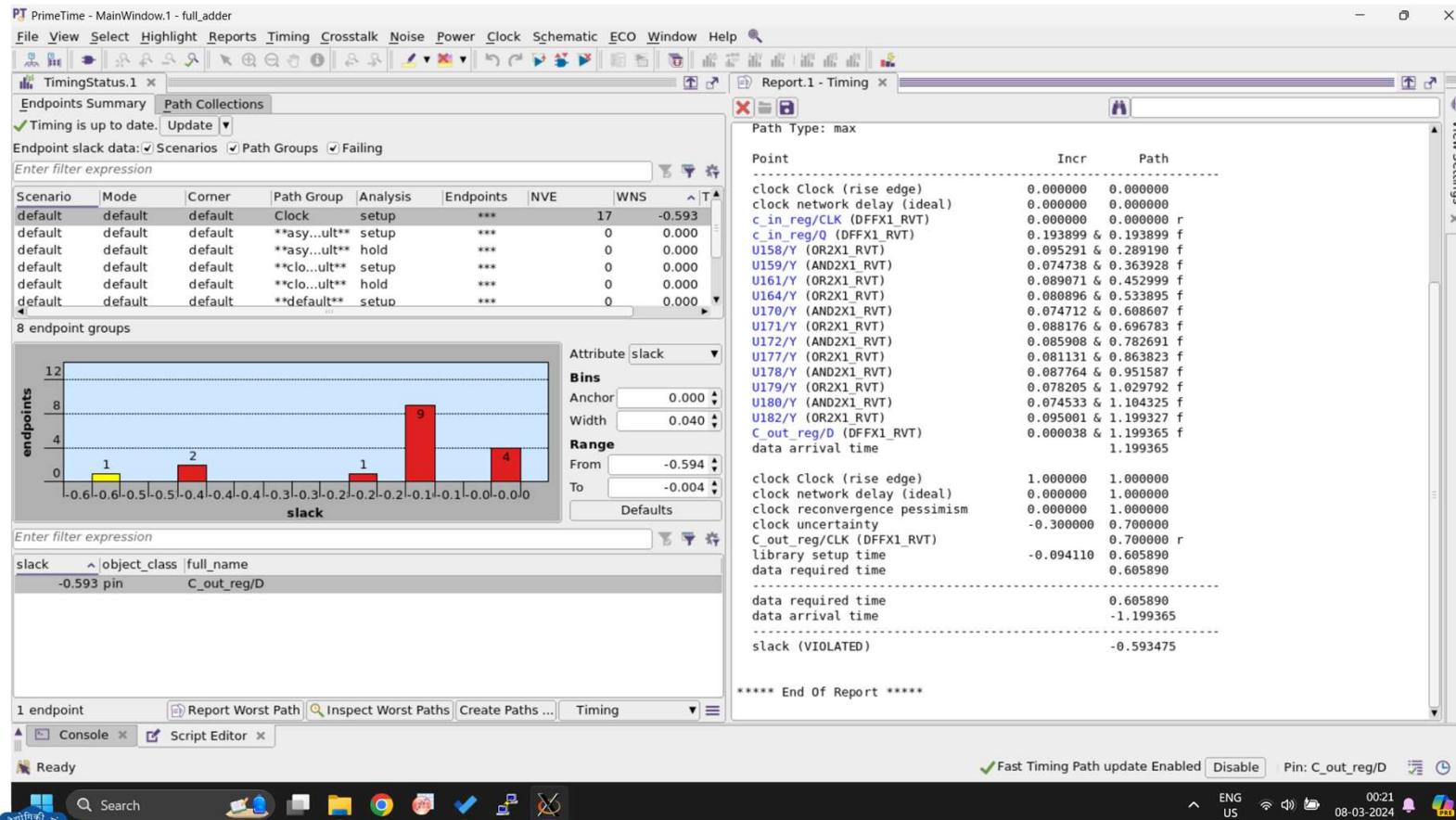
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PRIME TIME



TYPICAL worst
TIMING REPORT

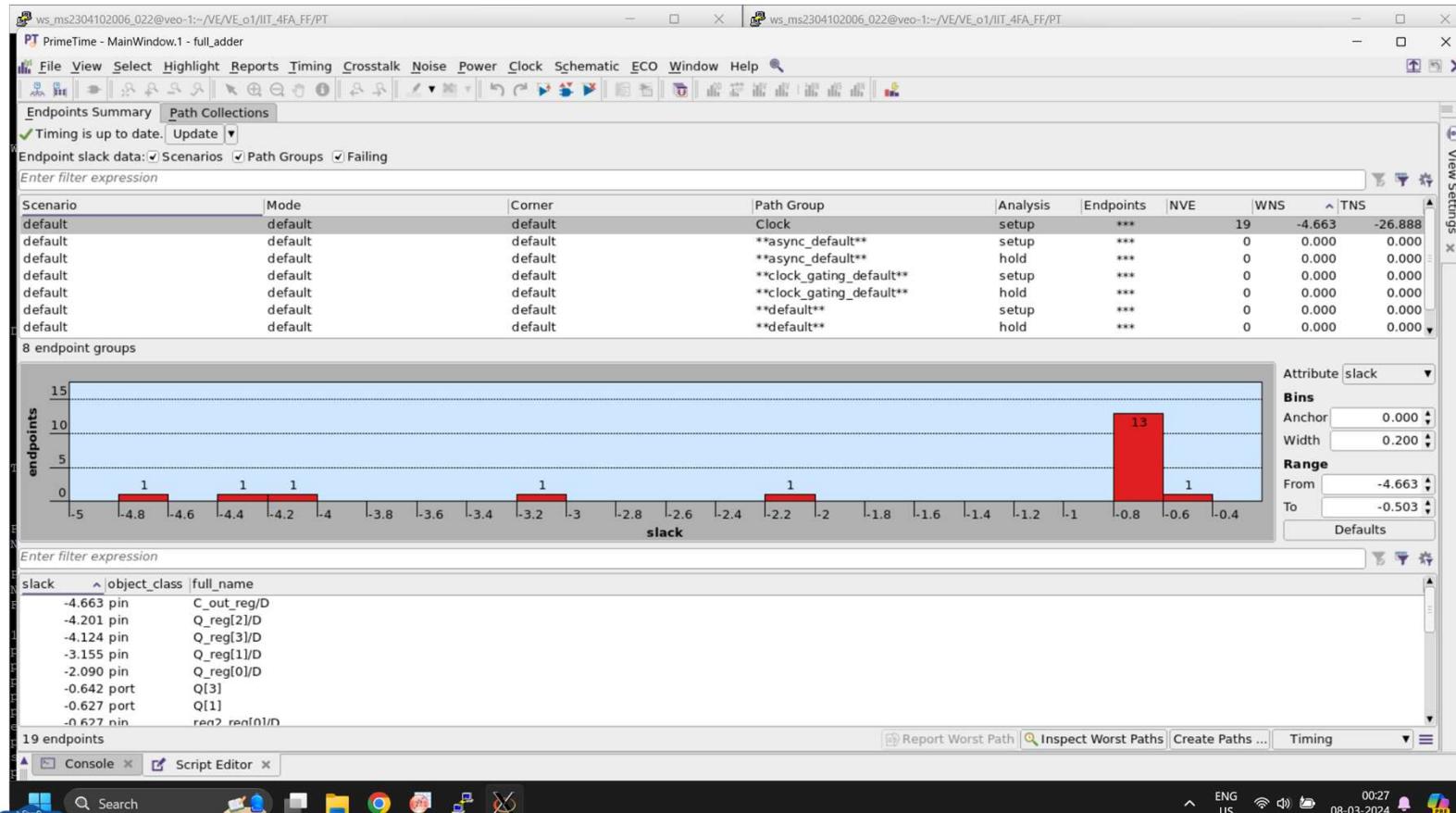
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PRIME TIME



TIMING REPORT
considering
PARASITIC P1

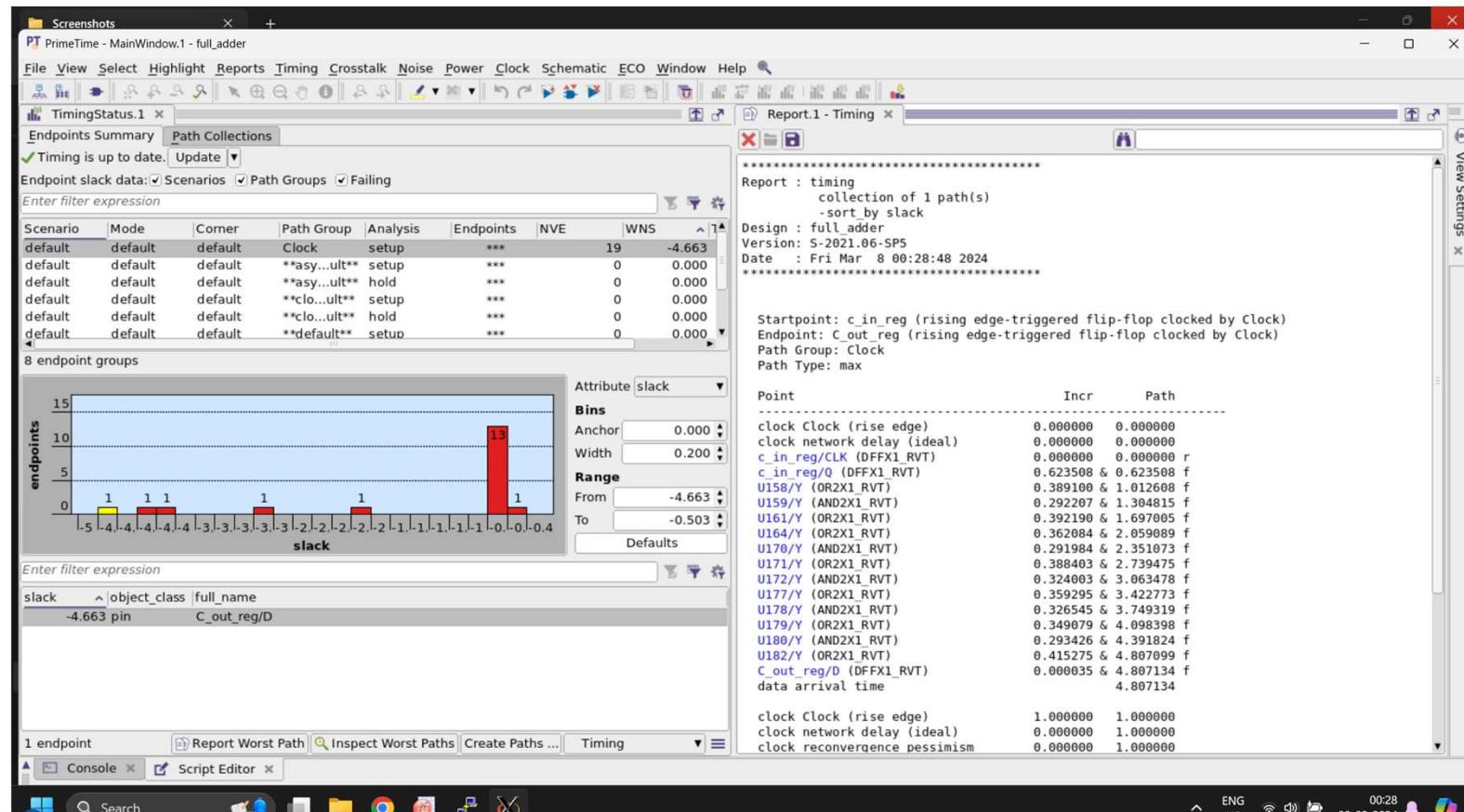
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PRIME TIME



TIMING (worst)
REPORT considering
PARASITIC P1

Submitted by

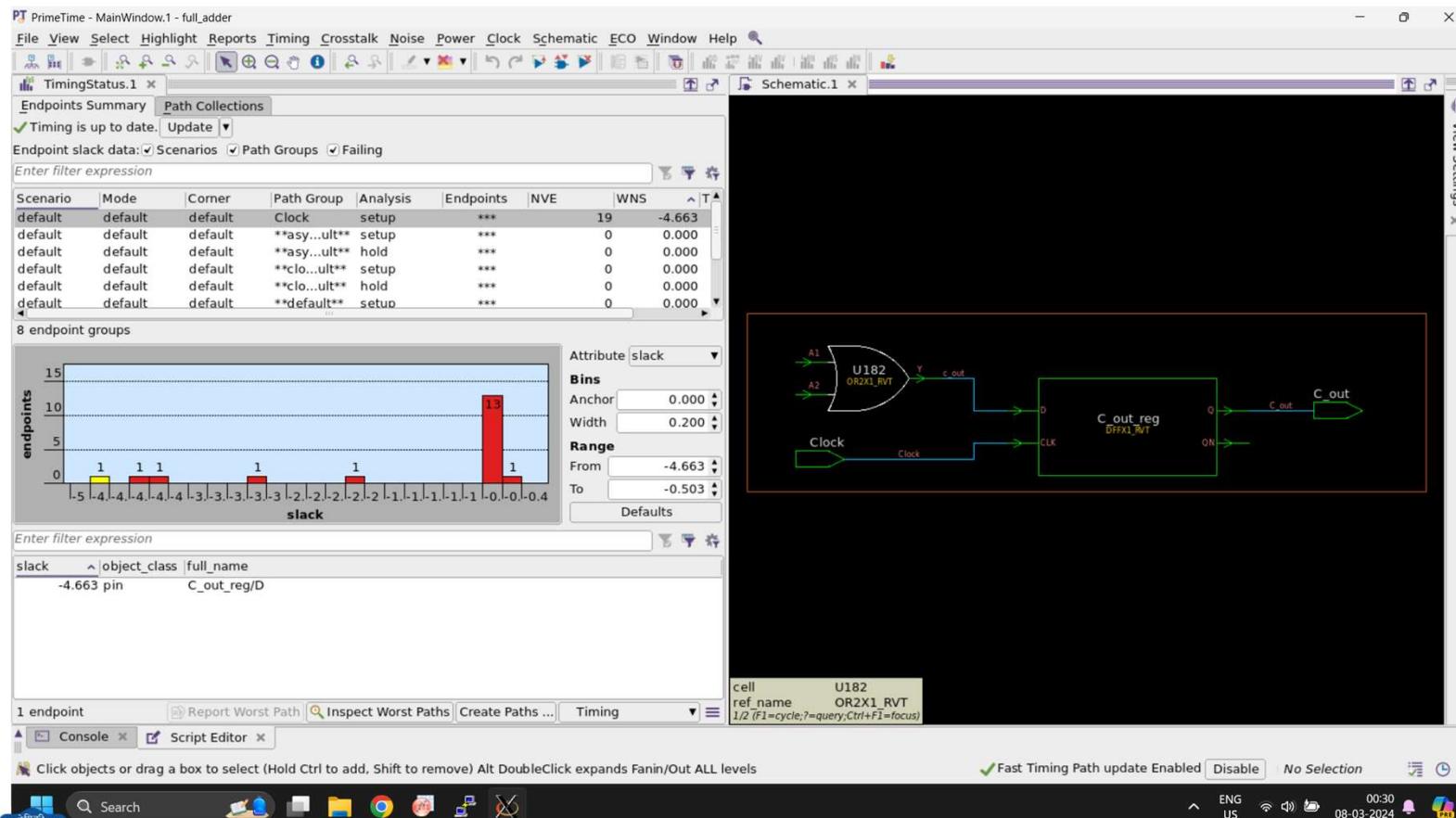
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PRIME TIME



TIMING (worst) PATH
considering
PARASITIC P1

Submitted by

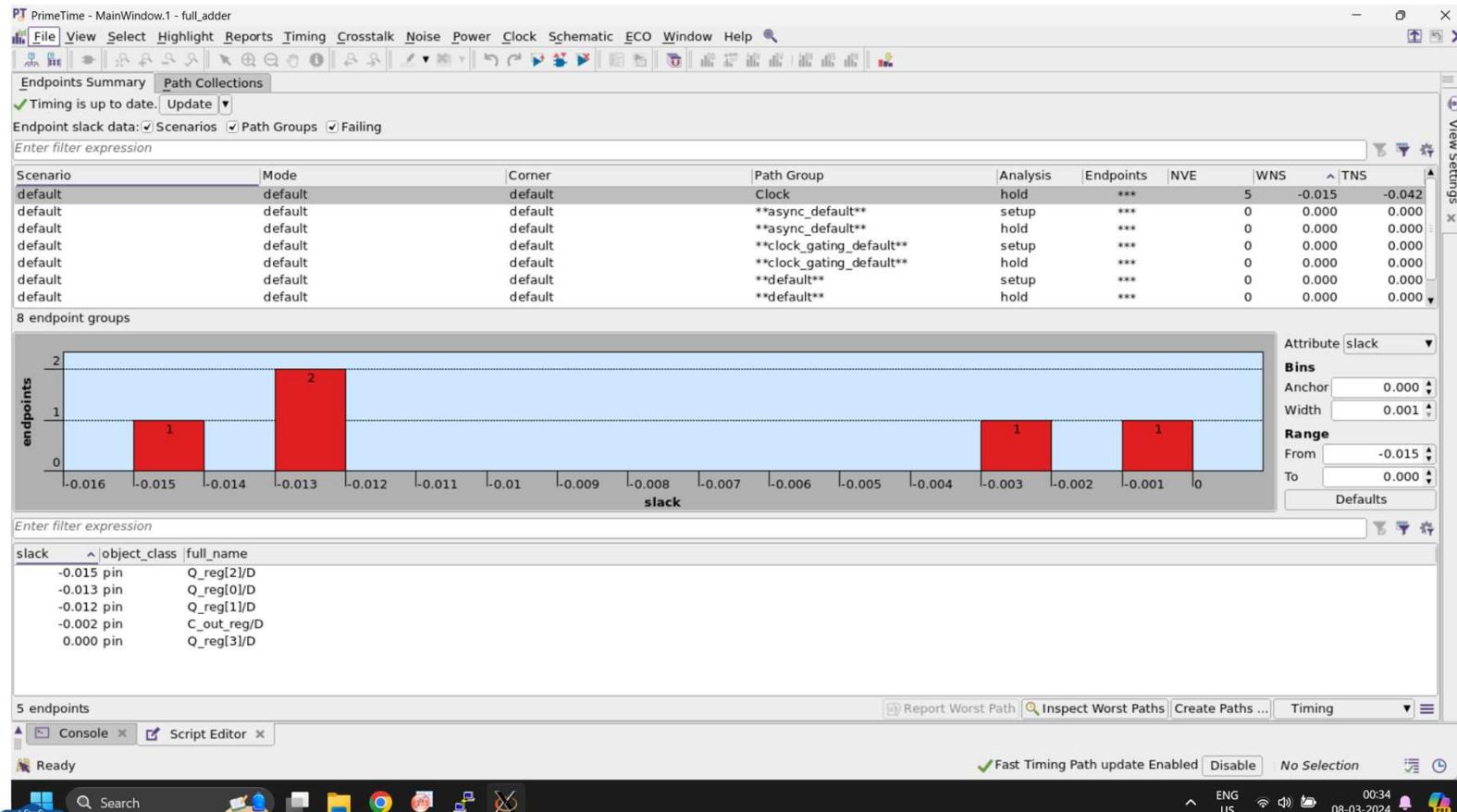
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PRIME TIME

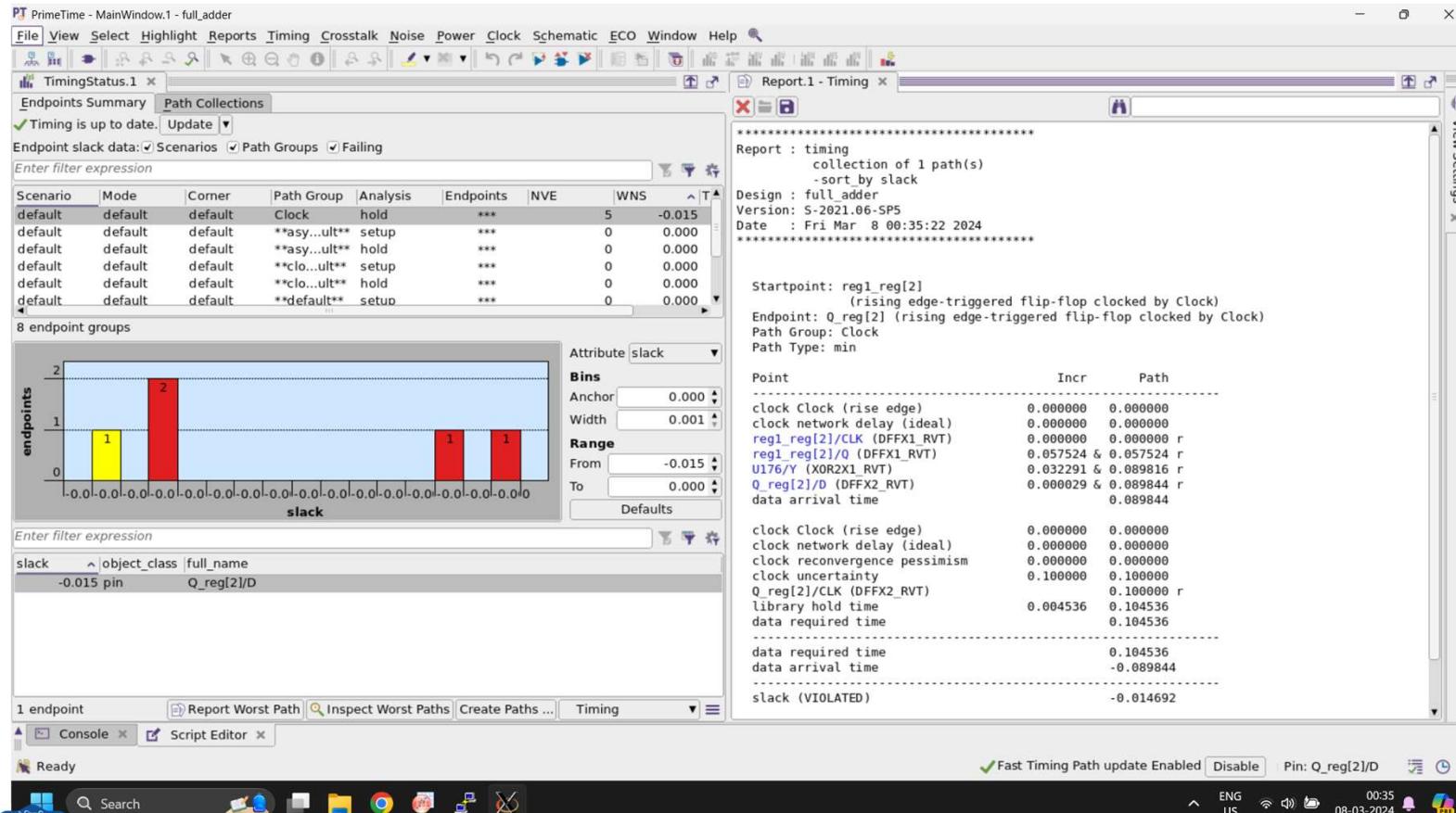


TIMING REPORT
considering
PARASITIC P2

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PRIME TIME



TIMING (worst)
REPORT considering
PARASITIC P2

Submitted by

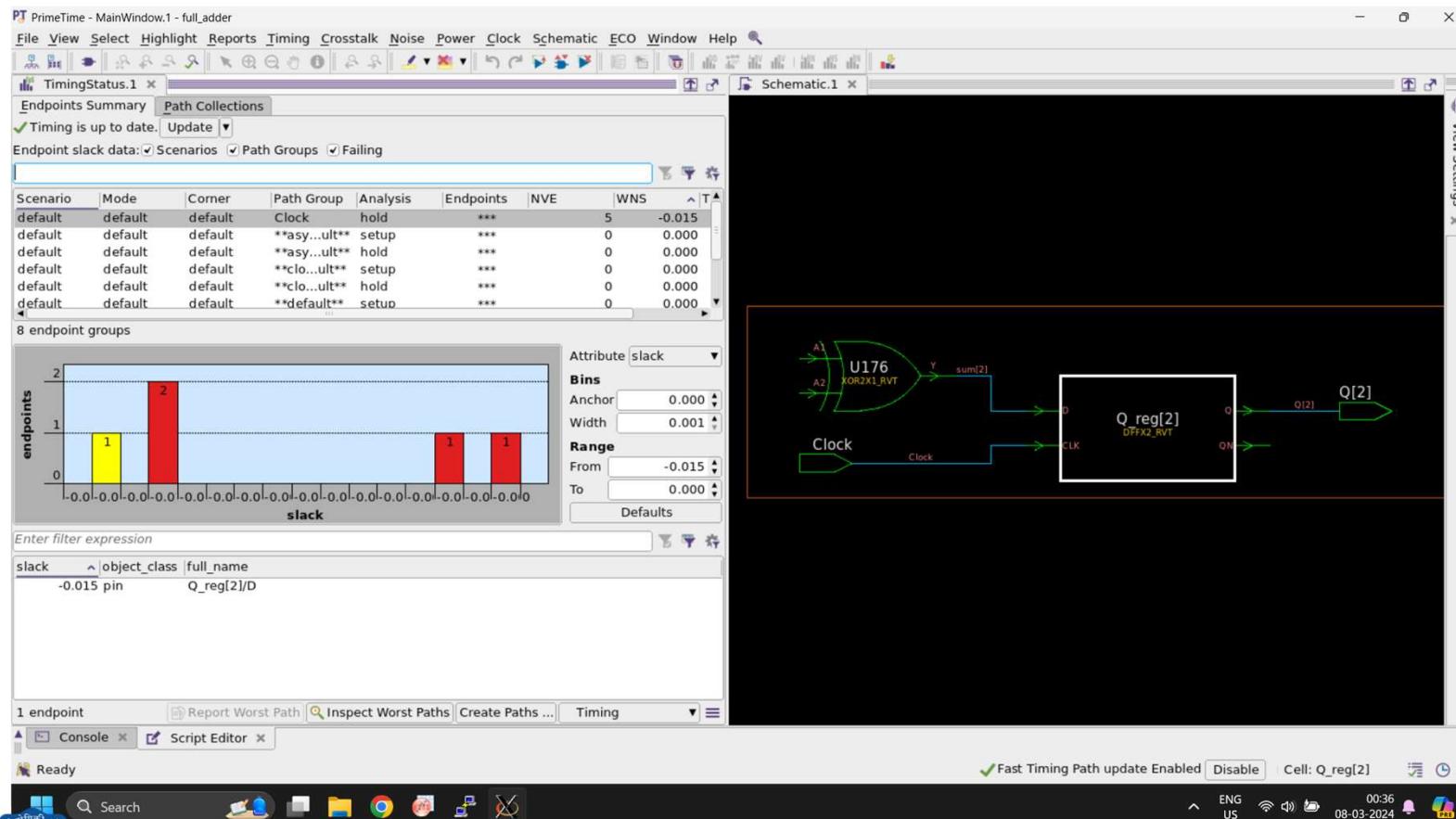
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PRIME TIME



TIMING (worst)
PATH considering
PARASITIC P2

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SPECIAL THANKS TO

- Mr. Puneet Mittal for interactive and informative guidance
- Will be helpful in studying each of the mentioned topics in depth because "***we haven't even learned 5% of PD***"
- I look forward to more such projects and might take up some.
- Hands on tool access was phenomenal. It was very interesting to work with all the tools used in the industry.



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