Integration, the VLSI Journal 65 (2019) 282–292

Contents lists available at ScienceDirect

Integration, the VLSI Journal

journal homepage: www.elsevier.com/locate/vlsi

Analyzing power-thermal-performance trade-offs in a high-performance 3D NoC architecture

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ARTICLE INFO

Keywords:
3D NoC
Small-world
Low power
Performance
VFI
Thermal hotspots

ABSTRACT

The emergence of three-dimensional (3D) network-on-chip (NoC) has revolutionized the design of high-performance and energy efficient manycore chips. However, in general, 3D NoC architectures still suffer from high power density and the resultant thermal hotspots leading to functionality and reliability concerns over time. The power consumption and thermal profiles of 3D NoCs can be improved by incorporating a Voltage Frequency Island (VFI)-based power management strategy and Reciprocal Design Symmetry (RDS)-based floor planning. In this paper, we undertake a detailed design space exploration for 3D NoC by considering power-thermal-performance (PTP) trade-offs. We specifically consider a small-world network-enabled 3D NoC (3D SWNoC) in this performance evaluation due to its superior performance and energy-efficiency compared to any other existing 3D NoC architectures. We demonstrate that the VFI-enabled 3D SWNoC lowers the energy-delay-product (EDP) by 57.3% on an average compared to a 2D MESH without VFI. Moreover, by incorporating VFI, we reduce the maximum temperature of 3D SWNoC by 15.2% on an average compared to the non-VFI counterpart. By complementing the VFI-based power management with RDS-based floor planning, the 3D SWNoC reduces the maximum temperature by 25.1% on an average compared to the non-VFI counterpart.

1. Introduction

Three-dimensional Network-on-Chip (3D NoC) achieves better performance and lower energy consumption than its two-dimensional (2D) counterparts [1–3]. Through the use of multiple planar layers and vertical communication capabilities, the 3D NoC enables smaller overall footprints with significant performance improvement over conventional 2D NoCs. In spite of this inherent performance benefits, 3D NoCs still suffer from thermal issues inherent in 3D ICs [1,2,4]. However, most of the existing works on 3D NoC focus only on the performance improvement without considering the effects of thermal hotspots. Creation of thermal hotspots adversely affects the performance of the manycore chip, compromising reliability and signal integrity, and eventually gives rise to possible higher cooling cost. High power density often leads to IR-drop issues, bias voltage instability and thereby imposes significant challenges for overall 3D system design. [5,6]

Voltage-Frequency Island (VFI)-based power management is a well-known methodology to lower the overall energy consumption within a given performance constraint [7,8]. Hence, it has been considered as an effective solution and employed to handle the thermal hotspots of conventional 2D as well as 3D manycore chips [9]. However, most of the existing VFI methodologies in 3D manycore chip use the conventional MESH-based NoC architectures [7,8]. As shown later in this work, incorporation of VFI-based power management for the MESH NoCs can introduce significant performance penalty and energy overheads for inter-VFI communications and thereby, fails to exploit the full benefits offered by VFIs under a given performance constraint. Hence, VFI-enabled 3D NoCs should incorporate a more efficient network topology to minimize the performance penalty and maximize the potential advantages of voltage-frequency (V/F) scaling.

A small-world network-enabled 3D NoC (3D SWNoC) is capable of outperforming traditional MESH-based and other irregular counterparts [10]. By adopting the power-law-based [11] small-world connectivity, the SWNoC reduces the average hop count and communication path length, and consequently, achieves significant performance gain and lower energy consumption compared to traditional multi-hop MESH NoCs. In a 3D SWNoC architecture with VFI-based power management, the vertical links can act as the long-range shortcuts for inter-VFI data exchange. This will ultimately mitigate the performance penalty inherent in any VFI-based design. Moreover, by adopting the Reciprocal Design Symmetry (RDS)-based floor planning [12] on top of VFI-based power management, we improve the thermal profile even further. In RDS, we

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https://doi.org/10.1016/j.vlsi.2017.12.002
Received 10 July 2017; Received in revised form 23 October 2017; Accepted 3 December 2017
Available online 15 March 2018

reduce the direct overlap of high power consuming core area to alleviate creation of thermal hotspots.

In this paper, we present a holistic design flow to address power, thermal, and performance (PTP) trade-offs of 3D SWNoC-based many-core chips. The salient contributions of this paper are as follows-

- We propose a joint optimization methodology by considering both performance and thermal profiles of the 3D SWNoC simultaneously. The optimization methodology is generic for any NoC architecture and results in significant thermal profile improvement while giving rise to insignificant performance penalty.
- We focus on the power, thermal, and performance trade-offs of 3D SWNoC-based manycore chips. In this work, we analyze and quantify the impact of topology, power management and RDS techniques with varying number of planar layers.
- We propose VFI- and RDS-enabled 3D SWNoC architecture to minimize the performance penalty and alleviate any possible thermal hotspots. We have also presented the comparative analysis of Non-VFI and VFI-based NoC with the different layer structures (2D and 3D), topologies (MESH and SW) and placement mechanisms (STACK and RDS).

The rest of the paper is organized as follows. Section 2 discusses previous research and developments pertinent to this study. Section 3 presents the design of 3D SWNoC architecture with VFI-based power management and RDS placement. Section 4 describes the thermal optimization incorporating the VFI clusters. Section 5 details the experimental analysis, and finally, Section 6 concludes this paper.

2. Related work

Most of the existing 3D NoCs predominantly utilize conventional MESH-based architectures [13,14]. However, it is well known that the MESH-based architecture suffers from high network latency and energy consumption due to its multi-hop communication. One of the major benefits of 3D-integration is the reduction of overall interconnect length by using the shorter vertical links. Consequently, by exploiting the shorter vertical links to reduce the network latency, NoC-bus hybrid architecture was proposed in [15]. This NoC architecture used a central bus arbiter and dynamic Time Division Multiple Access (dTDMA) technique for bus access in the vertical dimension. To improve the overall energy efficiency of the system, a 3D Dimensionally Decomposed (DimDe) NoC router architecture was developed [14]. Reducing the number of input ports, an improved version of 3D NoC router architecture was developed in [16]. All of these architectures have buses in the vertical-dimension, so they are subject to traffic congestion and high latency under high traffic injection loads when the network size increases.

To exploit the advantages of 3D integration, several works have addressed the synthesis of application-specific NoC architectures. The Sunfloor 3D was proposed for developing application-specific 3D NoCs [17]. The design and synthesis of application-specific 3D NoC architectures were also investigated in [18,19]. Later, a more general-purpose 3D NoC was proposed in [20] using an Integer Linear Programming (ILP)--based algorithm to insert long-range links to develop low diameter and low-radix architecture. The main focus of all the above-mentioned 3D NoC architectures is the performance improvement without considering the thermal concerns. Hence, in most of the cases, these architectures are subject to thermal hotspots.

Increasing power density and the resultant thermal hotspot are well-known limitations of 3D integration. There is a significant body of existing work that has dealt with various thermal issues in 3D ICs. The microfluidic channel (MFC)-based design is one of the most popular approaches to mitigate the thermal hotspot problem [4,21,22]. In addition, redundant TSV has also been utilized as the conducting channel between the dies of 3D ICs for dissipating the heat. In this context, a clustering-based redundant TSV insertion technique was proposed to remove heat in 3D ICs [23]. However, insertion of extra TSV is costly and affects the performance of neighboring TSVs. To spread the heat widely and effectively for overall 3D ICs, cooling architecture using thermal sidewalls, inter-chip plates, and a bottom plate (thermal-SIB architecture) is proposed in [24].

Thermal-aware task mapping is another popular design methodology to mitigate temperature hotspots in 3D IC. In [25], a genetic algorithm is used for thermal and communication aware task mapping in 3D design space. To predict the peak temperature profile of 3D IC, an accurate learning-based model is proposed in [26]. Several floor planning and TSV-placement methodologies are proposed for thermal- and leakage-power-aware 3D IC design [27–29]. However, in a 3D NoC, addressing only the thermal issues without considering the performance always results in suboptimal solutions. In this context, we propose a holistic design methodology and advocate to consider the power, thermal, and performance (PTP) tradeoffs simultaneously for designing an efficient 3D NoC architecture.

3. Design of 3D NoC architecture with VFI and RDS

In this section, we discuss the design methodology of a high performance, energy and thermal efficient 3D NoC architecture. First, we describe the details of only performance oriented 3D NoC design. Subsequently, to improve the energy efficiency further, we present the design methodology to incorporate VFI-based power management in the adopted 3D NoC architecture. We consider the small-world network-enabled 3D NoC (3D SWNoC) as the testbed to incorporate VFI-enabled power management. The 3D SWNoC architecture outperforms other regular and irregular NoC architectures in terms of network latency and energy efficiency [11]. Hence, we principally focus on this architecture. In addition to the VFI-based power management, we also consider the Reciprocal Design Symmetry (RDS)-based vertical placement to further reduce the power density and alleviate thermal hotspots in 3D SWNoC.

3.1. High performance 3D small-world NoC (SWNoC)

A small-world (SW) network lies between a regular, locally interconnected mesh network and a completely random Erdös-Rényi topology. The average shortest path length of SW graphs is bounded by $\log(N)$, where N refers to the number of nodes [30]. Hence, the SWNoC overcomes the limitations of multi-hop communications inherent in conventional MESH NoCs [10]. We consider the small-world network enabled 3D NoC architecture due to its superior performance compared to other existing 3D NoC architectures [11]. In our adopted 3D SWNoC topology, each core is connected to a nearby router and the routers are interconnected using planar metal wires and vertical links. The vertical links are enabled by through-silicon-vias (TSVs). Fig. 1 shows illustration diagram of small-world enabled 3D NoC (3D SWNoC) with TSVs as vertical links.

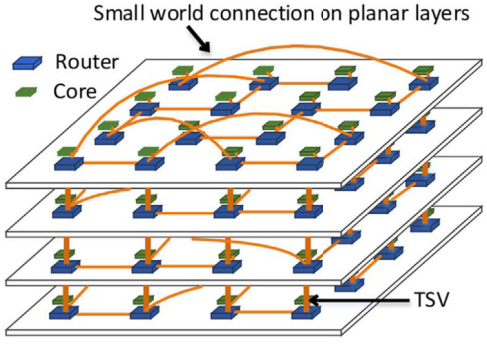

Fig. 1. Conceptual view of 3D SWNoC with TSV. For simplicity, only one logical XY-plane SW connection is shown here.

3.1.1. Designing power-law based 3D SWNoC

We construct 3D SW NoC architectures following a power-law based connectivity. The planar and vertical links follow the power law: $P_l = \gamma \cdot l^{-\alpha}$ where l is the length of the link, α is a parameter to determine the small-worldness, and γ is a normalization factor [31]. P_l is the number of the planar and vertical length-l links in network which follows the power law. Suppose a set of target link distributions $L = L_1, L_2, \ldots, L_T$ where T is the total number of layers and L_k is the link distribution in layer k. L_k is $r_{k,1}, r_{k,2}, \ldots$ where $r_{k,l}$ is the number of length-l links in layer k. We assume that a vertical link is much smaller than a planar link which count as length-1. r_v is the total number of vertical links. If P_1 is the number of length-1 links, $P_1 = \sum_k r_{k,1} + r_v$, and P_l is the number of length-l planar links, $P_l = \sum_k r_{k,l} (l > 1)$. The planar links follow this distribution of links: $\sum_k L_k = r_1, r_2, r_3 \ldots$ where $r_{(l=1)} = (\gamma \cdot l^{-\alpha} - r_v)$ and $r_{(l>1)} = \gamma \cdot l^{-\alpha}$. For example, if we consider a 64-core 3D MESH and SWNoC with 4 layers, it uses 48 vertical links and 96 planar links. The adopted 3D SWNoC architectures also use the same number of vertical and planar links. Hence, $L = 24, 24, 24, 24$ and $r_v = 48$. Also, if α is 2.4, L_k becomes $\{16, 5, 2, 1$ for each die. With this link distribution and design constraints, we randomly generate the initial solution which guarantees the connectivity (there exists at least one path between any pair of nodes). Depending on this power-law based link distribution, we can design 3D SWNoC architecture by following the physical NoC design constraints. For a fair comparison of the optimized SWNoC with MESH-based NoC, we constrain the SWNoC to have the same number of vertical and horizontal links as a 3D MESH. In addition, just like the MESH architecture, we evenly assign the same number of planar links to the four layers, so each layer has equal number of links for the same system sizes across different NoC configurations.

3.1.2. Optimization for high performance

Following the power-law-based connectivity and initialization of 3D SWNoC, we optimize the locations of the planar and vertical links to achieve better performance. We define C as the communication path length of a 3D NoC, which is a product of hop count, frequency of communications, and link length summed over every source and destination pair, i.e.,

$$C = \sum_{i=1}^{N} \sum_{j=1}^{N} \left(m \cdot h_{ij} + d_{ij}\right) \cdot f_{ij} \tag{1}$$

where h_{ij}, d_{ij}, and f_{ij} are defined as hop count, the Cartesian distance and the communication frequency between the i^{th} and j^{th} nodes respectively, and the parameter m is the number of NoC router stages.

For any two nodes, i and j, the parameter hop count, h_{ij}, indicates the number of intermediate nodes needs to be traveled to reach from one node to other. Alternatively, it refers to the number of intermediate routers for any message to travel from the source to the destination. Hence, h_{ij} is related to internode communication. The value of h_{ij} for any particular set of nodes (i, j) mainly depends on the network connectivity and ranges from 1 to N, where N is the total number of nodes. d_{ij} is physical distance corresponding to each hop calculated along the path. The parameter f_{ij} denotes the number of flits communicated between i^{th} and j^{th} nodes per cycle.

The routing stage parameter, m, is the number of intra-node stages that a message traverses from the input-port to output-port of a particular router. These stages include routing path computation, input arbitrations, input virtual channel allocation, switch allocation, switch traversal and similar steps on the output ports. In our adopted NoC routing scheme, we have employed three-stage routing mechanism including-route computation (RC) + virtual channel allocation, switch arbitration, switch traversal, and output arbitration. Hence, the numerical value of m in this work is 3. Optimizing the cost function, C, ensures lower average hop count and improves the overall NoC performance. It should be noted that the proposed design optimization methodology can be applied to NoC architectures with any number of intra-node stages.

3.1.3. Routing algorithm for 3D NoCs

The performance of a NoC largely depends on the routing algorithm. For the regular MESH architecture, XYZ is the preferred routing algorithms for their simplicity. In the case of irregular architectures such as the SWNoC considered here, the topology agnostic Adaptive Layered Shortest Path Routing (ALASH) algorithm is shown to be suitable [32]. ALASH is built upon the layered shortest path (LASH) algorithm, but has higher flexibility by allowing each message to adaptively switch paths, letting the message choose its own route at every intermediate router. The network is divided into a set of virtual layers and a message is not allowed to revisit a layer that it has already visited. This ensures that the layer's channel dependency graph remains free from cycles and deadlocks [32]. In this work, we incorporate the ALASH routing for SWNoC and XYZ dimension order routing for MESH NoC.

3.2. Voltage frequency island-enabled 3D NoC

Incorporating suitable power management strategy improves the power and thermal profiles of the 3D NoC-based manycore chips further. This can be implemented in two possible ways, viz., Dynamic Voltage and Frequency Scaling (DVFS) [9] and Voltage Frequency Islanding (VFI) [7]. In DVFS, the voltage and frequency (V/F) of each core and network element are fine-tuned individually depending on workload and traffic patterns. However, in VFI-based designs, a group of cores and their associated network elements are clustered together based on their computation and communications patterns. Then each cluster is assigned a single V/F level. Between these two power management techniques, DVFS is a more fine-grained methodology compared to VFI, and hence, can save more power. However, the implementation and hardware overhead in terms of on-chip voltage regulators and synchronizers is much more in DVFS than in VFI.

The VFI-based power management can be applied in two ways, viz., Static Voltage Frequency Islanding (SVFI) and Dynamic Voltage Frequency Islanding (DVFI). In this work, our main target is to analyze and quantify how incorporation of VFI-based power management can improve the thermal profiles of the 3D manycore system. Hence, as a case study, we have considered SVFI for the PTP trade-off analysis undertaken in this work.

To find the optimal clustering, we group the cores that have similar utilization i.e. instructions per cycle (IPC) and hence can benefit from the same V/F level tuning. For example, cores with low utilization are grouped together and assigned low V/F level, while cores with high utilization are clustered together to allocate high V/F levels. To determine the best static V/F levels for any cluster, we employ the power and performance models proposed in [33]. The model uses a constrained-posynomial-based formulation for determining the workload-dependent power-frequency relationship over an extended range. Also, the performance and power models are trained and cross-validated for various benchmarks with root-mean-squared-percentage-error (RMSPE) of 4.37% [33].

To illustrate the heterogeneous-clustering-based VFI-enabled 3D NoC architecture, Fig. 2 shows an example of a 64-core system with four VFIs. As seen from the figure, the number of cores in each individual cluster vary among them. In addition, the cores of the highest power consuming cluster are, in general, placed closer to the heat sink for removing maximum possible heat from the system. However, this does not essentially remove all the thermal hotspots from the manycore chip, which motivates us to investigate the role of efficient floor planning in 3D NoC architecture.

3.3. Reciprocal Design Symmetry (RDS) placement

In a 3D manycore chip, the placement of cores, routers, and associated network elements significantly affect the thermal profile of the

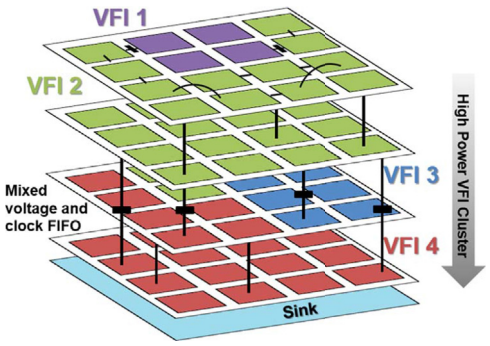

Fig. 2. Illustration of VFI-Enabled 3D SWNoC architecture. Each VFI has different number of tiles.

overall architecture. Stacking high power consuming cores directly on top of each other increases the power density and consequently, creates thermal hotspots. To solve this thermal issue in the 3D NoC, we employ Reciprocal Design Symmetry (RDS)-based vertical placement. Fig. 3(a) shows the general vertical placement in a 3D architecture where cores in every die are stacked on top of each other (their individual sizes may vary depending on the design). Hence, we call this general vertical placement as the 'STACK' arrangement. In STACK placement, adjacent routers are perfectly aligned and TSVs maintain direct communications among them. Consequently, the routers from adjacent layers (dies) communicate in a single hop with STACK-based placement. This ensures maximum achievable performance from floor planning and router placement. However, it may introduce thermal hotspots in the system.

To alleviate the thermal hotspots due to stacking of high power consuming cores on top of each other, RDS-based floor planning has been advocated [12]. Fig. 3(b) shows the RDS-based placement in the 3D NoC architecture. For RDS-based floor planning, instead of stacking cores on top of each other (STACK), the cores are placed diagonally such that the amount of overlap area among the vertically adjacent cores is minimized. In general, cores dissipate the highest amount of power in a manycore chip. Consequently, the diagonal vertical placement of cores and associated routers alleviates creation of the thermal hotspots without any additional area overhead. However, it is necessary to add an extra planar link between two diagonally placed routers. As a result, the total interconnect length increases and the overall performance worsens compared to the STACK-based design. Hence, we achieve thermal efficiency in the RDS-based design at the cost of performance degradation. In this work, we employ RDS vertical placement in 3D NoC architectures on top of the VFI-based power management and evaluate the efficiency of the proposed design considering the performance-thermal trade-offs.

4. Optimization of thermal-aware 3D SWNoC

In this section, we present the optimization methodology of our proposed architecture including thermal modeling and the design of 3D SWNoC incorporating the VFI clusters.

4.1. Thermal modeling

Design of 3D SWNoC requires efficient placement of cores and links, so we optimize the locations of the cores and links at the same time. To unify the NoC performance with thermal-aware core and link placement, we define a single cost function that combines them as follows:

$$\text{cost} = \alpha \cdot C + \beta \cdot T \tag{2}$$

where C is the unified NoC performance from (1); T is the temperature of the system determined by following [34]; and α and β are weighting factors. Our goal is to minimize the cost function to achieve the optimum network latency, energy consumption, and the lowest temperature of the 3D SWNoC.

In order to estimate the temperature T, the 3D IC can be converted into a 3D resistive network. Then, we can solve the whole 3D resistive network by a matrix solver to obtain the temperature of each node. Additionally, the standard thermal profile characterization tool e.g. Hotspot simulator [35] can be employed to determine the temperature, T. However, solving the matrix equation (and/or standard thermal simulator call) for each solution during the optimization process is still costly in terms of resource and time consumption. Hence, we use the established model from [34], which is simple and relatively fast to make the optimization methodology faster. Using this model ensures placing the high power consuming cores close to the bottommost layer (near the heat sink) and low power consuming cores near the topmost layer. It is to be noted that we have used the fast-forward model during the optimization process only, however, for comparative thermal profile evaluation (Section 5), and to determine the final temperature we employ the Hotspot tool.

4.2. Thermal-aware network optimization

To optimize the overall cost function, we use simulated annealing (SA) algorithm. As we focus on both core and link perturbation in the 3D SWNoC architectural space, we utilize two moves for solution perturbation namely the *swapping* ($S(i,j)$) and the *new link placement* ($L(l)$) as discussed below:

- *Swapping - S(i,j)*: selects two cores i and j randomly and swaps their locations.
- *New link placement - L(l)*: selects and removes a link of length-l between two randomly selected routers. If a link is a planar link, create a new link of the same length between two other routers in the same layer. If a link is a TSV along the vertical direction, create a new TSV.

The $L(l)$ move preserves the number of length-l links, which is required to maintain the power-law and the small-worldness of the 3D SWNoC architecture during and after optimization. On each iteration, the probability of selecting the $S(i, j)$ or the $L(l)$ perturbation is set to 0.5. Alternating in between these two perturbations, we avoid the possibility to get stuck to a local minimum in the solution space and thereby reach a global optimum.

To incorporate the VFI-based power management, we modify the

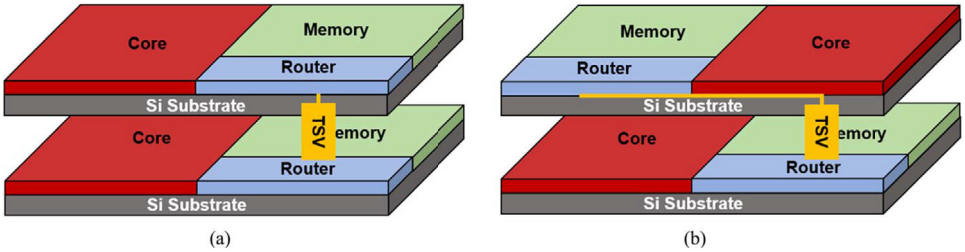

Fig. 3. Illustration of different floor planning methodologies to enable multi-layer (die) 3D manycore chip design. Two kinds of floor planning (a) STACK and (b) RDS vertical placement have been shown. In the figure, the different elements are marked with different colors to emphasize the relative power consumption profiles (red being the highest power consuming element while blue is the least one). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article)

simulated annealing algorithm used for NoC architecture optimization. First, we modify the swapping perturbation function, *S(i,j)* to *S′(i,j)* as follows:

- *VFI Swapping – S′(i,j)*: selects two cores *i* and *j* randomly and swaps their locations if the locations do not violate the constraint of VFI clusters after swapping.

By redefining the *swapping* move (*S′(i,j)*), we can optimize the location of cores and VFI clusters with the simulated annealing-based algorithm. In the following example, we show how the VFI swapping function works. To incorporate the VFI power management, we change the core swapping perturbation function. In VFI swapping, we select two cores *i* and *j* randomly and swap their location if the locations do not violate the constraint of VFI clusters after swapping (no isolated cores from their V/F clusters). For example, Fig. 4 shows examples of VFI-enabled 3D NoC, which has been marked with the distinct colors to highlight the different VFI clusters. From Fig. 4(a), if we swap core A and B, there is no isolated cores from their respective V/F clusters after swapping A and B in Fig. 4(b) (no violation of the VFI constraint and corresponding swapping is allowed). However, if we swap core A and C in Fig. 4(a), the core A is isolated from blue clusters (violation of VFI constraint and hence, this swapping is not allowed) in Fig. 4(c).

During the optimization process, optimizing the cost function (as defined in (2)) places the high power consuming cores close to the bottommost layer (near heat sink) while low power consuming cores move to the topmost layer. Therefore, the high power VFI cluster is placed closer to the heat sink to improve the thermal profiles. Hence, even if we put the high power VFI cluster away from the heat sink, for the optimized configuration, the cluster will move near the heat sink regardless of initial VFI-cluster placement. However, choosing a random VFI-cluster placement takes longer time to reach the optimized configuration. In this work, during the initialization step, we adopted a greedy algorithm for VFI-cluster placement to achieve the optimized solution faster. In other words, we placed the high power VFI cluster near the sink while the least power consuming cluster is placed furthest away from the sink to achieve the optimized solution faster.

5. Experimental results and analysis

In this section, we evaluate the performance and estimate the temperature profiles of the NoC architectures with different number of planar layers by considering various benchmarks. For this performance evaluation, we consider two relevant performance metrics: latency, and energy-delay-product (EDP). We define the EDP as the product of network latency and energy dissipation to unify the effects of both these two metrics into a single parameter. To evaluate the thermal profiles of the architecture, we consider the maximum, average, and minimum temperature of the manycore chip.

5.1. Experimental setup

To obtain the detailed processor and network level information, we use GEM5 [36], the full system simulator, for a system consisting of 64 alpha cores. The memory system is MOESI_CMP_directory and it consists of 64KB L1 (data + instruction) and a shared 8MB L2 cache. In this performance evaluation, we consider a set of eight applications with widely varying communication and computation intensities. We use four SPLASH-2 benchmarks (FFT, RADIX, LU, and WATER) [37] and four PARSEC benchmarks (DEDUP, VIPS, FLUIDANIMATE (FLUID), and CANNEAL (CAN)) [38]. We incorporate the processor level statistics generated from GEM5 in McPAT (Multicore Power, Area, and Timing) [39] to determine the processor level power values.

We follow the hybrid clustering methodology presented in [40]. Table 1 shows the V/F values of all four VFI clusters and their respective sizes for the eight benchmarks. These VFI clusters are created to achieve at least 95% of performance of the system with all clusters running at the nominal V/F. In this work, the adopted VFI-controller consumes 39.1 *nJ* energy for each V/F transition [40]. In addition, the VFI controller incurs area overhead. However, the controller area overhead is also related to the size of the individual cluster. In our work, the largest VFI controller has an area of 0.06 mm^2, which is less than 0.1% of the overall chip area ($10 \times 10 \times 4$ mm^2 total area) and can be considered negligible for the overall chip footprint. Consequently, in this work, we use VFI as the suitable power management mechanism for 3D SWNoC and apply heterogeneous clustering (having different number of tiles for each cluster) for exploiting maximum benefits of VFI-based methodology [40].

After obtaining all the core and network powers, we use the HotSpot [35] to obtain the thermal profile of the overall system. We arrange the 64 cores in 1-layer, 2-layer, 3-layer, and 4-layer 3D systems. Table 2 shows the die size of each different layer structures. All the SWNoC configurations use the same number of vertical and planar links as a MESH NoC for fair comparison and analysis. Fig. 5 shows our overall experimental setup considered in this work.

5.2. Effects of performance and thermal joint-optimization

In this section, we evaluate the effectiveness of the proposed joint-optimization framework (performance and thermal) for 3D SWNoC. To characterize both the system performance and the overall thermal profile, we consider two parameters, viz. the energy-delay-product (EDP) per message and the temperature of the system. We consider the maximum, average and minimum temperatures in order to determine any possible creation of thermal hotspots. For ease of referencing, the joint optimized (performance and thermal) SWNoC and the baseline SWNoC (optimized only for performance) are marked as PTO and PO respectively. It is to be noted that for PO-based NoC architecture, we optimize the performance oriented unified cost function termed as the communication path length, *C*, as defined in (1). On contrary, for PTO-based architectures, we target to optimize the joint cost function that unifies both the performance (*C*)

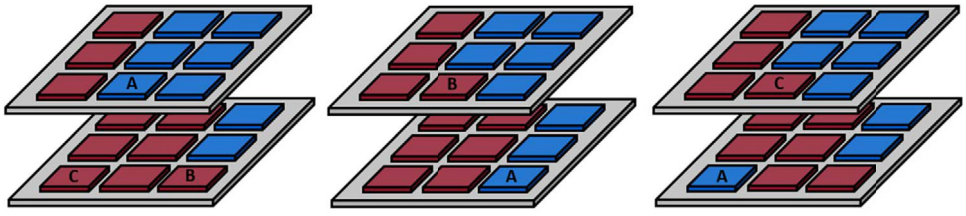

Fig. 4. Illustration of VFI core swapping cases. (a) is the initial design before swapping. (b) has no VFI cluster violation after swapping cores A and B (swapping is allowed). (c) has VFI cluster violation after swapping cores A and C (swapping is not allowed). (For interpretation of the references to color in this figure, the reader is referred to the web version of this article)

Table 1
VFI clusters size and their respective V/F levels [40].

	CANNEAL	DEDUP	FFT	FLUID	LU	RADIX	VIPS	WATER
Cluster 1	22–0.6	40–0.9	29–0.9	40–0.9	32–0.8	37–1.0	30–0.7	33–0.8
Cluster 2	22–1.0	16–1.0	23–1.0	16–1.0	24–1.0	19–0.9	26–0.9	23–1.0
Cluster 3	16–0.6	4–1.0	7–0.9	4–0.7	4–0.6	4–0.9	4–0.7	4–0.9
Cluster 4	4–0.9	4–1.0	5–0.9	4–0.8	4–0.9	4–0.8	4–0.9	4–0.7

Table 2
Chip size for the different number of layers.

Number of layers	1	2	3	4
Layer size (mm^2)	20×20	20×10	15×10	10×10

and temperature profile (T) of the NoC as defined in (2).

Fig. 6 shows the maximum, average and minimum temperature values of the 4-layer PO- and PTO-SWNoC of non-VFI system for eight SPLASH-2 and PARSEC benchmarks mentioned earlier in Section 5.1. From the figure, we can see that the PTO-based design improves the temperature profile compared to PO across all the benchmarks. The peak temperature of PTO is lower than PO by 1.9–18.9% (2.3 °C to 19.8 °C) depending on the specific benchmark. In addition, the difference between the maximum and minimum temperatures of PTO is lower than that of PO. The PTO-based NoC more efficiently distributes the total power over the whole 3D chip when compared to the NoC optimized for performance (PO) only, and hence, PTO alleviates creation of thermal hotspots. The variation in peak temperature reductions shown in Fig. 6 is related to the standard deviation among the core power values for a particular application.

To explain this, we show the average and the standard deviation of core powers for the same four-layer 3D manycore chip in Table 3. In this table, the WATER benchmark has the highest average and the second highest standard deviation among the core powers. This happens due to the presence of a few highly active and frequently communicating cores for this specific benchmark. In PO, to optimize performance, high power consuming cores are placed closer to each other leading to thermal hotspots and a poor temperature profile (more than 130^0C). In contrast, PTO distributes these highly active cores over the whole chip area by considering their temperature profiles during the optimization process, and thereby lowers the peak temperature to 114^0C. In addition, among all the applications considered, the RADIX benchmark achieves the least reduction in the maximum chip temperature. This happens due to the fact that for the RADIX benchmark, the core power consumptions are nearly uniform (as shown with a low standard deviation value in Table 3) and thus the temperature profile of RADIX cannot be improved significantly by varying the placement of the processing cores.

In addition, to compare the performance of PO and PTO, Fig. 7 shows their respective EDP values. For comparison purpose, the EDPs are normalized with respect to the EDP value of PO. Here, to compute the EDP value, we consider the average message latency and the average message energy. As shown in the figure, the PTO shows on an average 2.2% higher EDP values than that of the PO, while the maximum increase of 4.4% is observed for the CANNEAL benchmark.

By comparing both Figs. 6 and 7, one can observe that the PTO technique significantly improves the thermal efficiency (maximum reduction of peak temperature by 18.9%) of the 3D SWNoC while only incurring a maximum 4.4% EDP penalty when compared to the baseline PO. In addition, if we compare the average of the peak temperature and EDP values, then PTO shows 9.9% thermal improvement while incurring 2.2% higher EDP compared to PO. Hence, we can conclude that PTO-based design methodology is more efficient considering the performance-thermal trade-offs compared to the PO-based approach.

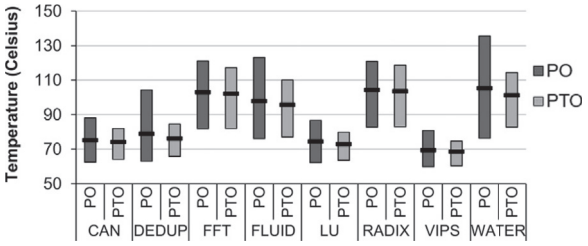

Fig. 6. Maximum, average and minimum temperatures of 4-layer PO- and PTO-SWNoC of non-VFI system for all the benchmarks.

Table 3
Average and standard deviation of core-power of a 64-core non-VFI system.

Benchmark	Average (W)	Standard deviation (W)
CANNEAL	0.71	0.12
DEDUP	0.82	0.43
FFT	1.36	0.11
FLUID	1.25	0.33
LU	0.68	0.14
RADIX	1.38	0.07
VIPS	0.57	0.10
WATER	1.40	0.41

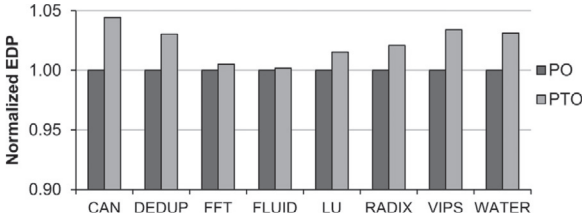

Fig. 7. Normalized EDP profiles of 4-layer PO- and PTO-SWNoC of non-VFI system for all the benchmarks.

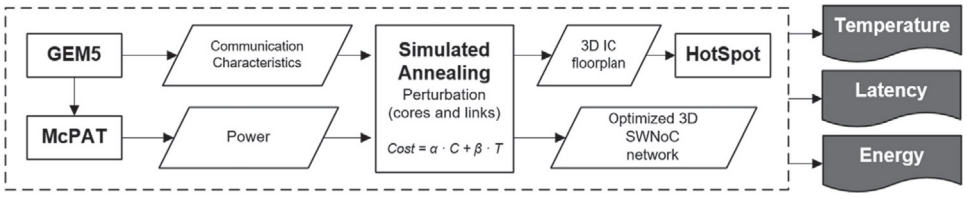

Fig. 5. Experimental set up for establishing the performance and thermal trade-off for VFI-enabled 3D SWNoC.

5.3. Performance and temperature trade-off

In this section, we explore the impact of the system design parameters on the performance of the 3D SWNoC. In particular, we evaluate the impact of the number of planar layers, network configuration, V/F scaling and different vertical placements. We consider four different configurations, viz. 1-layer (2D SWNoC), 2-layer, 3-layer and 4-layer 3D SWNoC architectures. To evaluate the impact of VFI-based power management, we use NVFI (non-VFI, employs no V/F tuning) and heterogeneous clustering-enabled VFI (explained earlier in Section 3.2.) strategies. In addition, to evaluate the effects of vertical placement on the performance and thermal profiles of 3D NoC, we consider STACK- and RDS-based floor planning (explained in Section 3.3). Just like the previous sections, we choose the normalized network latency, EDP value and the temperature profile as the relevant performance metrics.

5.3.1. NoC performance evaluation

In this section, we compare the performance of the MESH and SWNoC architectures by incorporating VFI-based power management. By default, the initial VFI configuration follows the STACK-based floor planning. Next, we evaluate the role of the RDS-based floor planning in the VFI-based design. As mentioned earlier in Section 5, we consider the average network latency and EDP per message as the relevant metrics. All the network latency and EDP values are normalized with respect to the latency and EDP of a baseline 2D non-VFI system with standard MESH NoC architecture.

Fig. 8 demonstrates the normalized network latency of the 3D MESH and SWNoC with NVFI and VFI configurations for different number of layers. All the network latencies are normalized with respect to that of 3D MESH with NVFI and 1-layer configuration.

From Fig. 8, it is seen that as the number of layers increases, the network latencies of MESH and SWNoC decrease. The best network latency value is achieved for the 4-layer 3D SWNoC architecture with NVFI configuration. To explain this, we show the normalized average path lengths (as defined in (1)) for each 3D configurations in Fig. 9. As seen from this figure, the SWNoC has lower communication path length compared to the MESH-based counterparts for the same number of layer. Consequently, SWNoC achieves lower latency than the MESH-based NoC. In addition, increasing the number of planar layers lowers the average path length significantly. For example, a four-layer 3D architecture can reduce as much as 24.0% and 36.9% average path length for MESH and SWNoC architectures respectively compared to their 1-layer counterparts. As a result, the four-layer SWNoC architecture shows 15.8% lower network latency value compared to its 1-layer counterpart.

From Fig. 8, we can also see that the VFI-enabled NoC incurs different amount of network latency penalty compared to its NVFI counterpart depending on the number of layers and network configurations. VFI-enabled SWNoC incurs maximum and average of 14.3% and 6.3% network latency penalty respectively compared to its NVFI counterpart. The VFI-enabled traditional MESH design incurs more latency penalty than the VFI-enabled SWNoC architecture. Interestingly, the VFI-based SWNoC, shows better network latency than NVFI MESH. In VFI-based NoC, the energy consumption of the overall system is reduced by incurring a certain amount the performance penalty. Due to the trade-off between the network latency and energy, the EDP is the unified and most relevant metric to analyze the efficiency of manycore systems with VFI-enabled power management.

Fig. 10 shows the EDP profiles of the 3D MESH and SWNoC, and their respective VFI-enabled configurations for different number of layers. For comparative performance evaluation among different configurations, EDP values are normalized with respect to the 3D NVFI MESH architecture. From Fig. 10, we can observe that the EDP value also decreases for both the MESH- and SW-based architectures as the number of layers increases. The EDP value of a network depends on the average hop count and communication path length. As seen from Fig. 9, as the number of layers increases, more number of vertical links can act as the long-range shortcuts between layers and the path length reduces. Consequently, following the network latency trend in Fig. 8, the EDP also decreases progressively as the number of the layer increases. The NoC with more layers offers more connectivity and opportunities for exploring the optimized NoC architecture. Hence, 3D NoCs with higher number of layers perform better than 2D NoCs (number of layer equals to 1 for 2D NoC). On an average, 3D SWNoC with 4-layer shows 20.8% reduction in EDP value compared to 2D NoC.

In addition, from Fig. 10, by comparing the EDP of NVFI and VFI-enabled architectures for all possible configurations, we can see that the VFI outperforms NVFI counterparts while using the same topologies and layer configurations. The EDP of the VFI-enabled SWNoC is lower than that of the NVFI NoC by up to 15.1% (average 8.3%) depending on the specific benchmark. This happens because the VFI-enabled SWNoC incurs only 2.6–14.3% penalty in network latency while reduces energy consumption by 8.5–34.9% compared to the NVFI counterpart.

Moreover, as shown in Fig. 10, the EDP of the VFI-enabled SWNoC is lower than that of the VFI-enabled MESH by up to 30.8% (average 16.9%) depending on the specific benchmark for the same number of layers. The lower EDP of SWNoC is primarily due to its lower path length compared to the MESH (can be observed in Fig. 9). Lower path lengths lead to lower inter-router hop counts resulting in the reduction of energy consumption in the routers and links. Thus, the SWNoC always shows lower EDP than the MESH. Also, the latency penalty incurred by the VFI technique is minimized by adopting the SW-network topology.

To summarize the performance of different NoC configurations, Fig. 11 demonstrates the normalized average EDP value of all benchmarks for the NVFI and VFI configurations for both the MESH and SWNoC architectures. On an average, the EDP difference between NVFI MESH and SW topologies varies from 13.6% to 28.1% depending on the number of layers. Similarly, the EDP difference between VFI MESH and SW topologies ranges from 8.8% to 22.5%. In addition, VFI MESH topologies show 11.7–15.8% lower EDP values compared to their NVFI counterparts. Finally, the EDP difference between NVFI and VFI SW topologies varies from 6.9% to 9.7%. From the figure, it is evident that among all these configurations, VFI SWNoC with 4-layer achieves the lowest EDP. On an average, VFI SWNoC achieves 57.3% lower EDP compared to NVFI 2D MESH (with 1-layer).

Fig. 12 shows the normalized network latency of VFI configuration for MESH and SWNoC using STACK and RDS vertical placement for the

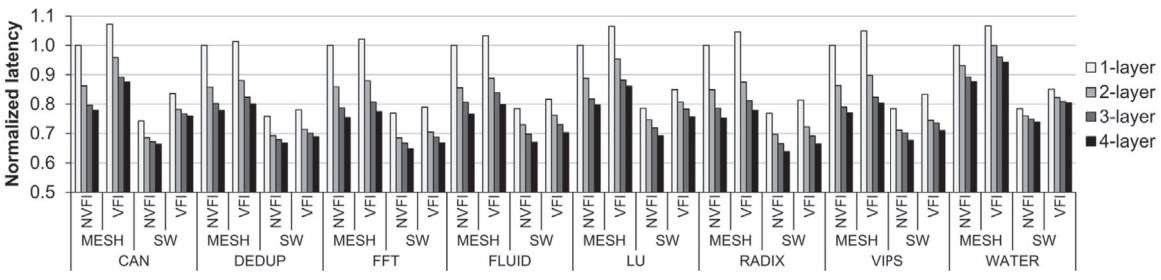

Fig. 8. Normalized network latency of NVFI and VFI configurations for 3D MESH and SWNoC architectures for different number of layers.

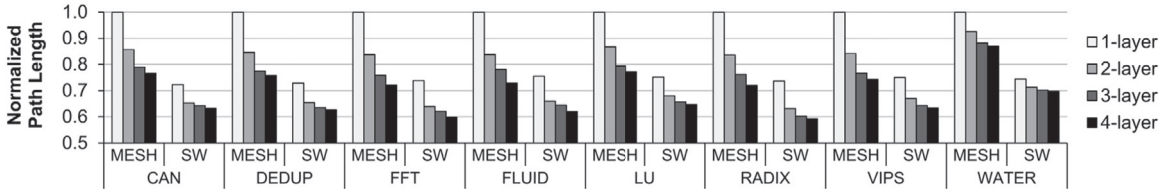

Fig. 9. Normalized path length of 3D MESH and SWNoC for different number of layers.

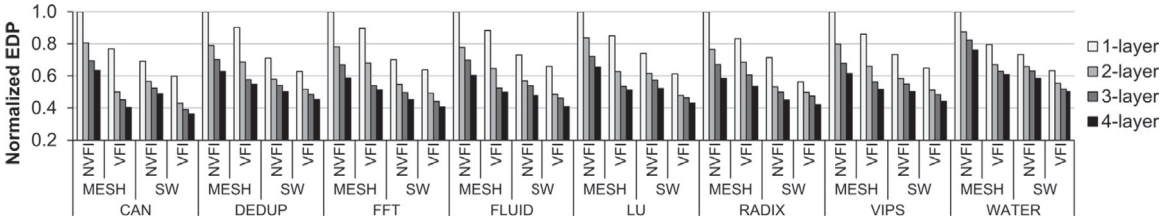

Fig. 10. Normalized EDP of NVFI and VFI configurations for 3D MESH and SWNoC architectures for different number of layers.

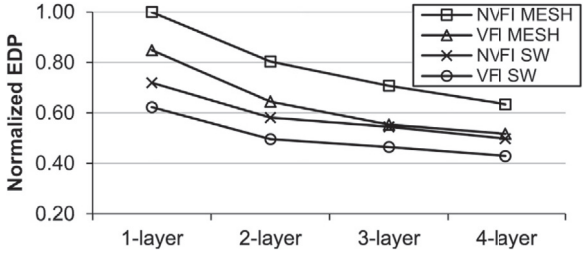

Fig. 11. Normalized average EDP profiles for NVFI and VFI configurations for 3D MESH and SWNoC architectures.

different number of layers. From Fig. 12, we can see that the network latency increases for both the MESH and SWNoC architectures with the RDS-based placement (except for 1-layer configuration). NoC architectures with 1 layer are essentially planar configurations and hence, for this case, there is no difference between the RDS- and STACK-based floor planning. However, for architectures with more than one layer, the RDS-configurations show higher network latency values compared the STACK-based counterparts. From Fig. 12, we can see that for all the benchmarks considered, the MESH with RDS-based floor planning shows up to 5.8% (average 3.9%) higher network latency than the STACK-based configurations while SWNoC with RDS shows up to 4.8% (average 3.7%) higher network latency than STACK. This happens because of the fact that for the RDS-based floor planning, the average interconnect length and communication path-length are more than that of the STACK configurations. To illustrate this, Fig. 13 shows the normalized average path lengths for each 3D configuration. On an average, MESH and SWNoC using RDS vertical placement have 4.3% and 3.5% higher path length compared to 3D NoC using STACK placement. Consequently, the increased communication path length between layers leads to higher network latency values for the RDS compared to the STACK placement.

In addition to the network latency analysis, we also evaluate the RDS and STACK NoCs from the EDP perspective. Fig. 14. shows the normalized EDP of VFI-enabled MESH and SWNoC configurations using STACK and RDS placements with different numbers of layers. The MESH topology using RDS vertical placement shows up to 10.4% (average 5.1%) higher EDP than STACK. Similarly, the RDS-enabled SWNoC topology shows up to 6.4% (average 4.5%) higher EDP than STACK placement.

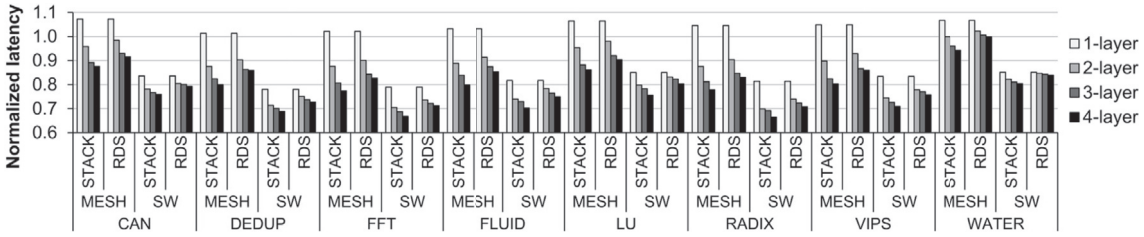

Fig. 12. Normalized network latency of VFI configuration for 3D MESH and SWNoC architectures using STACK and RDS vertical placement for different number of layers.

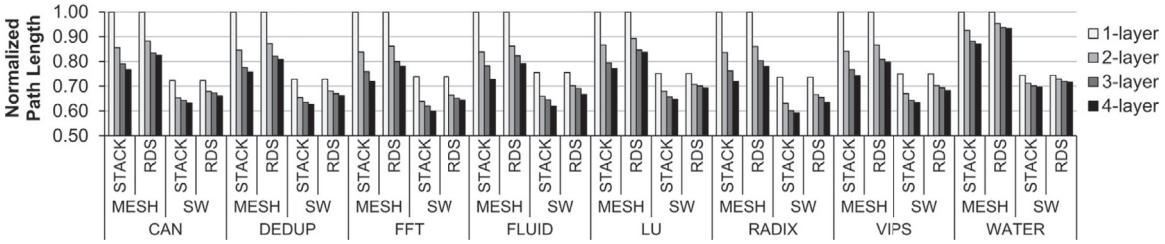

Fig. 13. Normalized path length of 3D MESH and SWNoC architectures using STACK and RDS vertical placement for different number of layers.

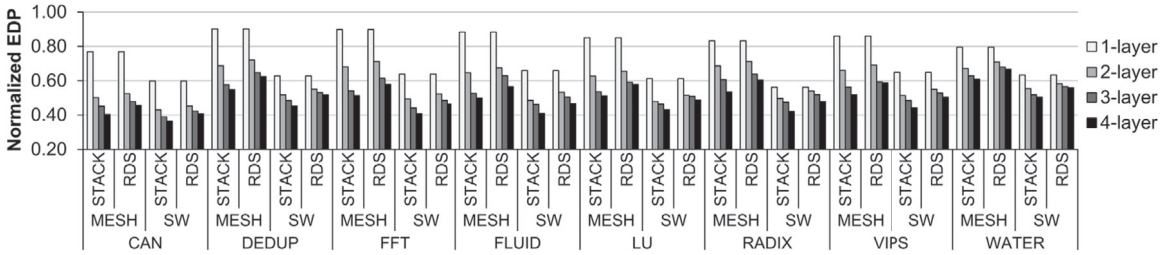

Fig. 14. Normalized EDP of VFI configuration for 3D MESH and SWNoC architectures using STACK and RDS vertical placement for different number of layers.

The reason behind the increase in EDP profile of RDS-based floor planning is that each message travels longer planar link lengths in the NoC using RDS placement than in STACK. Since longer path lengths lead to higher router, link and overall energy consumption per message, the 3D NoC using RDS vertical placement has higher EDP than STACK.

Finally to summarize the effects of RDS and STACK based floor planning on the 3D NoC configurations, Fig. 15 shows the average EDP profiles (averaged over all the benchmarks considered in Fig. 14) of VFI-enabled 3D MESH and SWNoC with different number of layers. The EDP difference between STACK and RDS increases gradually from 1-layer to 4-layer. The average EDP difference of MESH topology between STACK and RDS is 0.0%, 3.0%, 5.6% and 6.6% for layer-1 to layer-4 respectively. Similarly, the average EDP difference of SWNoC between STACK and RDS are 0.0%, 3.4%, 4.3% and 5.6% respectively for layer-1 to layer-4.

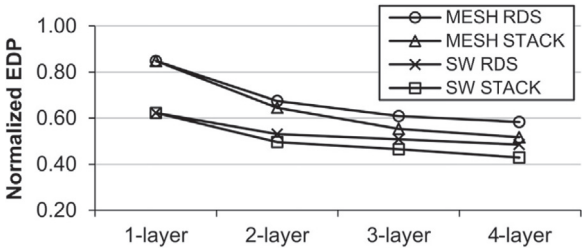

Fig. 15. Normalized average EDP profiles of VFI configuration for 3D MESH and SWNoC architecture using STACK and RDS vertical placement of all benchmarks.

5.3.2. Evaluation of thermal profiles

In this section, we evaluate the thermal profiles of different NoC configurations. For thermal profile evaluations, we consider the 3D SWNoC as the baseline architecture as it performs better than the MESH (as shown earlier in Section 5.3.1). To demonstrate the merits of VFI-based power management to improve the thermal profiles, we consider the 3D SWNoC architecture with NVFI and VFI configurations. In addition, to evaluate the joint effects of power management and vertical placement, we compare the thermal profiles of VFI configuration using STACK and RDS-based floor planning. To characterize the thermal effect, we consider the maximum, average and minimum temperatures of the system as the relevant metrics.

Fig. 16 shows the maximum, average and minimum temperature values of the 3D SWNoC with varying number of planar layers for both non-VFI and VFI-enabled configurations. By default, the temperature profile shown in Fig. 16 considers the STACK-based floor planning. From this figure, we observe that as the number of layer increases, the maximum, average and minimum temperatures are increased noticeably. Moreover, the difference between the maximum and minimum temperatures also increases progressively as we increase the number of layers. The planar die area of a chip is scaled down with the increase in the number of layers to keep the total area of the 3D chip fixed. Hence, this leads to higher power densities and temperatures (in Fig. 16). To evaluate the impact of VFI-based power management, we compare the temperatures between the SWNoC with NVFI and VFI. VFI-enabled 3D SWNoC architecture improves the temperature profiles compared to the NVFI counterpart. The maximum temperature of 4-layer 3D architecture is reduced by up to 24.4% (average 15.2%) by virtue of incorporating VFI techniques.

Compared to the NVFI-3D SWNoC configuration, the VFI-based 3D SWNoC achieves an average of 3.2 °C, 5.6 °C, 10.0 °C and 14.9 °C reduction in maximum temperature for 1-layer, 2-layer, 3-layer and 4-layer 3D STACK, respectively. The maximum temperature difference increases progressively from 1- to 4-layer. This occurs due to the fact that VFI-based power management reduces the V/F levels and hence, mitigates the power density problems associated with multiple stacked layers. Therefore, it helps to alleviate the thermal hotspots.

Now, we discuss the joint effects of VFI-enabled power management methodology with RDS-based floor planning. Fig. 17 shows the temperature profile of VFI-enabled 3D SWNoC architecture using STACK and RDS-based floor planning for different number of layers. From this figure, we can see that VFI-enabled SWNoC using RDS vertical placement has better temperature profile than STACK in all the cases except 1-layer configuration (both the RDS and STACK configurations are same for 1-layer architecture). The maximum temperature of 4-layer architecture using RDS vertical placement reduces up to 14.5% (average 10.9%) compared to the STACK-configuration. This happens due to the placement of high power consuming cores in non-overlapping configurations.

Compared to the STACK-configuration, the VFI-enabled SWNoC with RDS-based floor planning achieves on an average of 0.0%, 5.4%, 6.9% and 10.9% reduction in maximum temperature for 1-layer, 2-layer, 3-layer and 4-layer designs respectively. There is no temperature difference for 1-layer configuration. As the number of layers increases, the possibility of thermal hotspot creation increases for STACK configurations. However, for RDS-based floor planning, the creations of hotspots are avoided. Consequently, the average and maximum temperatures are reduced for the RDS-based configurations. The improvement in temperature difference for the RDS configuration increases as the number of layers increases from 1-layer to 4-layer. To verify the efficiency of RDS technique, we compare the performance and thermal trade-offs of 3D SWNoC. From Fig. 14, the EDP penalty of RDS-based SWNoC is 0.0%, 3.4%, 4.3% and 5.6% from 1-layer to 4-layer compared to STACK. Hence, as the number of layers increases in the system, the RDS floor planning becomes more efficient. For configurations with one or two layers, the efficiency of the RDS-based floor planning is modest.

As discussed in Section 5.3.1, VFI-based power management significantly reduces overall power consumption of the manycore chip and consequently, the temperature profile of the system improves. In addition to the VFI-based methodology, RDS-based vertical placement also helps to reduce the creation of thermal hotspots. Fig. 18 shows the thermal maps of 3D SWNoC for three different configurations viz. 3D SWNoC with STACK and without VFI (STACK NVFI), 3D SWNoC with STACK and VFI (STACK VFI), and 3D SWNoC with RDS and VFI (RDS VFI). From the figure, it is seen that STACK NVFI shows the highest temperature expectedly. Incorporating the VFI-enabled power management methodology with STACK-based 3D SWNoC (STACK VFI) lowers the maximum and average temperatures for all the nodes across the manycore chip. On the other hand, the 3D SWNoC with RDS and VFI-enabled methodology

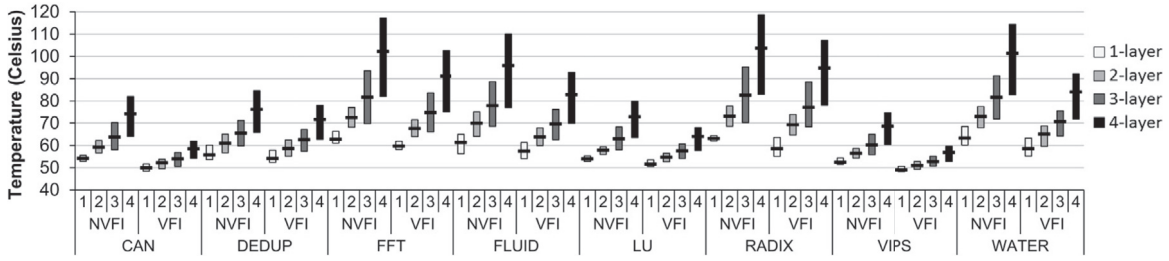

Fig. 16. Temperature profile of 3D SWNoC architecture with NVFI and VFI configurations for different number of layers.

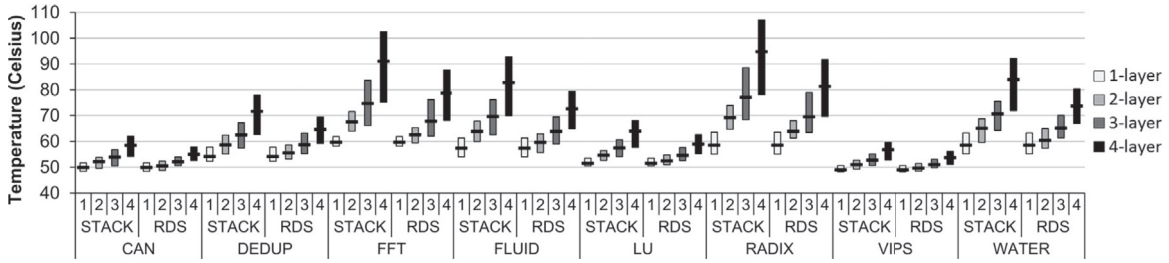

Fig. 17. Temperature profile of 3D SWNoC with VFI-enabled configurations using STACK and RDS placement for different number of layers.

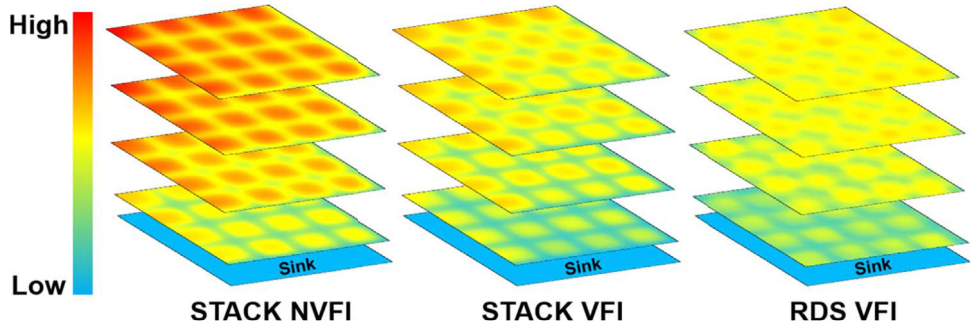

Fig. 18. Thermal map for 4-layer 3D SWNoC architecture with NVFI and VFI configurations using STACK and RDS vertical placement of the WATER benchmark (as a case study). The VFI-enabled architecture significantly removes the thermal hotspots (mostly for the layers away from the heat sink) as found predominantly in the STACK NVFI architecture. The RDS VFI configuration achieves the best temperature profile among all of them.

(RDS VFI) in addition to the lowering the total power dissipation, also distributes all the high-power consuming cores over the whole chip area to alleviate the thermal hotspots. Consequently, it reduces the maximum and average temperature of the system significantly. As a result, the joint effects of both VFI and RDS have the maximum influence in improving the thermal profile. By combining the result from Figs. 14 and 15, it is seen that the SWNoC with VFI configuration using RDS placement shows on an average 25.1% less maximum temperature than that of the STACK NVFI configuration. So, we can conclude that VFI-based power management methodology along with RDS-based vertical placement can improve the thermal profile of the 3D SWNoC significantly.

5.3.3. *Trade-off summary*

To summarize the performance and temperature profiles of all 3D NoC architectures considered here, we show the variation of average EDP and maximum temperature profiles by changing the number of planar layers in Fig. 19. From this figure, it is evident that the VFI-enabled 3D SWNoC achieves both better performance and thermal profile for any number of layers compared to the MESH-based counterparts. To resolve the thermal hotspot issues, we employed RDS-based vertical placement and associated floor planning to lower the maximum temperature of the system by incurring a small amount of EDP penalty compared to STACK-based design. We demonstrated that, the VFI-enabled power management methodology along with the RDS-based floor planning achieves the best PTP trade-offs for the 3D manycore chip.

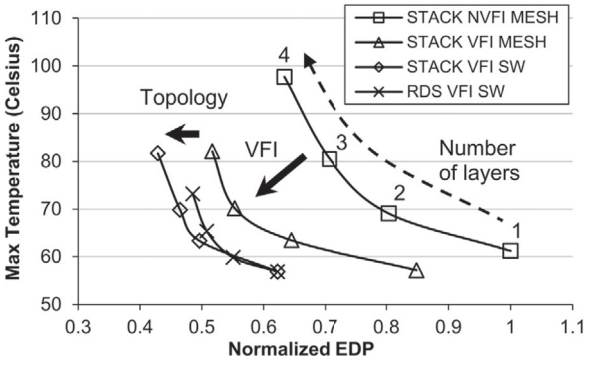

Fig. 19. Average EDP and maximum temperature profiles of STACK NVFI-MESH, STACK VFI-MESH, STACK VFI-SWNoC and RDS VFI-SWNoC (averaged over all benchmarks).

6. Conclusion

In 3D NoCs, stacking more layers improves the achievable performance and energy efficiency of the manycore platforms. However,

stacking a high number of planar layers while keeping the total foot-print area, increases the power density of the system and subsequently, it introduces thermal hotspots in the manycore chip. In this paper, we present a detailed design methodology of an energy- and thermal-efficient 3D NoC architecture incorporating VFI-based power management and RDS-based floor planning. The use of small-world network-enabled 3D NoC (SWNoC) architecture enables performance improvement over conventional MESH-based counterparts while incorporation of VFI-based power management improves both the energy efficiency and thermal profile. We demonstrate that the VFI-enabled 3D SWNoC achieves on an average 57.3% lower EDP than conventional 2D MESH-based architecture. By incorporating RDS-based floor planning, we alleviate the thermal hotspots and thereby, improve the overall thermal profiles. The 3D SWNoC architecture while incorporating both the VFI and RDS techniques lowers the maximum temperature by 25.1% on an average compared to the conventional non-VFI counterpart. Finally, the proposed performance-thermal co-design (PTO) approach for 3D SWNoC improves the thermal profile by 18.9% while incurring only 2.2% performance penalty compared to only performance oriented (PO) 3D SWNoC architecture.

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