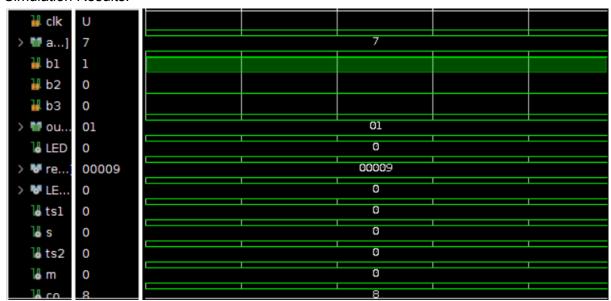
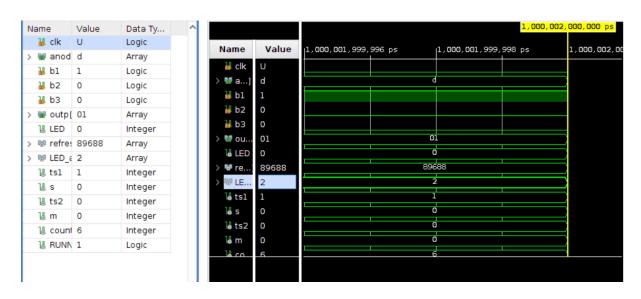
## **ASSIGNMENT 6:**

Roshan Raj(2019CS50437) Anannya Mathur(2019TT10953)

We reduced the 100Mhz on-board clock to 10 Hz. We used three modulo-10 counters and one modulo-6 counter. The rate of individual anode activation was kept at around 300-400Hz.

## Simulation Results:





## Constraints file(.xdc)-

```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports clk]
set_property IOSTANDARD LYCMOS33 [get_ports clk]
```

```
##7 segment display
set property PACKAGE PIN W7 [get ports {outp[6]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {outp[6]}]
set_property PACKAGE_PIN W6 [get_ports {outp[5]}]
    set property IOSTANDARD LVCMOS33 [get ports {outp[5]}]
set property PACKAGE PIN U8 [get ports {outp[4]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {outp[4]}]
set property PACKAGE PIN V8 [get ports {outp[3]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {outp[3]}]
set property PACKAGE_PIN U5 [get_ports {outp[2]}]
    set property IOSTANDARD LVCMOS33 [get ports {outp[2]}]
set property PACKAGE PIN V5 [get ports {outp[1]}]
    set property IOSTANDARD LVCMOS33 [get ports {outp[1]}]
set_property PACKAGE_PIN U7 (get_ports {outp[0]})
    set property IOSTANDARD LVCMOS33 [get ports {outp[0]}]
set property PACKAGE PIN U2 [get ports {anode[0]}]
    set property IOSTANDARD LVCMOS33 [get ports {anode[0]}]
set property PACKAGE PIN U4 [get ports {anode[1]}]
    set_property IOSTANDARD LVCMOS33 [get_ports {anode[1]}]
set_property PACKAGE_PIN V4 [get_ports {anode[2]}]
    set property IOSTANDARD LVCMOS33 [get ports {anode[2]}]
set property PACKAGE PIN W4 [get ports {anode[3]}]
    set property IOSTANDARD LVCMOS33 [get ports {anode[3]}]
set property PACKAGE PIN W19 [get ports b1]
    set_property IOSTANDARD LVCMOS33 [get_ports b1]
set property PACKAGE_PIN T17 [get_ports b2]
    set property IOSTANDARD LVCMOS33 [get ports b2]
set property PACKAGE PIN U17 [get ports b3]
    set property IOSTANDARD LVCMOS33 [get ports b3]
set property CLOCK DEDICATED ROUTE FALSE(get nets bl IBUF)
set property CLOCK DEDICATED ROUTE FALSE(get nets b2 IBUF)
set property CLOCK DEDICATED ROUTE FALSE(get nets b3 IBUF)
```

## Resource count-

LUT-32 Flip Flops-61 BRAMs-0 URAM-0 DSP-0

