M = 20190953
S= {0, 1, 2, 3, 5, 9}

Dec	Bin
0	0000
1	0001
2	0010
3	0011
5	0101
9	1001

Dec	Bin	A	B	C	D	E	F	G
0	0000	1	1	1	1	1	1	0
1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	1	1	1	1	0	0	1
5	0101	1	0	1	1	0	1	1
9	1001	1	1	1	1	0	1	1

Using the above table,

a) For design 1:
   We consider each output separately, i.e., 4 inputs and 1 output.
   Let us consider segment A to demonstrate our approach:
   For A:

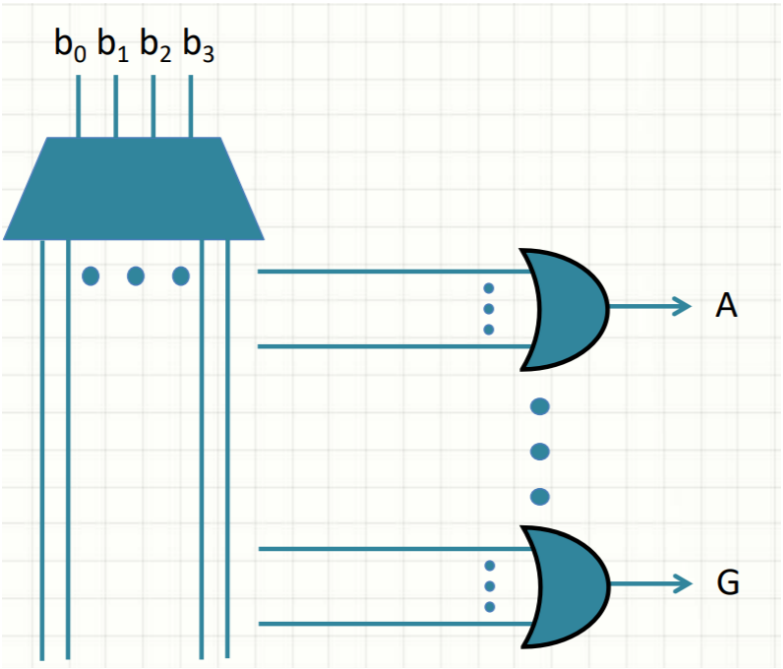
	b3	b2	b1	b0	y
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1

4	0	1	0	0	-
5	0	1	0	1	1
6	0	1	1	0	-
7	0	1	1	1	-
8	1	0	0	0	-
9	1	0	0	1	1
10	1	0	1	0	-
11	1	0	1	1	-
12	1	1	0	0	-
13	1	1	0	1	-
14	1	1	1	0	-
15	1	1	1	1	-

- represents “Don’t cares”.

We then plot the Karnaugh map to find an effective solution.
Similarly, we do the above steps for segments B, C, D, E, F, G and build logic circuits for each of them.

b) For design 2,
We consider all outputs together while also ensuring that there is a maximum sharing of gates, i.e., 4 inputs and 7 outputs.
The final circuit will look something like this:


b_0 b_1 b_2 b_3
A
G