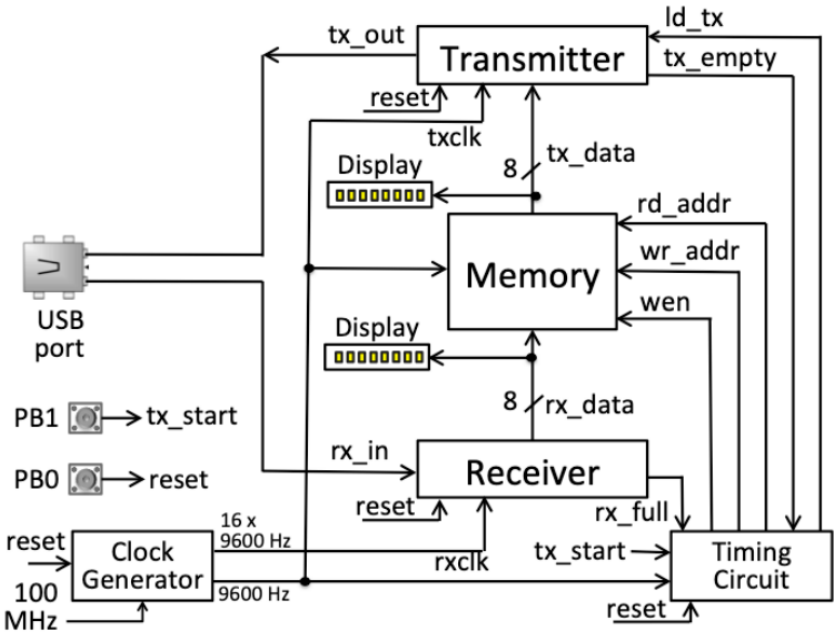
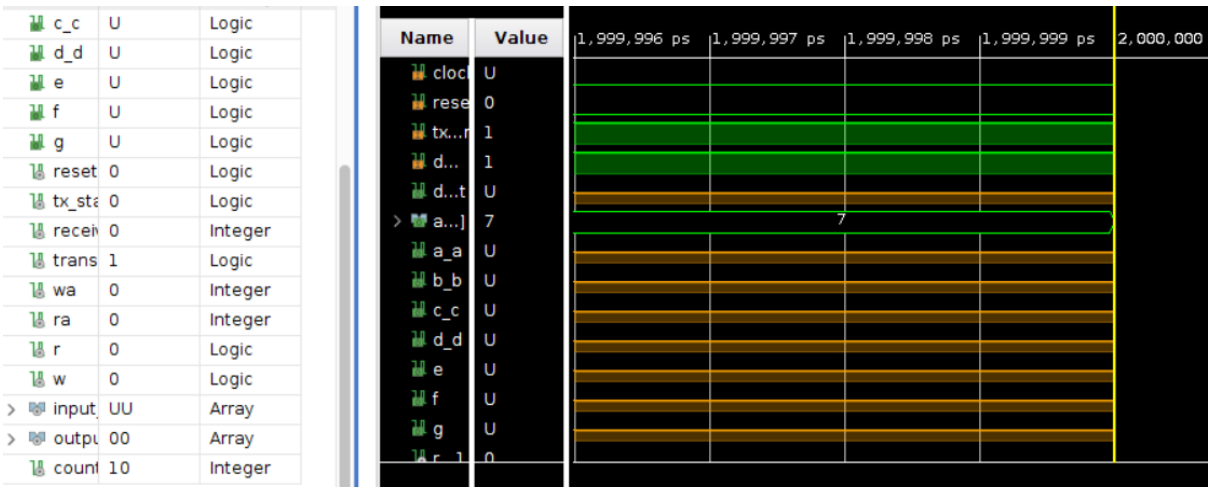
Assignment 10
Roshan Raj(2019CS50437) Anannya Mathur(2019TT10953)

The A10 code consists of four parts- receiver, transmitter, BRAM, and timing circuit. We have used read first mode for our BRAM component. We used our codes of A8 for the receiver-transmitter pair, keeping in view a few changes to accommodate the needs of A10. Whenever the receiver reaches its final stop state, it outputs 1 to indicate that the received bits should be stored in memory. On the other hand, if the start signal for transmission was enabled, the transmitter passed the '1' value whenever in its idle state to indicate it is ready to receive the next set of bits and that the read signal must be enabled to read from memory. We also used the 7-segment displays for debugging purposes. The leftmost two anodes were used for the received bits, and the rightmost two anodes were used to display the transmitted bits. We have tried to implement the suggested block diagram as given in the assignment description-

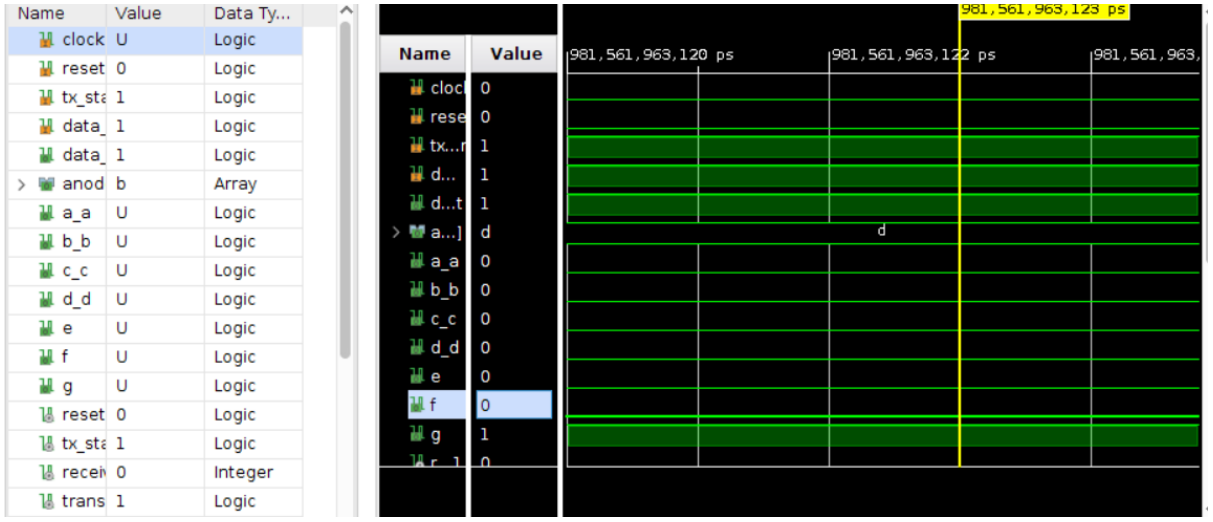


The timing circuit was inspired by our A9 code on FIFO implementation.
We used 16 bits as the width and 256 bits as the depth for the BRAM component.

Simulation Results-
Clock of period 1000ns-



Clock of period 1s-



Resource count-
LUT-110
FF-152
BRAM-0.5
URAM-0
DSP-0