Assignment-8

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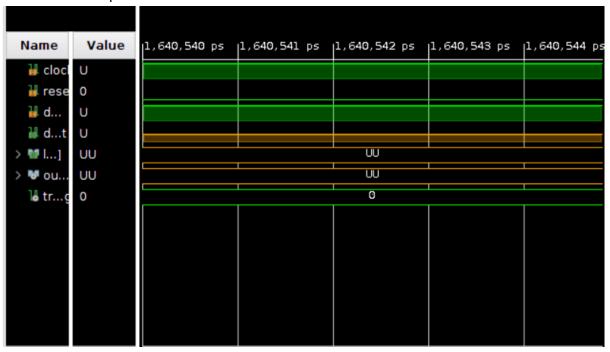
For the transmission of data bits passed by the receiver, we have used a clock that operates at the baud rate of 9600Hz. We have not considered the parity bits.

For receiving the bits, we used the receiver code from A7. In addition to the existing A7 code, we maintained a stop_transmit counter to track when the transmission of bits must end. The default value was kept at 0. It turned 1 in the stop state while the duration counter was less than 15. It turned back to 0 in the idle state. Also, we output the receiving bits in the data_receive state just when the bits_read counter turns 7. This was done to ensure no delay between receiving and transmission of bits.

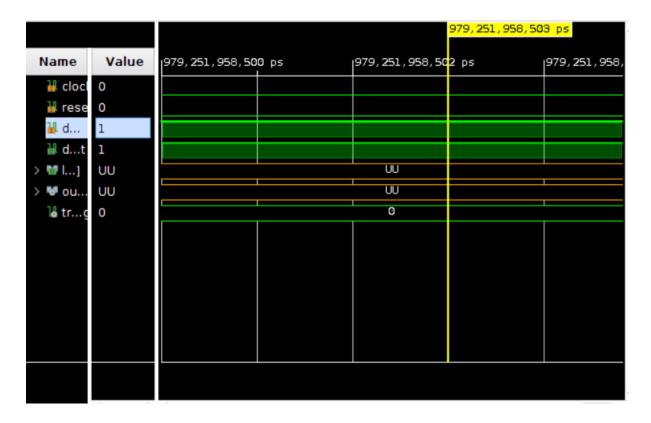
Transmitter:

We maintain four states-idle, start, data_receive and stop. The default state is idle. If the reset button is pressed, the state is returned to the idle state. We check for the stop_transmit value passed to the code from the receiver module. If the value is 1, the eight bits received from the receiver are passed to the transmission module to be processed. The state conversion from idle to start happens only when the stop_transmit counter becomes 1. In the idle state and the stop state, we output '1' to indicate the stop bit, while in the start state, we output '0' to indicate the start bit. From the start state, the state goes to the data_read state, where the 8 bits of the received bits are output one after another. Once the 8 bits are read, the state goes to the final stop state, which prepares the idle state for the next set of bits.

Simulation Results-Clock of 1000ns period:



Clock of period 1s:

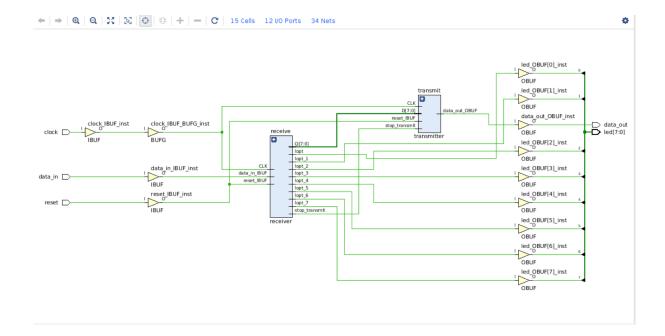


The code is able to receive and transmit back the sent bits to the PC.

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Constraints file-
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To receive and transmit the bits back to the PC-
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Resource count-



LUT-74 Flip Flops-79 BRAMs-0 URAM-0 DSP-0