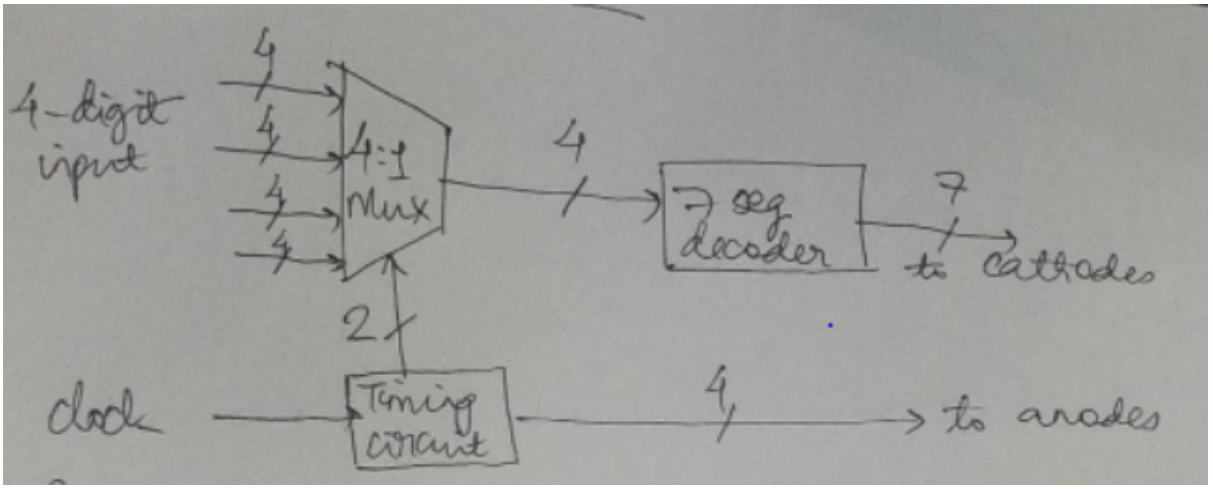
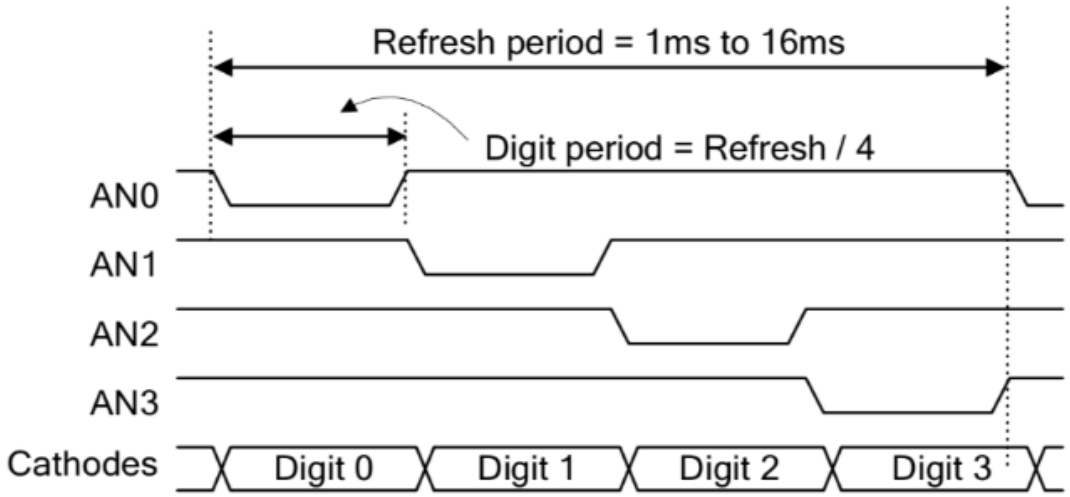
Assignment 3

Roshan Raj(2019CS50437) Anannya Mathur(2019TT10953)

Circuit design:



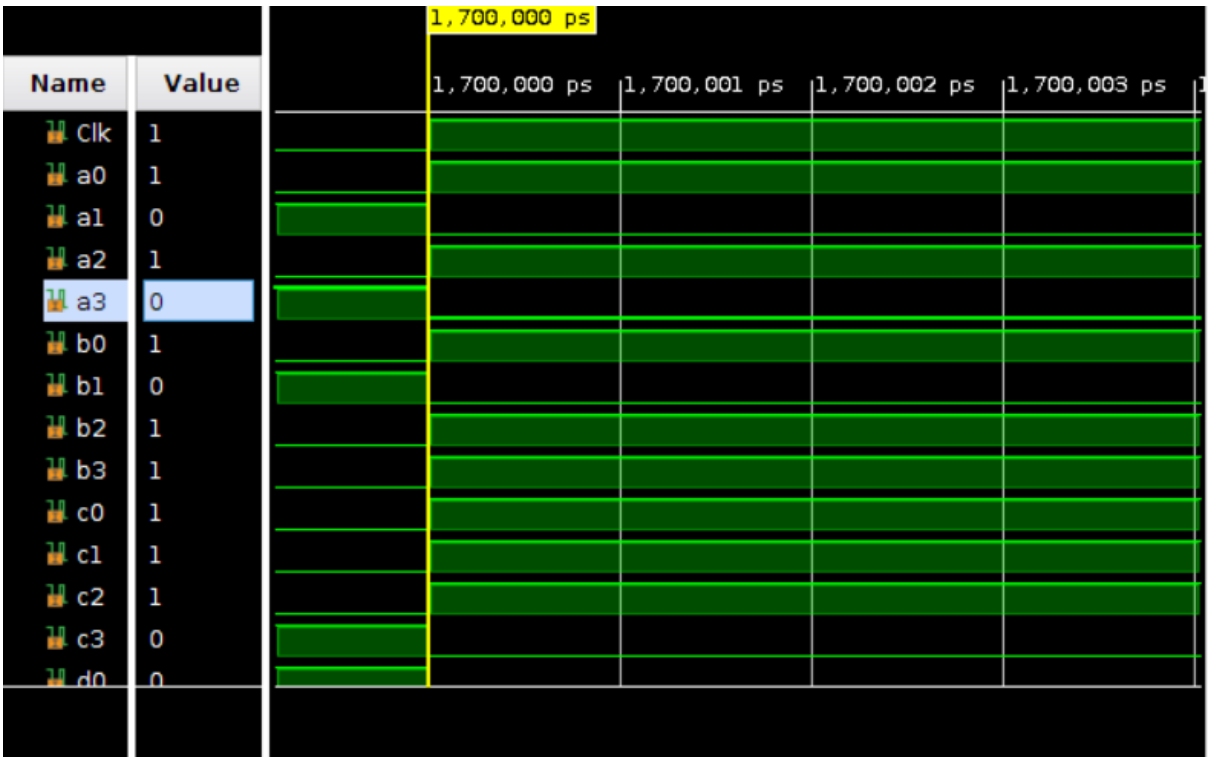
Timing Circuit:

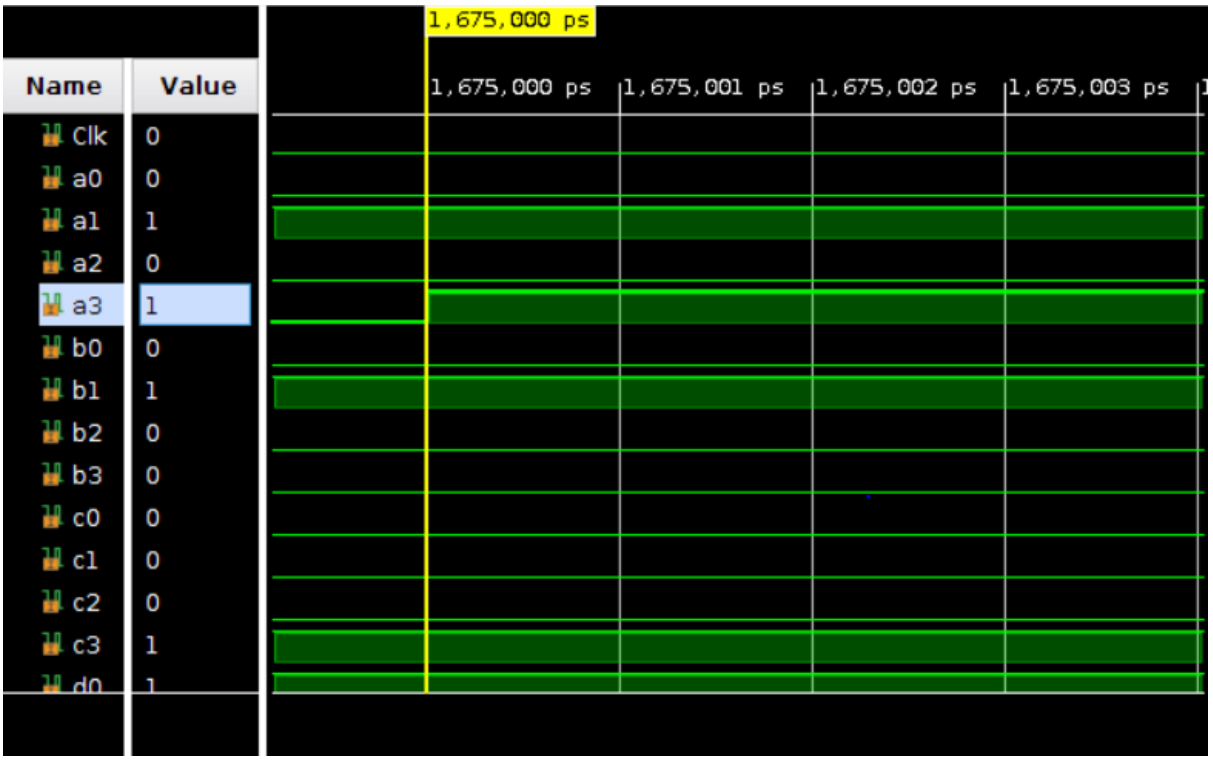


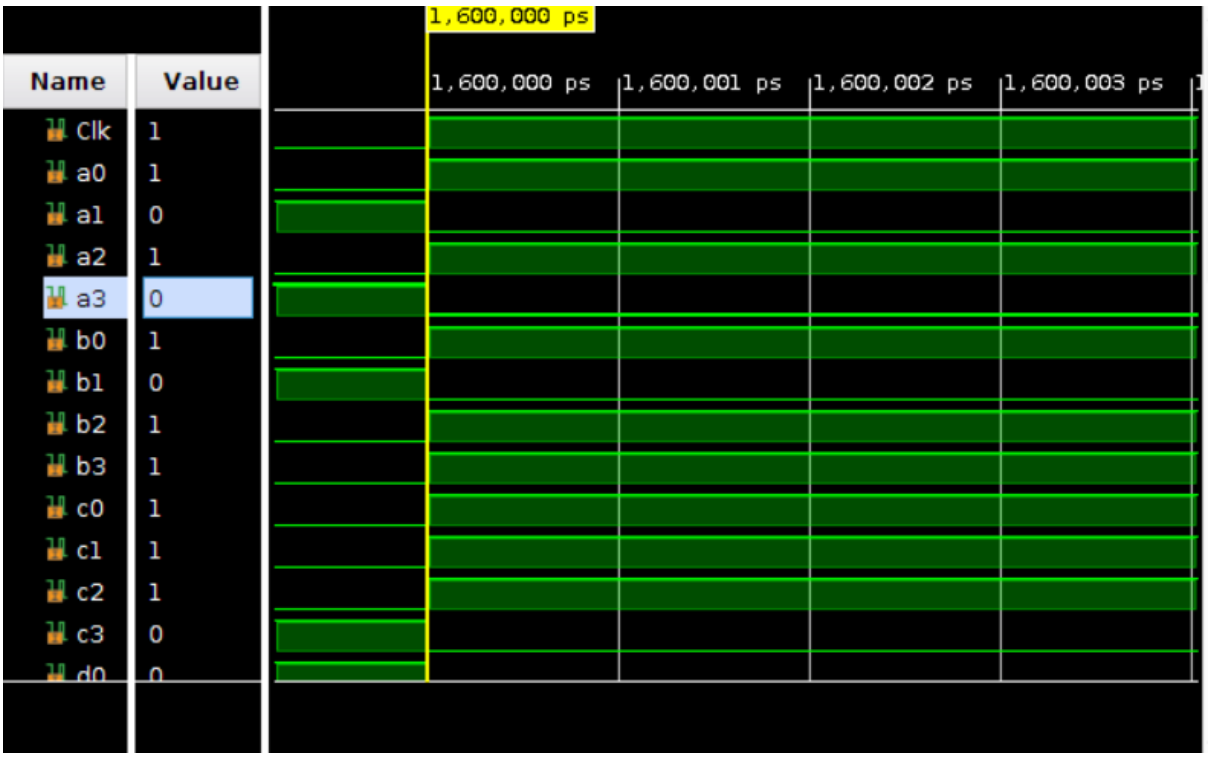
The clock frequency needs to be in the range of 250 Hz to 4000Hz. The on-board clock is 100 MHz which needs to be divided suitably. For this purpose, we used 16 T Flip-Flops, which reduced the frequency to 1525.88 Hz.

To activate the anodes for every digit, we used the last two states produced by our timer- “00”, “01”, “10”, and “11”. Similarly, we used these states to determine which of the four digits to display.

Simulation Results:


1,700,000 ps
Name
Value
1,700,000 ps
1,700,001 ps
1,700,002 ps
1,700,003 ps
Clk 1
a0 1
a1 0
a2 1
a3 0
b0 1
b1 0
b2 1
b3 1
c0 1
c1 1
c2 1
c3 0
d0 0


1,675,000 ps
Name
Value
1,675,000 ps
1,675,001 ps
1,675,002 ps
1,675,003 ps
Clk 0
a0 0
a1 1
a2 0
a3 1
b0 0
b1 1
b2 0
b3 0
c0 0
c1 0
c2 0
c3 1
d0 1



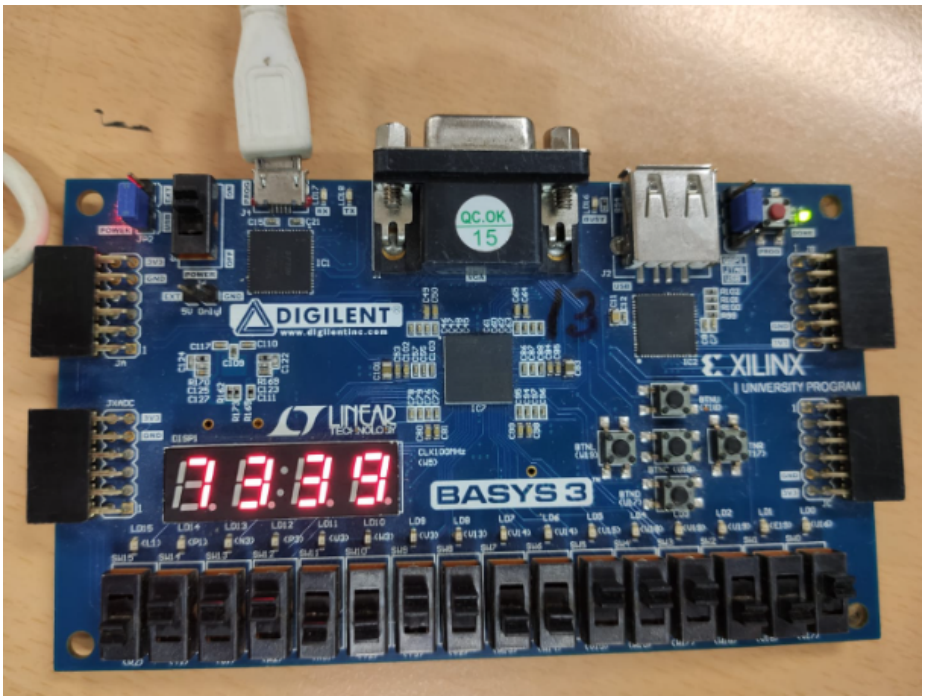
Constraints file(.xdc)-

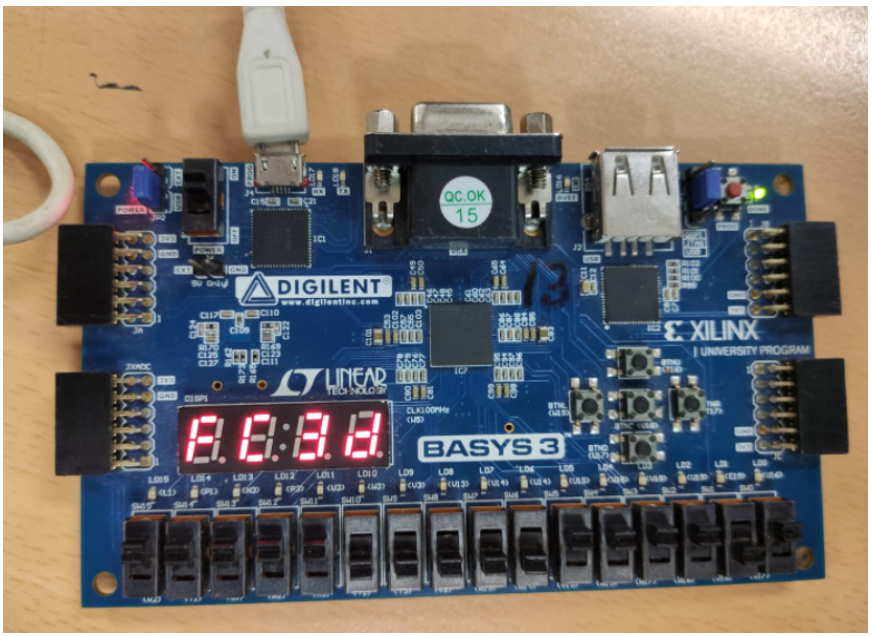
```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports Clk]
        set_property IOSTANDARD LVCMOS33 [get_ports Clk]
        create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports Clk]
```

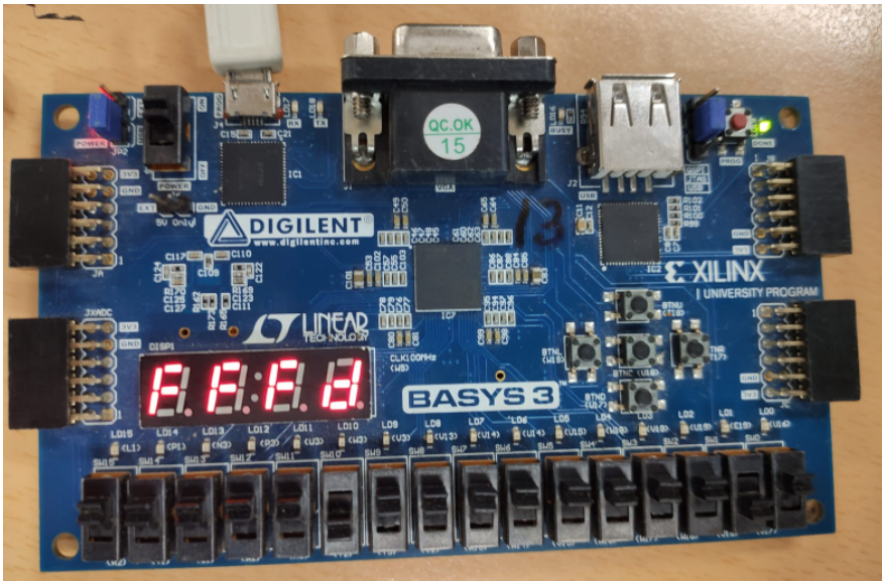
a0, a1, a2, a3, b0, b1, b2, b3, c0, c1, c2, c3, d0, d1, d2, d3- 4 digits of 4 bits as input-

```
## Switches
set_property PACKAGE_PIN V17 [get_ports {a3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {a3}]
set_property PACKAGE_PIN V16 [get_ports {a2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {a2}]
set_property PACKAGE_PIN W16 [get_ports {a1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {a1}]
set_property PACKAGE_PIN W17 [get_ports {a0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {a0}]
set_property PACKAGE_PIN W15 [get_ports {b3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b3}]
set_property PACKAGE_PIN V15 [get_ports {b2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b2}]
set_property PACKAGE_PIN W14 [get_ports {b1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b1}]
set_property PACKAGE_PIN W13 [get_ports {b0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b0}]
set_property PACKAGE_PIN V2 [get_ports {c3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {c3}]
set_property PACKAGE_PIN T3 [get_ports {c2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {c2}]
set_property PACKAGE_PIN T2 [get_ports {c1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {c1}]
set_property PACKAGE_PIN R3 [get_ports {c0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {c0}]
set_property PACKAGE_PIN W2 [get_ports {d3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d3}]
set_property PACKAGE_PIN U1 [get_ports {d2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d2}]

set_property PACKAGE_PIN T1 [get_ports {d1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d1}]
set_property PACKAGE_PIN R2 [get_ports {d0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d0}]
```

```
##7 segment display
set_property PACKAGE_PIN W7 [get_ports {A}]
        set_property IOSTANDARD LVCMOS33 [get_ports {A}]
set_property PACKAGE_PIN W6 [get_ports {B}]
        set_property IOSTANDARD LVCMOS33 [get_ports {B}]
set_property PACKAGE_PIN U8 [get_ports {C}]
        set_property IOSTANDARD LVCMOS33 [get_ports {C}]
set_property PACKAGE_PIN V8 [get_ports {D}]
        set_property IOSTANDARD LVCMOS33 [get_ports {D}]
set_property PACKAGE_PIN U5 [get_ports {E}]
        set_property IOSTANDARD LVCMOS33 [get_ports {E}]
set_property PACKAGE_PIN V5 [get_ports {F}]
        set_property IOSTANDARD LVCMOS33 [get_ports {F}]
set_property PACKAGE_PIN U7 [get_ports {G}]
        set_property IOSTANDARD LVCMOS33 [get_ports {G}]

set_property PACKAGE_PIN V7 [get_ports dp]
        set_property IOSTANDARD LVCMOS33 [get_ports dp]

set_property PACKAGE_PIN U2 [get_ports {Anode0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Anode0}]
set_property PACKAGE_PIN U4 [get_ports {Anode1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Anode1}]
set_property PACKAGE_PIN V4 [get_ports {Anode2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Anode2}]
set_property PACKAGE_PIN W4 [get_ports {Anode3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {Anode3}]
```




QC.OK
15
DIGILENT
XILINX
UNIVERSITY PROGRAM
LINEAR TECHNOLOGY
BASYS 3


QC.OK
15
DIGILENT
XILINX
UNIVERSITY PROGRAM
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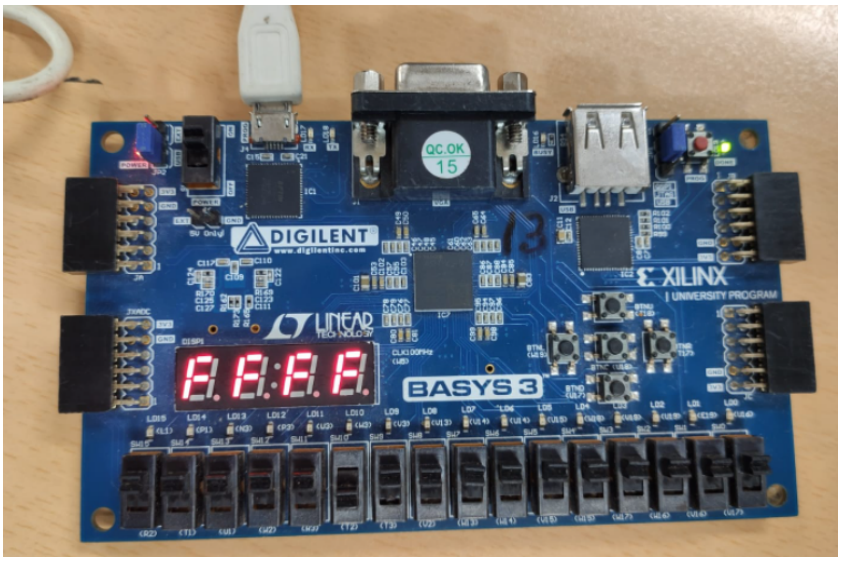
BASYS 3


QC.OK
15
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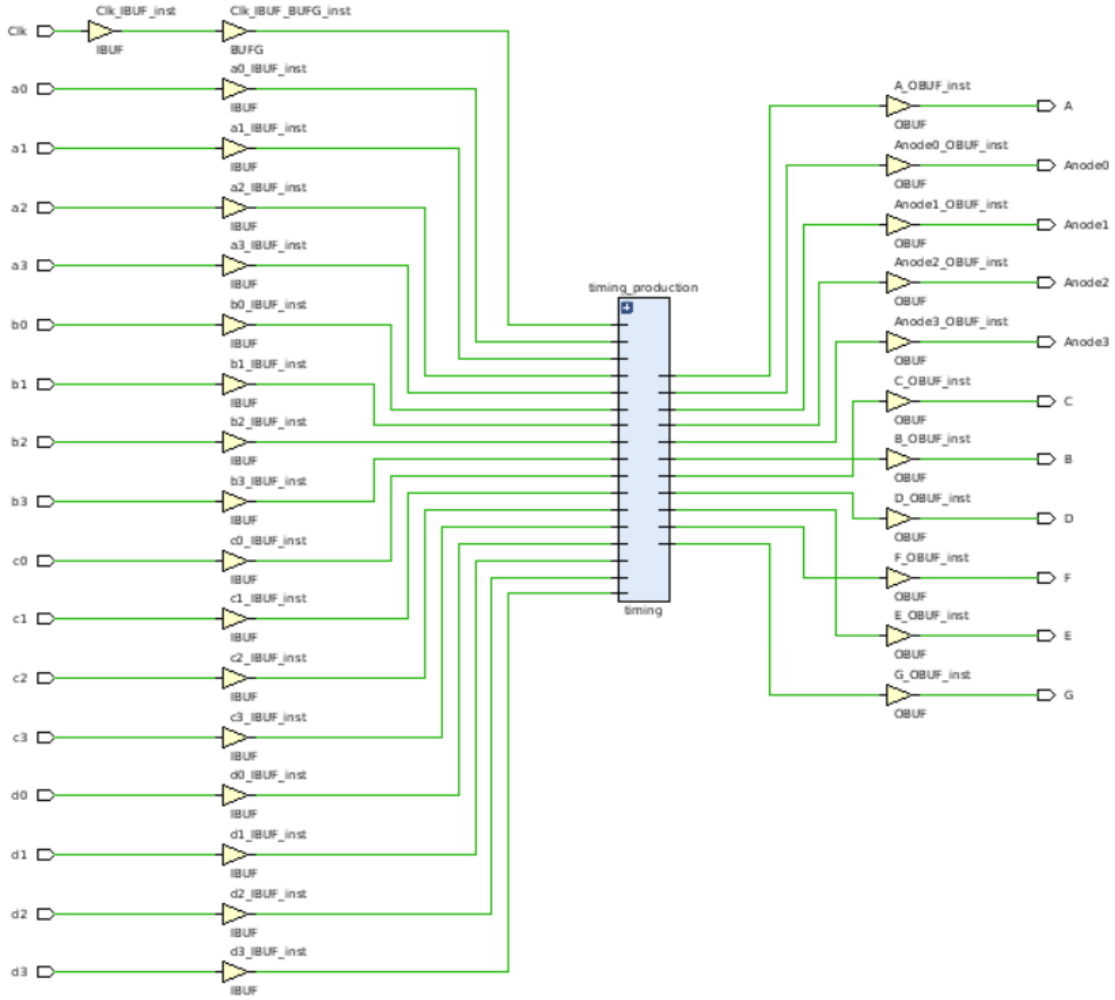
BASYS 3

Resource count:
LUT-24
Flip Flops-15
BRAMs-0
URAM-0
DSP-0



Observations- We observe that our results match the expected values; thus, we can conclude that our algorithm works right.