Assignment 9
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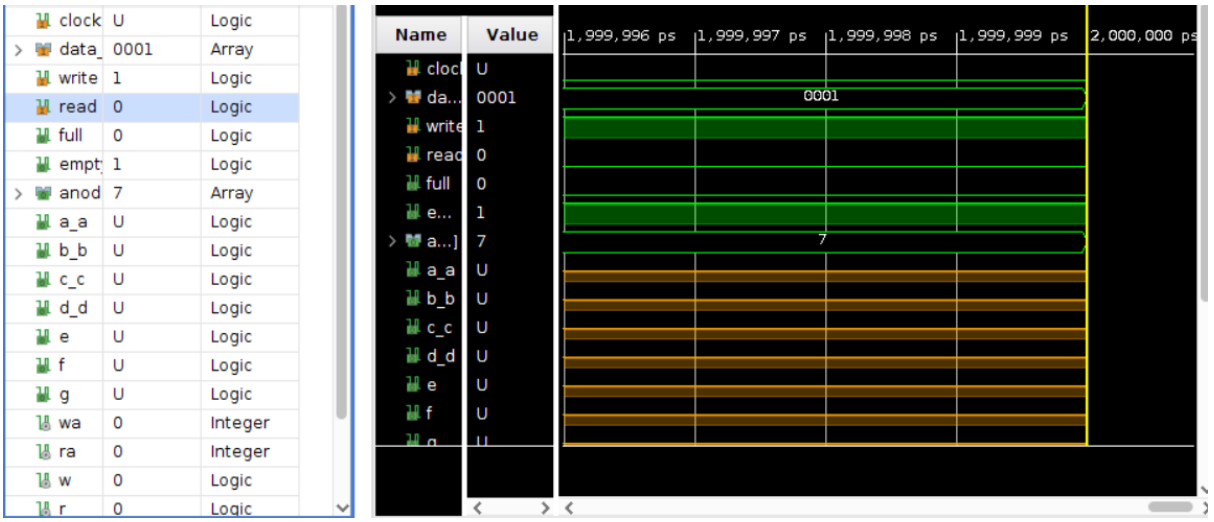
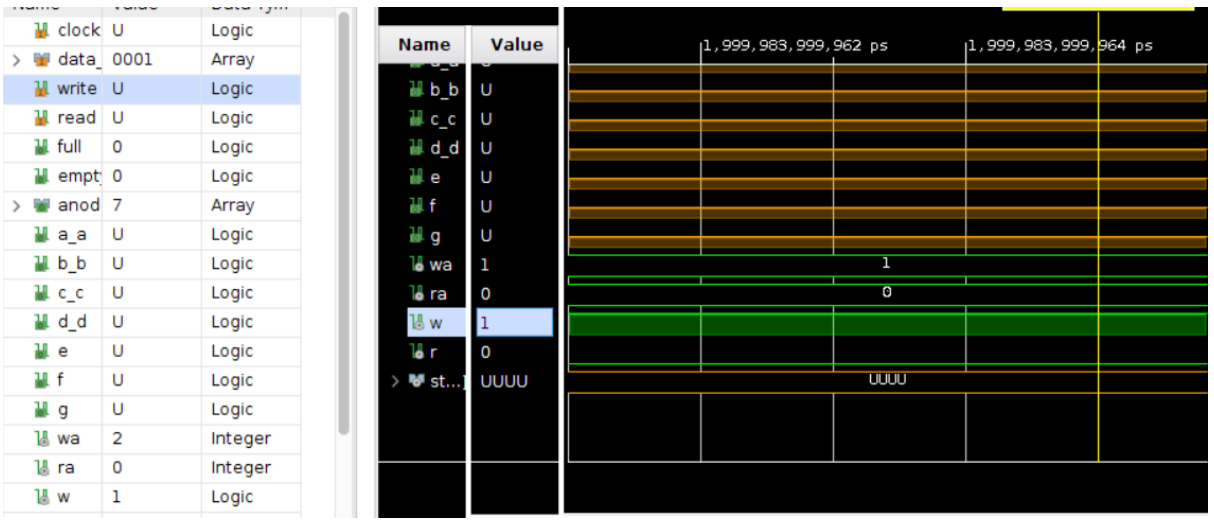
We first built a BRAM component with ports for reading, writing, read address, write address, and a common clock for reading and writing functions. We have used read first mode for our BRAM component. To ensure we do not end up reading an empty FIFO or writing into a full FIFO, we maintained a pointer with an initial value of 0. Whenever the read signal was enabled, we kept the 0 value to the pointer but updated it to 1 on receiving a write enable signal. At every operation, we checked if the write and read addresses reached the same value. In case they did, we checked for the value contained by the pointer. If it was 1, we declared FIFO full; otherwise, it was stated empty.

We used 16 bits as the width and 256 bits as the depth for the BRAM component.
Here, 16 bits correspond to input taken by the user from the 16 slide switches. We used two push buttons for write and read operations.

Simulation Results-
Clock of period 1000ns-



Clock of period 1s-



Resource count-
LUT-45
FF-63
BRAM-0.5
URAM-0
DSP-0