Single port BRAM

Question: Design single port BRAM, of depth 2048 bits and width 16 bits, how many 36K BRAM does it consume?

Verilog code:

```
module singlePort_BRAM(
   input clk,
   input we,
   input [10:0] addr,
   input [15:0] din,
   output reg [15:0] dout
   );
   (* ram_type="block" *)
   reg [15:0] mem [0:2047];
   always @(posedge clk) begin
   if (we) begin
   mem[addr]<=din;
   end
   dout <= mem[addr];
   end
endmodule
```

Schematics:

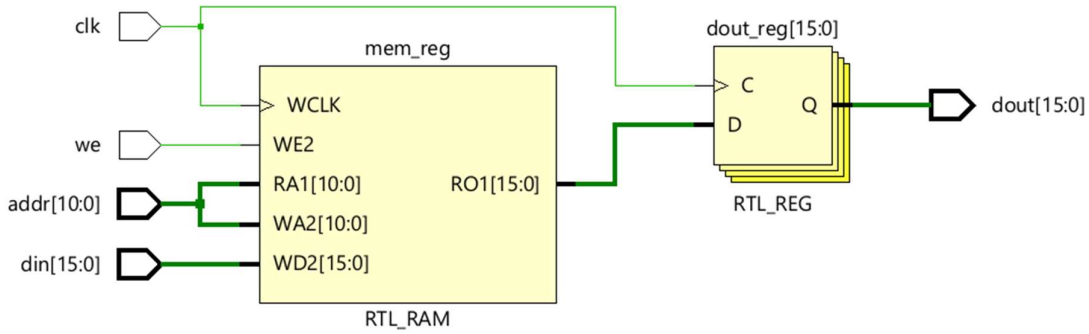

Figure 1: RTL Schematic

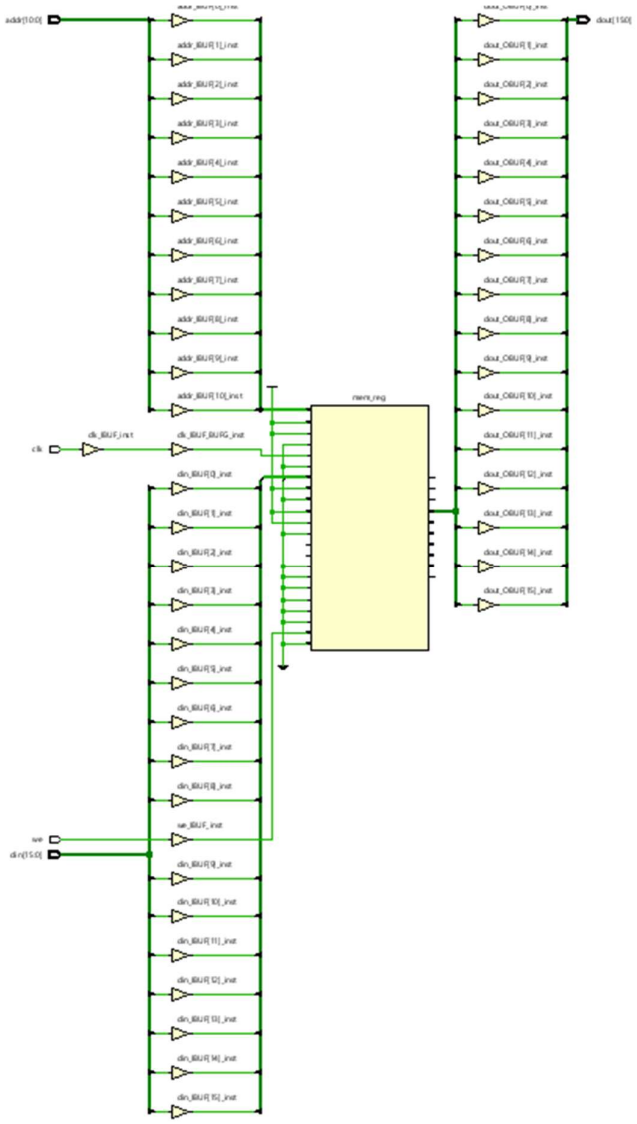

Figure 2: Synthesized Schematic

Observation: One block of 36Kb BRAM (RAMB36E1) is sufficient, as the total bits is 16*2048 = 32768 bits, which is less than total bits of RAMB36E1 i.e, 36*1024=36864 bits.

Logic tables:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	0	0	0	53200	0.00
LUT as Logic	0	0	0	53200	0.00
LUT as Memory	0	0	0	17400	0.00
Slice Registers	0	0	0	106400	0.00
Register as Flip Flop	0	0	0	106400	0.00
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Figure 3: Slice logic table

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	1	0	0	140	0.71
RAMB36/FIFO*	1	0	0	140	0.71
RAMB36E1 only	1				
RAMB18	0	0	0	280	0.00

Figure 4: Memory table