TRUE Dual Port BRAM

Block diagram:

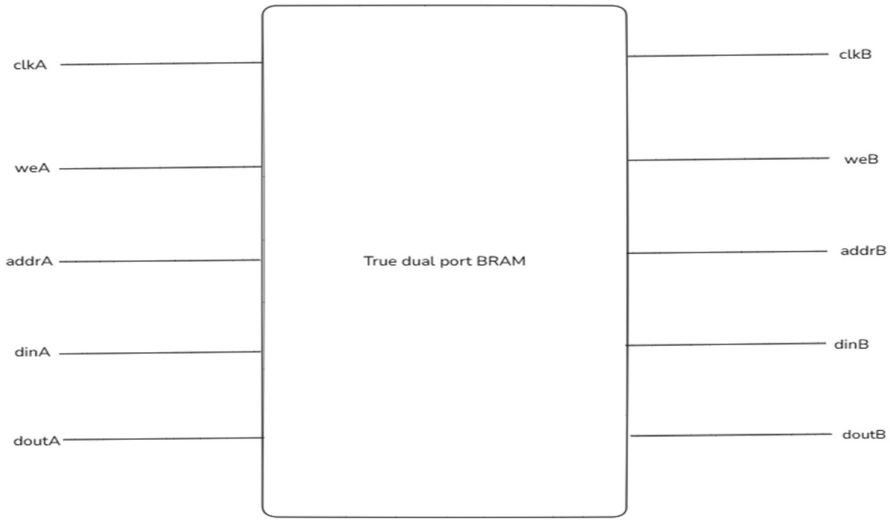

Figure 1: Block diagram

Verilog code:

```
module true_dualPort_BRAM(
input clkA,clkB,weA,weB,
input [13:0] addrA, addrB,
input [31:0] dinA, dinB,
output reg [31:0] doutA, doutB
   );
(* ram_type = "block" *)
reg [31:0] mem [0:16384];

always @(posedge clkA) begin
if (weA) begin
mem[addrA]<= dinA;
end
doutA<=mem[addrA];
```

```
end


always @(posedge clkB) begin
if (weB) begin
mem[addrB]<= dinA;
end
doutB<=mem[addrB];
end

endmodule
```

Schematics:

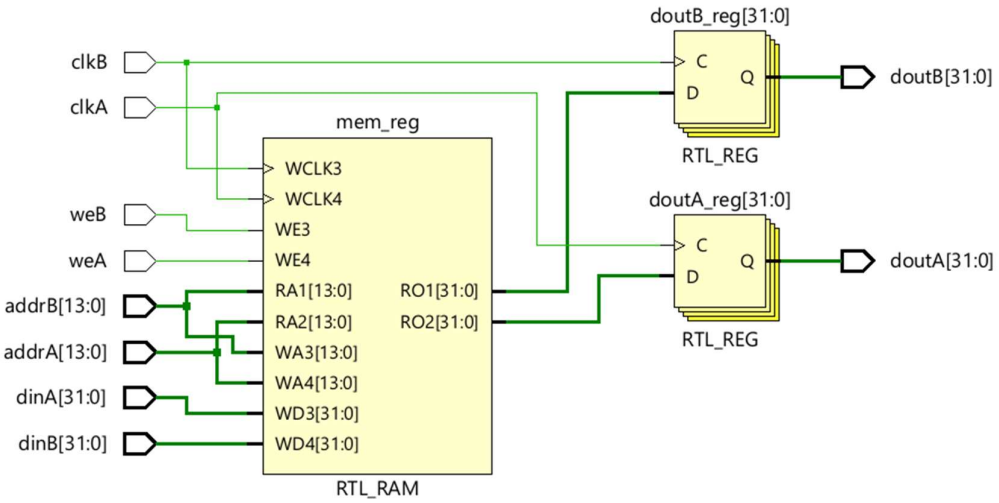

Figure 2: RTL Schematic

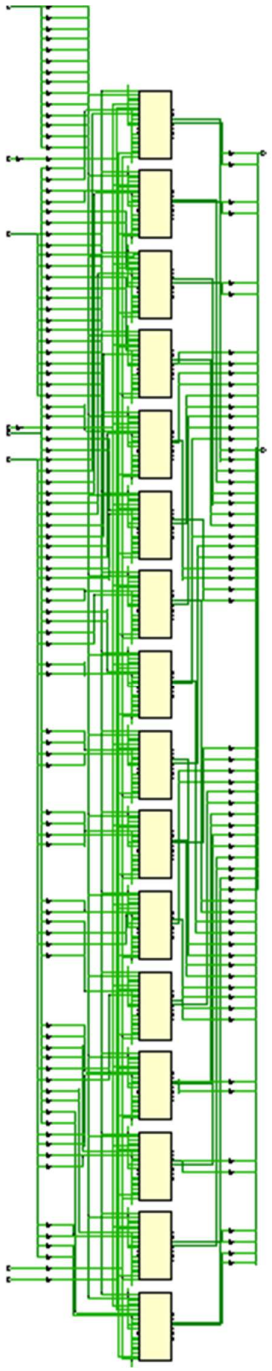

Figure 3: Synthesized schematic

Obseravation: Based on the give requrirement that is 32 bit width and 16K bit depth, 32*16Kb = 524288 bits (512 Kb). Therefore number of 36K block ram is 524288/36864 = 15 blocks.