Distributed BRAM (256 width x 32 depth)

Distributed BRAM: Implemented using LUT’s

As we have 256 various locations to be stored, therefore the address width is $\log_2(256)=8$ and the I/O lines are of 32 bit each. For distributed BRAM asynchronous read is the key part.

Verilog code:

```
module distributed_BRAM(
   input clk,
   input we,
   input [7:0] addr,
   input [31:0] din,
   output [31:0] dout
   );
   (* ram_type="distributed" *)
   reg [31:0] mem [0:255];
   always @(posedge clk) begin
   if (we) begin
   mem[addr]<=din;
   end
   end
   assign dout = mem[addr];
endmodule
```

Schematics:

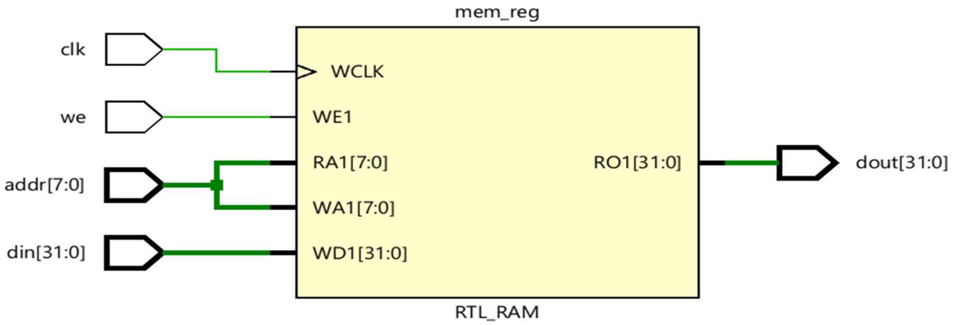


Figure 1: RTL Schematic

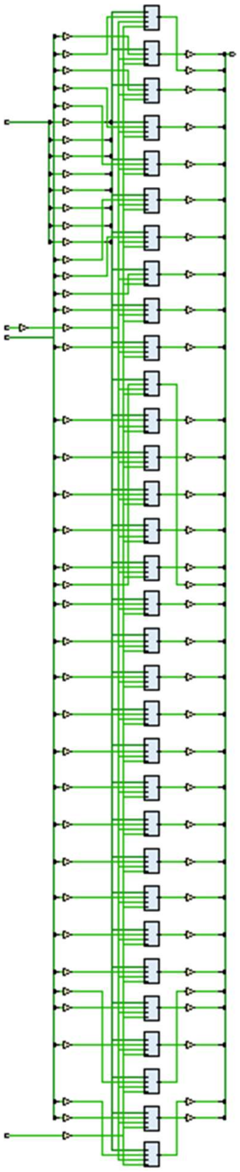
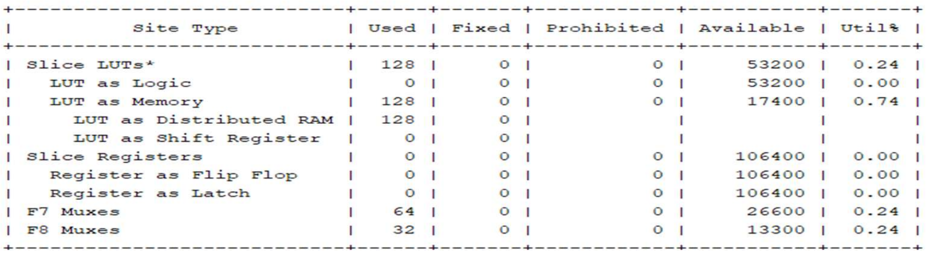


Figure 2: Synthesized Schematic

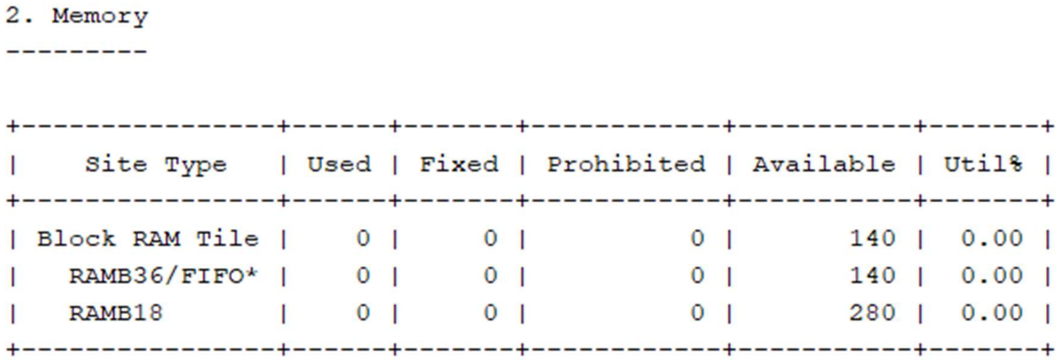
Above schematic the design utilizes block RAM256X1S, which is implemented using the LUT resources. Hence distributed BRAM is properly implemented.

Logic tables:



```
+----------------------------+------+-------+------------+-----------+-------+
|          Site Type         | Used | Fixed | Prohibited | Available | Util% |
+----------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*                |  128 |     0 |          0 |     53200 |  0.24 |
|   LUT as Logic             |    0 |     0 |          0 |     53200 |  0.00 |
|   LUT as Memory            |  128 |     0 |          0 |     17400 |  0.74 |
|     LUT as Distributed RAM |  128 |     0 |            |           |       |
|     LUT as Shift Register  |    0 |     0 |            |           |       |
| Slice Registers            |    0 |     0 |          0 |    106400 |  0.00 |
|   Register as Flip Flop    |    0 |     0 |          0 |    106400 |  0.00 |
|   Register as Latch        |    0 |     0 |          0 |    106400 |  0.00 |
| F7 Muxes                   |   64 |     0 |          0 |     26600 |  0.24 |
| F8 Muxes                   |   32 |     0 |          0 |     13300 |  0.24 |
+----------------------------+------+-------+------------+-----------+-------+
```

Figure 3: Slice logic table



```
2. Memory
---------

+----------------+------+-------+------------+-----------+-------+
|    Site Type   | Used | Fixed | Prohibited | Available | Util% |
+----------------+------+-------+------------+-----------+-------+
| Block RAM Tile |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB36/FIFO* |    0 |     0 |          0 |       140 |  0.00 |
|   RAMB18       |    0 |     0 |          0 |       280 |  0.00 |
+----------------+------+-------+------------+-----------+-------+
```

Figure 4: Memory table