

Negative Edge Detector

Timing diagram:

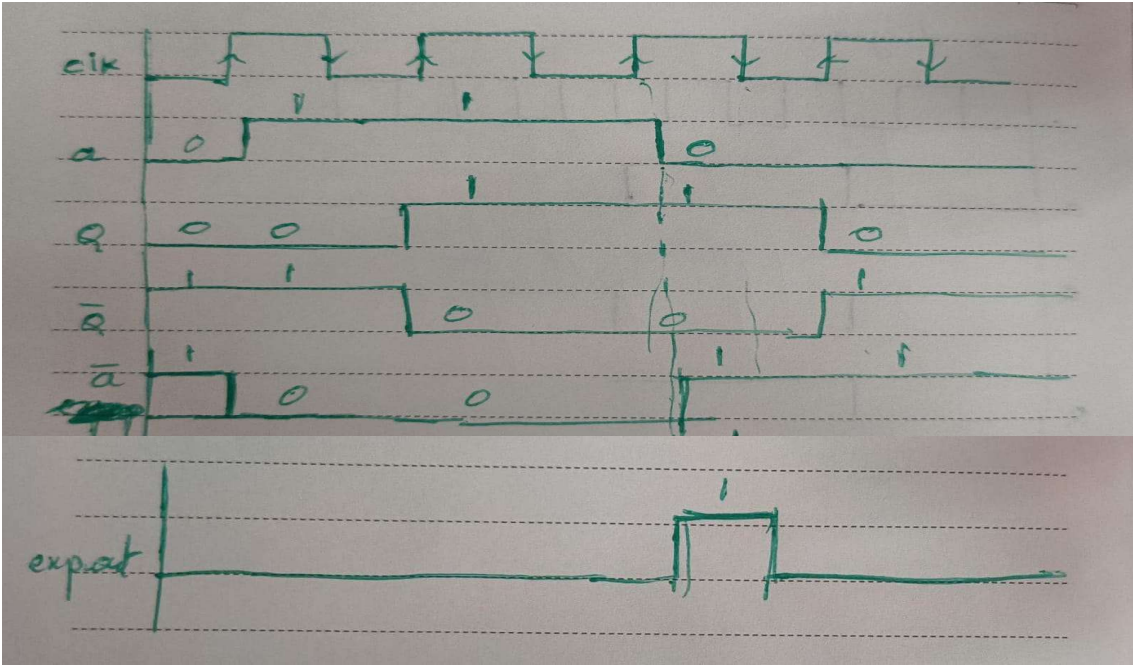


Figure 1: Timing diagram

AND gate truth table:

a'	Q	Y
0	0	0
0	1	0
1	0	0
1	1	1

Block diagram:

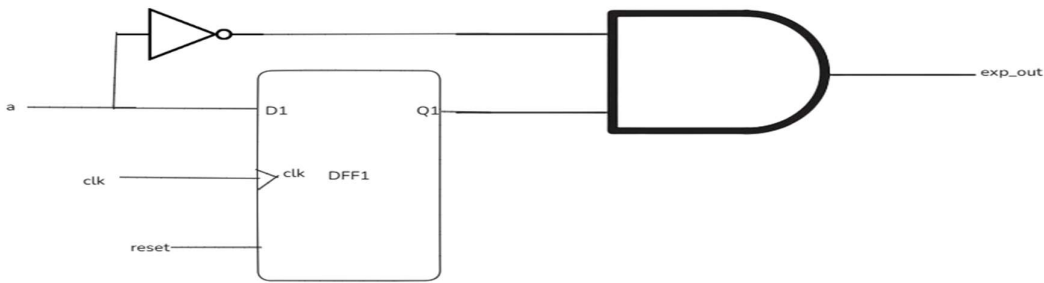


Figure 2: Block diagram for negative edge detector

Schematics:

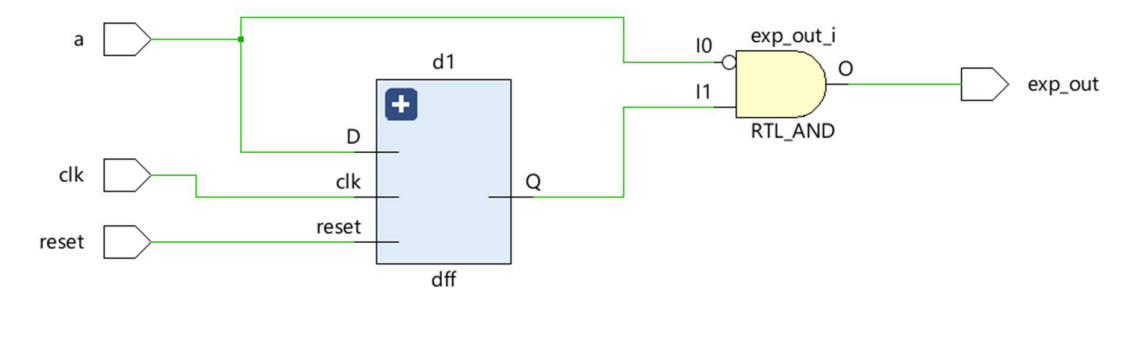


Figure 3: RTL Schematic

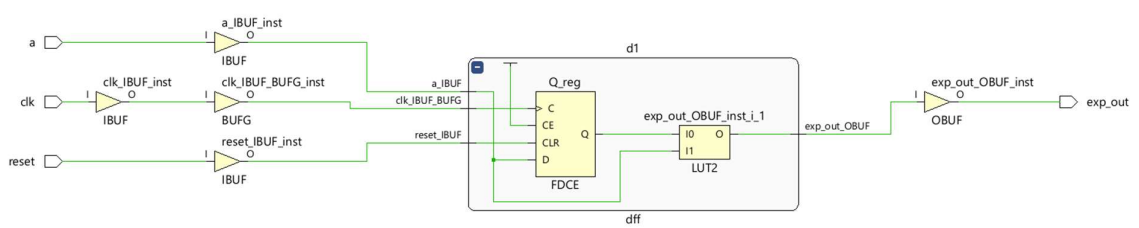


Figure 4: Synthesized Schematic

LUT's:

exp_out_OBUF_inst_i_1		
I1	I0	O=I0 & !I1
0	0	0
0	1	1
1	0	0
1	1	0

Figure 5: LUT2

Verilog code:

```
module negative_edgeDetector(  
    input clk,  
    input reset,  
    input a,  
    output exp_out  
);  
    wire x1,x2;  
    not(x1,a);  
    dff d1(clk,reset,a,x2);  
    and(exp_out,x1,x2);  
endmodule
```

```
module dff(input clk,reset,D,output reg Q);  
    always @(posedge clk or posedge reset) begin  
        if (reset) begin  
            Q<=1'b0;  
        end  
        else begin  
            Q<=D;  
        end  
    end  
endmodule
```

Testbench code:

```
module negative_edgeDetector_tb;  
    reg clk;  
    reg reset;  
    reg a;  
    wire exp_out;
```

```
negative_edgeDetector uut(.clk(clk),.reset(reset),.a(a),.exp_out(exp_out));
```

```
initial begin
```

```
clk=0;
```

```
forever #5 clk=~clk;
```

```
end
```

```
initial begin
```

```
    reset = 1; a = 0;
```

```
    #10;
```

```
    reset = 0;
```

```
    #10; a = 0;
```

```
    #10; a = 1;
```

```
    #10; a = 1;
```

```
    #10; a = 0;
```

```
    #10; a = 0;
```

```
    #10; reset = 1;
```

```
    #10;
```

```
    $finish;
```

```
end
```

```
initial begin
```

```
    $monitor("time = %0t | clk = %b | reset = %b | a = %b | exp_out = %b", $time, clk, reset, a, exp_out);
```

```
end
```

```
endmodule
```

Timing diagram:

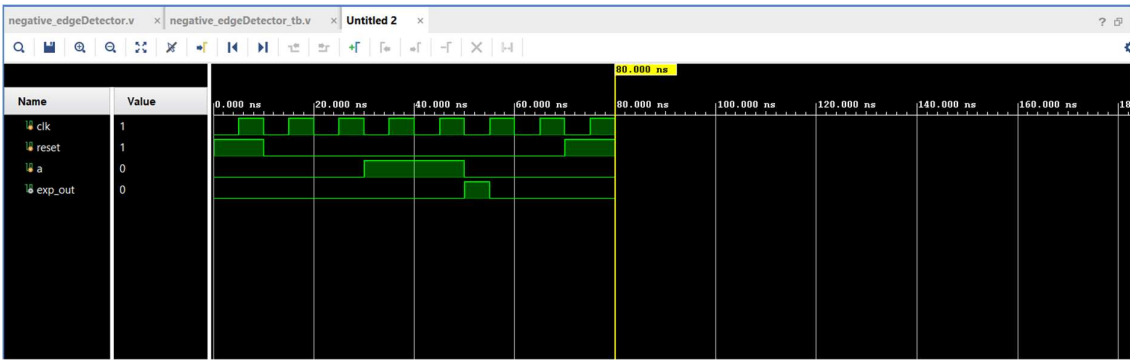


Figure 6: Timing diagram

Slice logic:

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	1	0	0	53200	<0.01
LUT as Logic	1	0	0	53200	<0.01
LUT as Memory	0	0	0	17400	0.00
Slice Registers	1	0	0	106400	<0.01
Register as Flip Flop	1	0	0	106400	<0.01
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Figure 7: Slice logic table