Full Adder

Block Diagram:

Figure 1: Block diagram

Design:

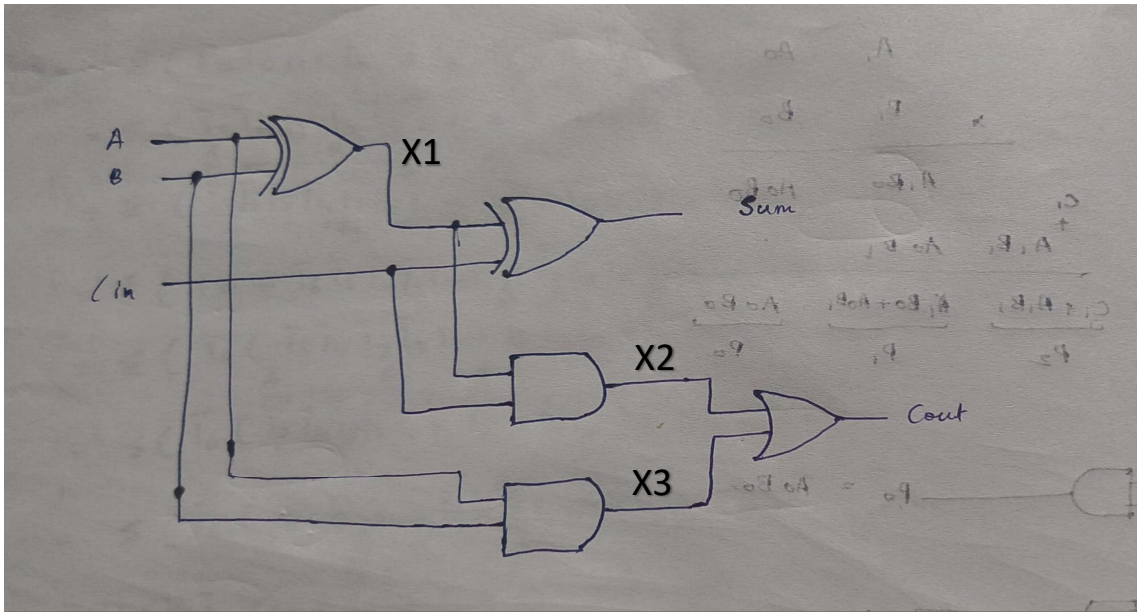

Figure 2: Full adder design

Truth table:

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Kmap:

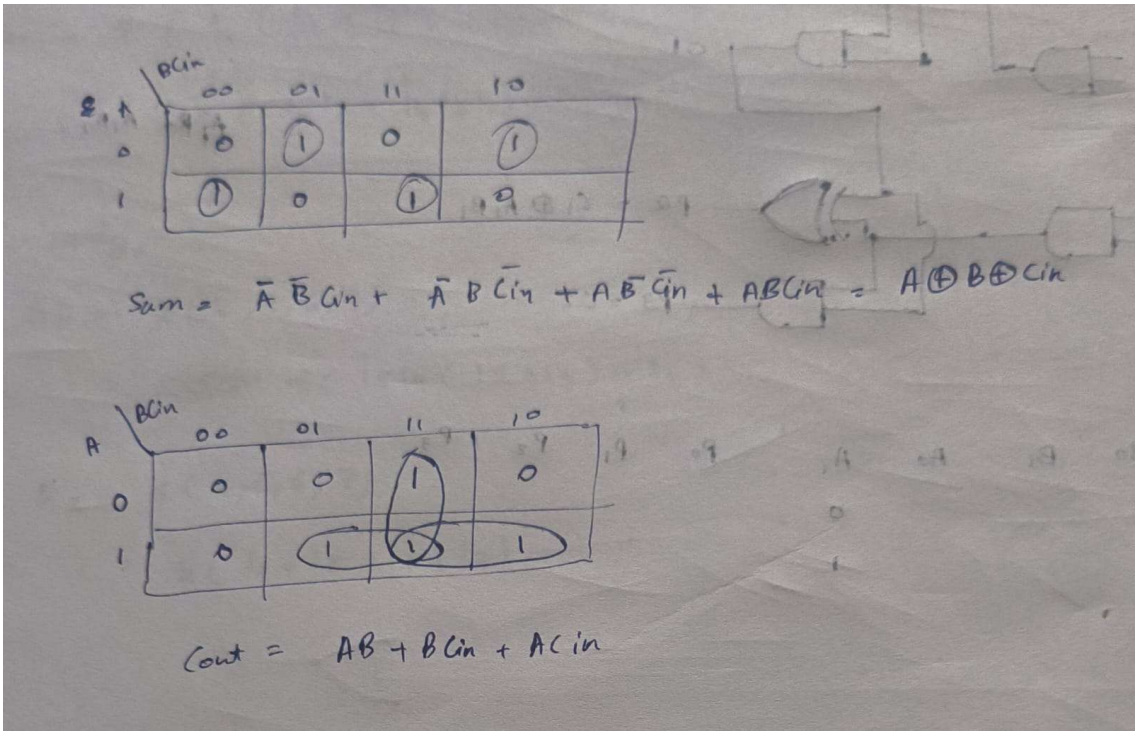

Figure 1: Kmaps for Sum and Cout

Verilog code:

```
// gate level implementation of Full adder
module fullAdder(input A,B,Cin, output Sum, Cout);
wire X1,X2,X3;
xor(X1,A,B);
xor(Sum,X1,Cin);
and(X2,X1,Cin);
and(X3,A,B);
or(Cout,X2,X3);
endmodule
```

Schematics:

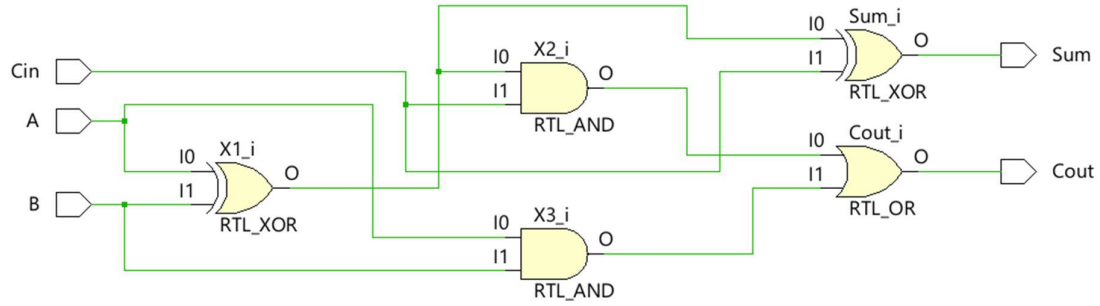

Figure 2: RTL analysis schematic – Full adder

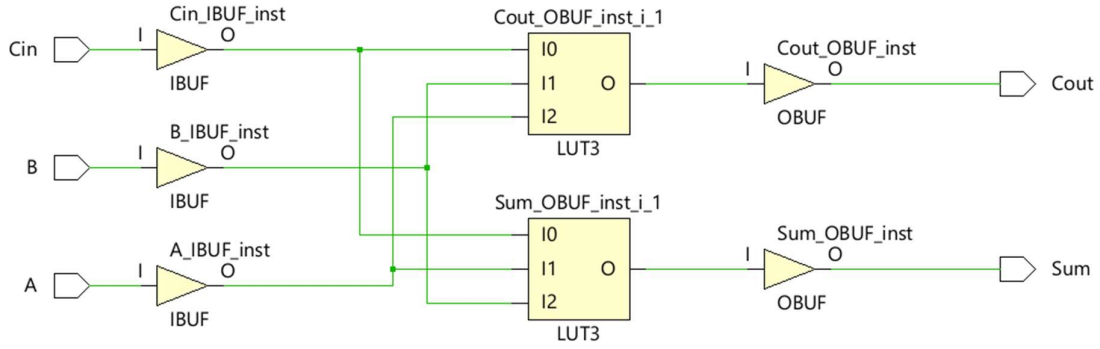

Figure 3: Synthesized schematic - Full adder

Look Up Tables:

Cell Properties

Cout_OBUF_inst_i_1

I2	I1	I0	O=I0 & I1 + I0 & I2 + I1 & I2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 5: LUT for Cout

Cell Properties

Sum_OBUF_inst_i_1

I2	I1	I0	O=I0 & !I1 & !I2 + !I0 & I1 & !I2 + !I0 & !I1 & I2 + I0 & I1 & I2
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Figure 4: LUT for Sum