

3-bit Multiplier

Block diagram

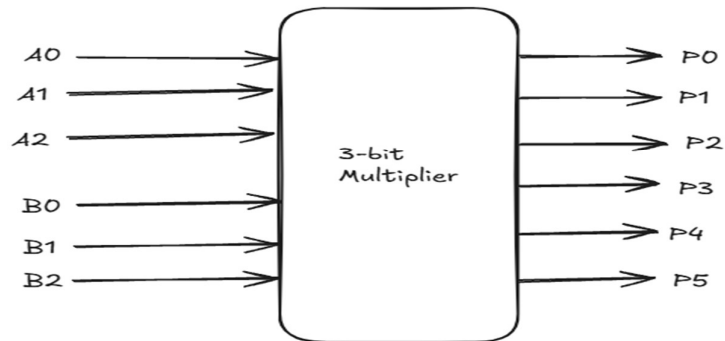


Figure 1: Block diagram

Working and Design:

			A2	A1	A0	
X			B2	B1	B0	
<hr/>						
			A2B0	A1B0	A0B0	
		A2B1	A1B1	A0B1		
+		A2B2	A1B2	A0B2		
<hr/>						
P5	P4	P3	P2	P1	P0	

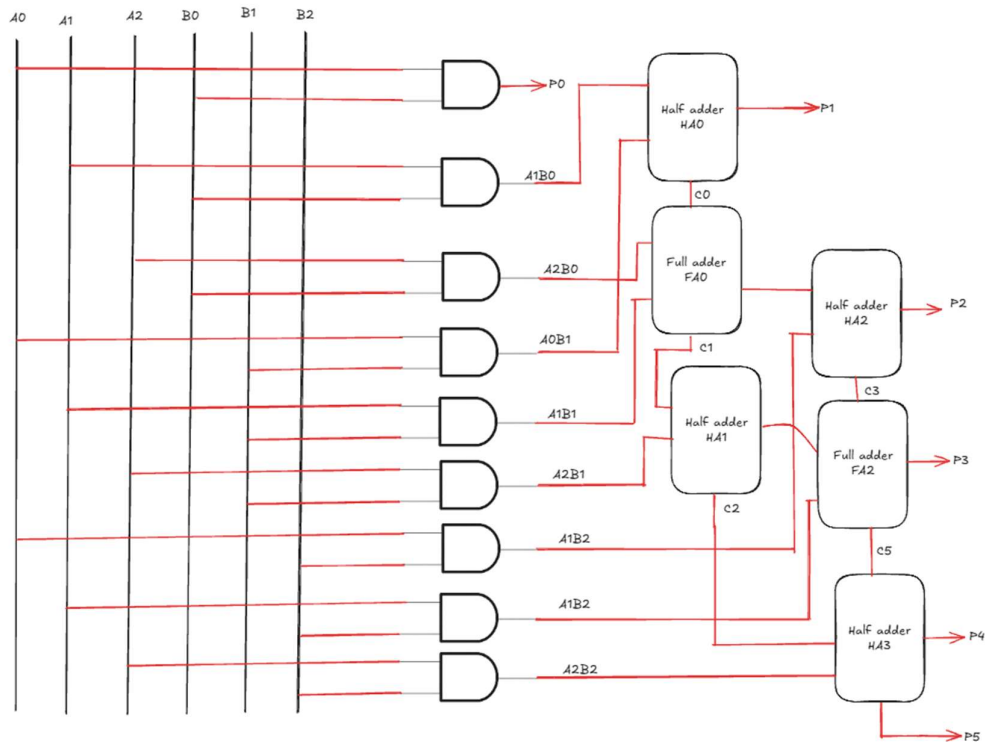


Figure 2: Design for 3bit Multiplier

Verilog code:

```
module multiplier_3bit (  
    input [2:0] A,  
    input [2:0] B,  
    output [5:0] P  
);
```

```
    wire A0B0 = A[0] & B[0];  
    wire A1B0 = A[1] & B[0];  
    wire A2B0 = A[2] & B[0];  
    wire A0B1 = A[0] & B[1];  
    wire A1B1 = A[1] & B[1];  
    wire A2B1 = A[2] & B[1];  
    wire A0B2 = A[0] & B[2];  
    wire A1B2 = A[1] & B[2];  
    wire A2B2 = A[2] & B[2];
```

```
    wire c0, c1, c2, c3, c5;  
    wire s1, s2, s3, s4;
```

```
    assign P[0] = A0B0;
```

```
    half_adder HA0 (A1B0, A0B1, P[1], c0);  
    full_adder FA0 (A2B0, A1B1, c0, s1, c1);  
    half_adder HA1 (s1, A0B2, s2, c2);  
    full_adder FA1 (A2B1, A1B2, c1, s3, c3);  
    half_adder HA2 (s2, s3, P[2], c5);  
    full_adder FA2 (A2B2, c2, c3, s4, P[5]);
```

```
half_adder HA3 (s4, c5, P[4], P[3]);
```

```
endmodule
```

```
module half_adder(input a, input b, output sum, output carry);
```

```
    assign sum = a ^ b;
```

```
    assign carry = a & b;
```

```
endmodule
```

```
module full_adder(input a, input b, input cin, output sum, output carry);
```

```
    assign sum = a ^ b ^ cin;
```

```
    assign carry = (a & b) | (b & cin) | (a & cin);
```

```
endmodule
```

Schematic:

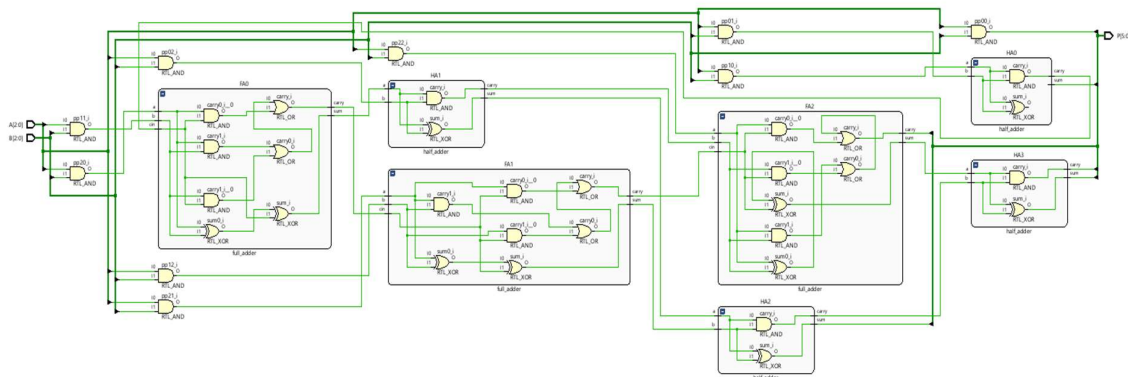


Figure 3: RTL Schematic

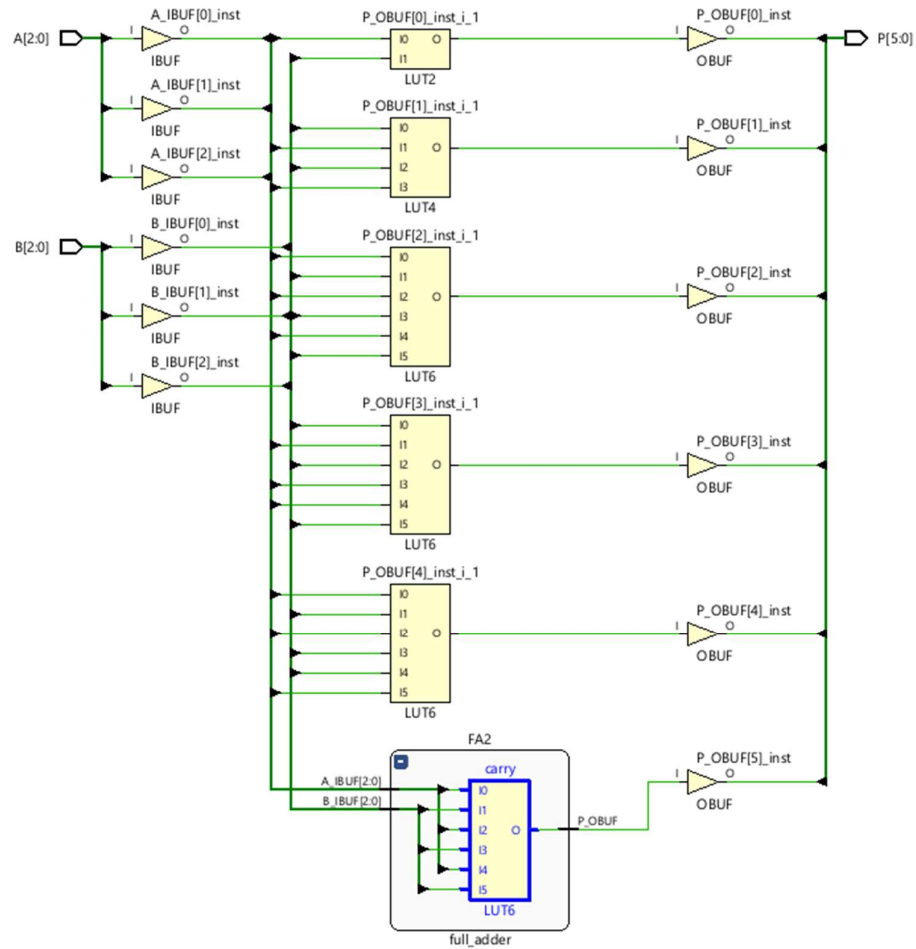


Figure 4: Synthesized Schematic

Look Up tables:

P_OBUF[0]_inst_i_1		
I1	I0	O=I0 & I1
0	0	0
0	1	0
1	0	0
1	1	1

Figure 5: LUT for P0

Cell Properties				
P_OBUF[1]_inst_i_1				
I3	I2	I1	I0	O=I0 & I1 & I3 + I0 & I1 & I2 + I1 & I2 & I3 + I0 & I2 & I3
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Figure 6: LUT for P1

LUT for P2

[illegible]

LUT for P3:

P_OBUF[3]_inst1_1

I5	I4	I3	I2	I1	I0	O=I0 & I1 & I12 & I13 & I4 & I5 + I0 & I1 & I2 & I13 & I14 & I5 + I0 & I1 & I12 & I3 & I4 & I15 + I0 & I1 & I2 & I3 & I14 & I15
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	0
0	0	1	0	0	0	0
0	0	1	0	0	1	0
0	0	1	0	1	0	0
0	0	1	0	1	1	0
0	0	1	1	0	0	0
0	0	1	1	0	1	0
0	0	1	1	1	0	0
0	0	1	1	1	1	1
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	0
0	1	0	0	1	1	0
0	1	0	1	0	0	0
0	1	0	1	0	1	0
I5	I4	I3	I2	I1	I0	O=I0 & I1 & I12 & I13 & I4 & I5 + I0 & I1 & I2 & I13 & I14 & I5 + I0 & I1 & I12 & I3 & I4 & I15 + I0 & I1 & I2 & I3 & I14 & I15
0	1	1	0	0	0	0
0	1	1	0	0	1	0
0	1	1	0	1	0	0
0	1	1	0	1	1	1
0	1	1	1	0	0	0
0	1	1	1	0	1	0
0	1	1	1	1	0	0
0	1	1	1	1	1	0
1	0	0	0	0	0	0
1	0	0	0	0	1	0
1	0	0	0	1	0	0
1	0	0	0	1	1	0
1	0	0	1	0	0	0
1	0	0	1	0	1	0
1	0	0	1	1	0	0
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	0	1	0	0	1	0
1	0	1	0	1	0	0
1	0	1	0	1	1	0
1	0	1	1	0	0	0
1	0	1	1	0	1	0

1	0	1	1	1	0	0
1	0	1	1	1	1	0
1	1	0	0	0	0	0
1	1	0	0	0	1	0
1	1	0	0	1	0	0
1	1	0	0	1	1	1
1	1	0	1	0	0	0
1	1	0	1	0	1	0
1	1	0	1	1	0	0
1	1	0	1	1	1	0
1	1	1	0	0	0	0
1	1	1	0	0	1	0
1	1	1	0	1	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	0
1	1	1	1	0	1	0
1	1	1	1	1	0	0
1	1	1	1	1	0	0
1	1	1	1	1	1	0

LUT for P4:

P_OBUF[4]_inst_1_1						
I5	I4	I3	I2	I1	I0	O=I1 & I2 & I4 & I5 + I1 & I2 & I3 & I4 & I5 + I10 & I2 & I3 & I4 & I5 + I10 & I1 & I3 & I4 & I5 + I0 & I2 & I4 & I5 + I10 & I1 & I2 & I4 & I5 + I0 & I1 & I2 & I4 & I4 + I1 & I2 & I4 & I4 & I5 + I1 & I2 & I3 & I4 & I5
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	0
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	0	1	0	1	0
0	0	0	1	1	0	0
0	0	0	1	1	1	0
0	0	1	0	0	0	0
0	0	1	0	0	1	0
0	0	1	0	1	0	0
0	0	1	0	1	1	0
0	0	1	1	0	0	0
0	0	1	1	0	1	0
0	0	1	1	1	0	0
0	0	1	1	1	1	0
0	1	0	0	0	0	0
0	1	0	0	0	1	0
0	1	0	0	1	0	0
0	1	0	0	1	1	0
0	1	1	0	0	0	0
0	1	1	0	0	1	0
0	1	1	0	1	0	0
0	1	1	0	1	1	0
0	1	1	1	0	0	1
0	1	1	1	0	1	1
0	1	1	1	1	0	1
0	1	1	1	1	1	1
1	0	0	0	0	0	0
1	0	0	0	0	1	0
1	0	0	0	1	0	0
1	0	0	0	1	1	0
1	0	0	1	0	0	0
1	0	0	1	0	1	0
1	0	0	1	1	0	1
1	0	0	1	1	1	1
1	0	1	0	0	0	0
1	0	1	0	0	1	0
1	0	1	0	1	1	1
1	0	1	1	0	0	1
1	0	1	1	1	0	1
1	0	1	1	1	1	1
1	1	0	0	0	0	1
1	1	0	0	1	0	1
1	1	0	0	1	1	0
1	1	0	1	0	0	1
1	1	0	1	0	1	0
1	1	0	1	1	0	0
1	1	0	1	1	0	0
1	1	0	1	1	1	1
1	1	1	0	0	0	1
1	1	1	0	0	1	0
1	1	1	0	1	0	0
1	1	1	0	1	1	0
1	1	1	1	0	0	0
1	1	1	1	0	1	0
1	1	1	1	1	0	0
1	1	1	1	1	1	1

LUT for P5:

15	14	13	12	11	10	O=I1 & I2 & I4 & I5 + I0 & I3 & I4 & I5	
0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0
0	0	0	0	1	1	0	0
0	0	0	1	0	0	0	0
0	0	0	1	0	1	0	0
0	0	0	1	1	0	0	0
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	0
0	0	1	0	0	1	0	0
0	0	1	0	1	0	0	0
0	0	1	0	1	1	0	0
0	0	1	1	0	0	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	0	0	0
0	0	1	1	1	1	0	0
0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0
0	1	0	0	1	0	0	0
0	1	0	0	1	1	0	0
0	1	0	1	0	0	0	0
0	1	0	1	0	1	0	0
0	1	0	1	1	0	0	0
0	1	0	1	1	1	0	0
0	1	1	0	0	0	0	0
0	1	1	0	0	1	0	0
0	1	1	0	1	0	0	0
0	1	1	0	1	1	0	0
0	1	1	1	0	0	0	0
0	1	1	1	0	1	0	0
0	1	1	1	1	0	0	0
0	1	1	1	1	1	0	0
1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	0	1	1	0	0
1	0	0	1	0	0	0	0
1	0	0	1	0	1	0	0
1	0	0	1	1	0	0	0
1	0	0	1	1	1	0	0
1	0	0	1	1	1	1	0
1	0	1	0	0	0	0	0
1	0	1	0	0	1	0	0
1	0	1	0	1	0	0	0
1	0	1	0	1	1	0	0
1	0	1	1	0	0	0	0
1	0	1	1	0	1	0	0
1	0	1	1	1	0	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	0	0	0
1	1	0	0	0	1	0	0
1	1	0	0	1	0	0	0
1	1	0	0	1	1	0	0
1	1	0	1	0	0	0	0
1	1	0	1	0	1	0	0
1	1	0	1	1	0	0	0
1	1	0	1	1	1	0	0
1	1	1	0	0	0	0	0
1	1	1	0	0	1	0	0
1	1	1	0	1	0	0	0
1	1	1	0	1	1	0	0
1	1	1	1	0	0	0	0
1	1	1	1	0	1	0	0
1	1	1	1	1	0	0	0
1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1