

## (8:3) Priority Encoder

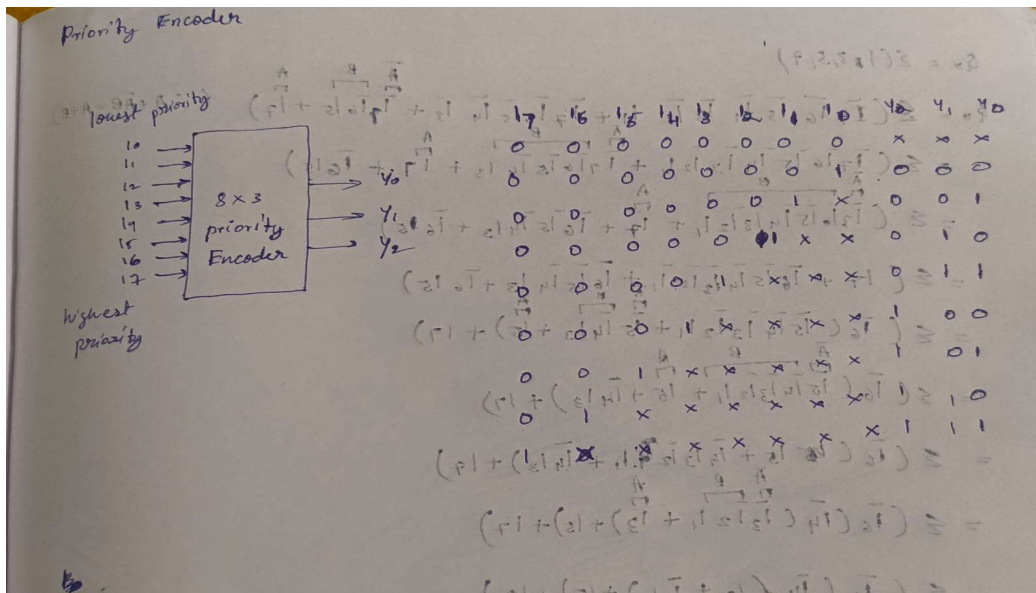


Figure 1: Block diagram and Truth table

### Verilog Code:

```

module priority_encoder( input [7:0] D, output reg [2:0] y);

always @(D) begin

    casex(D)

        8'b00000001 : y = 3'b000;

        8'b0000001x : y = 3'b001;

        8'b000001xx : y = 3'b010;

        8'b00001xxx : y = 3'b011;

        8'b0001xxxx : y = 3'b100;

        8'b001xxxxx : y = 3'b101;

        8'b01xxxxxx : y = 3'b110;

        8'b1xxxxxxx : y = 3'b111;

        default    : y = 3'bxxx;

    endcase

end
    
```

endmodule

### Alternate approach:

```
module priorityEncoder(input [7:0] I, output [2:0] Y );
```

```
assign Y[0]=(((~I[6])&((~I[4]&I[3])|(~I[4]&~I[2]&I[1]))|I[5])|I[7]);
```

```
assign Y[1]=(~I[5]&~I[4])&(I[2]|I[3])|I[6]|I[7];
```

```
assign Y[2]=(I[4]|I[5]|I[6]|I[7]);
```

endmodule

### RTL Synthesis Schematic:

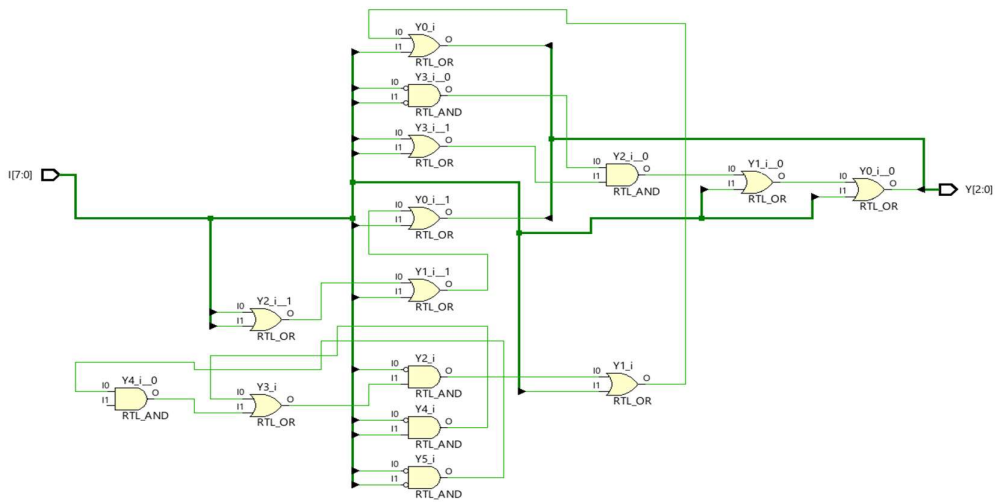


Figure 2: RTL Schematic

### Synthesized Schematic:

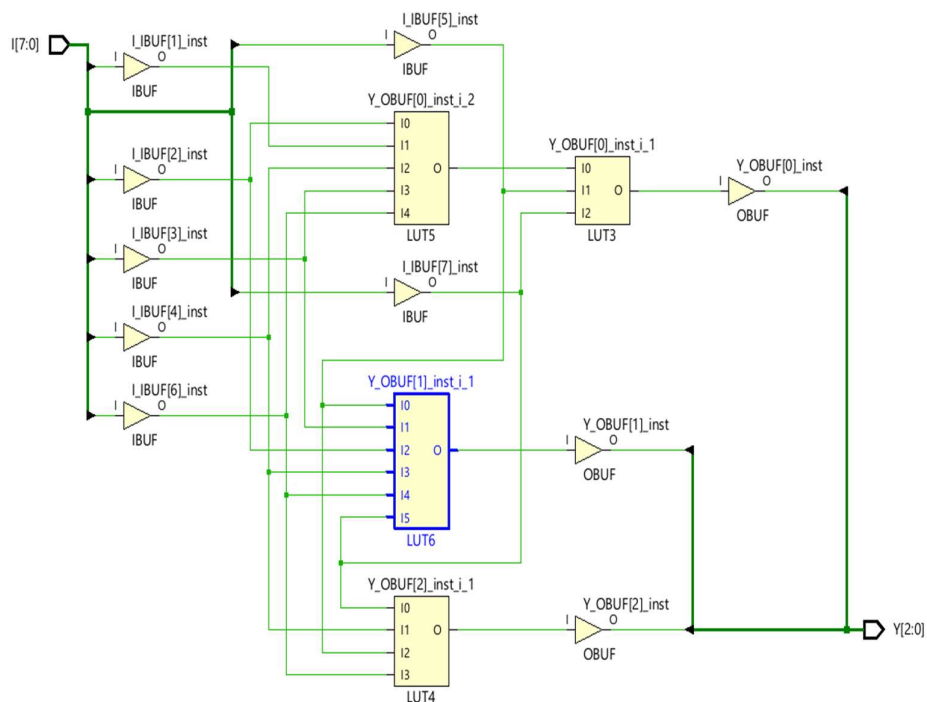


Figure 3: Synthesized Schematic

Look Up Tables:

Cell Properties				
Y_OBUF[0]_inst_i_1				
I2	I1	I0	O=I0 + I1 + I2	
0	0	0	0	
0	0	1	1	
0	1	0	1	
0	1	1	1	
1	0	0	1	
1	0	1	1	
1	1	0	1	
1	1	1	1	

Figure 4: LUT 3

Cell Properties					
Y_OBUF[2]_inst_i_1					
I3	I2	I1	I0	O=I0 + I1 + I2 + I3	
0	0	0	0	0	
0	0	0	1	1	
0	0	1	0	1	
0	0	1	1	1	
0	1	0	0	1	
0	1	0	1	1	
0	1	1	0	1	
0	1	1	1	1	
1	0	0	0	1	
1	0	0	1	1	
1	0	1	0	1	
1	0	1	1	1	
1	1	0	0	1	
1	1	0	1	1	
1	1	1	0	1	
1	1	1	1	1	

Figure 5: LUT 4

Cell Properties						
Y_OBUF[0]_inst_i_2						
I4	I3	I2	I1	I0	O=I10 & I1 & I12 & I14 + I12 & I3 & I14	
0	0	0	0	0	0	
0	0	0	0	1	0	
0	0	0	1	0	1	
0	0	0	1	1	0	
0	0	1	0	0	0	
0	0	1	0	1	0	
0	0	1	1	0	0	
0	0	1	1	1	0	
0	1	0	0	0	1	
0	1	0	0	1	1	
0	1	0	1	0	1	
0	1	0	1	1	1	
0	1	1	0	0	0	
0	1	1	0	1	0	
0	1	1	1	0	0	
0	1	1	1	1	0	
1	0	0	0	0	0	
1	0	0	0	1	0	
1	0	0	1	0	0	
1	0	0	1	1	0	
1	0	1	0	0	0	

Figure 4: LUT 5

Cell Properties						
Y_OBUF[1]_inst_i_1						
I5	I4	I3	I2	I1	I0	O=I4 + I14 & I5 + I10 & I1 & I13 & I15 + I10 & I2 & I13 & I15
0	0	0	0	0	0	0
0	0	0	0	0	1	0
0	0	0	0	1	0	1
0	0	0	0	1	1	0
0	0	0	1	0	0	1
0	0	0	1	0	1	0
0	0	0	1	1	0	1
0	0	0	1	1	1	0
0	0	1	0	0	0	0
0	0	1	0	0	1	0
0	0	1	0	1	0	0
0	0	1	1	0	0	0
0	0	1	1	0	1	0
0	0	1	1	1	0	0
0	0	1	1	1	1	0
0	1	0	0	0	0	1
0	1	0	0	0	1	1
0	1	0	0	1	0	1
0	1	0	0	1	1	1
0	1	0	1	0	0	1

Figure 5: LUT 6