Edge detector

Given timing diagram:

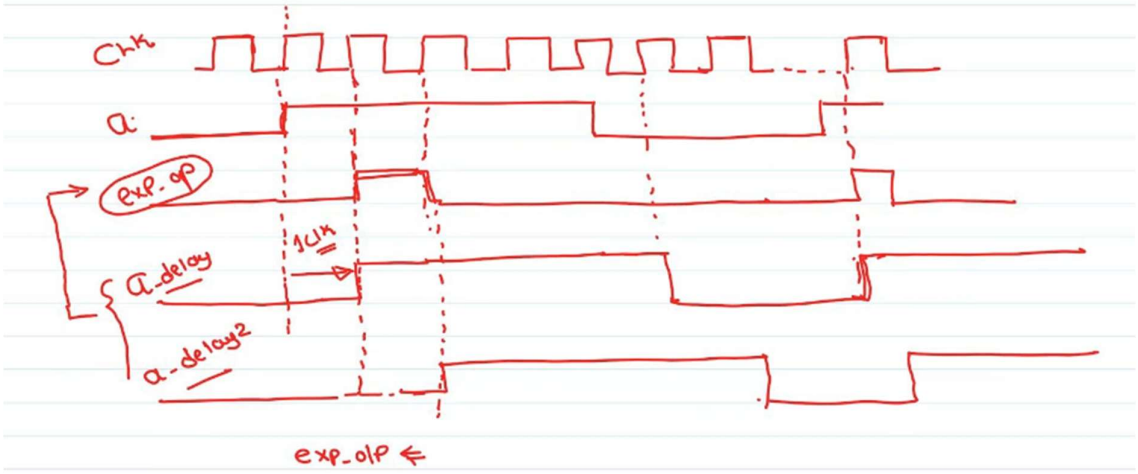

Figure 1: Question

Block diagram:

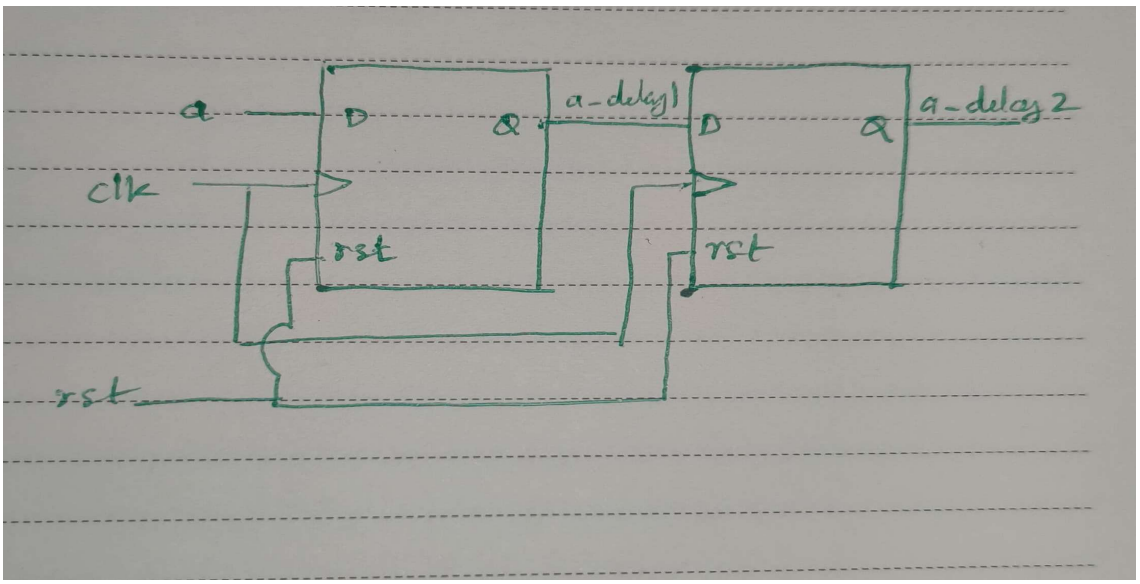

Figure 2: Block diagram

Verilog code:

```
module edgeDetection(
    input clk,
    input reset,
    input a,
```

```
    output exp_op,
    output a_delay1, a_delay2
    );

    dff d1(clk,reset,a,a_delay1);
    dff d2(clk,reset,a_delay1,a_delay2);
    assign exp_op= a_delay1 & ~a_delay2;

endmodule

module dff(input clk, input reset, input d, output reg q);
    always @(posedge clk) begin
        if (reset)
            q <= 1'b0;
        else
            q <= d;
    end
endmodule
```

Testbench code:

```
module edgeDetection_tb;
reg clk;
reg reset;
reg a;
wire exp_op;
wire a_delay1;
wire a_delay2;

edgeDetection uut(.clk(clk),.reset(reset),.a(a),.exp_op(exp_op),.a_delay1(a_delay1),.a_delay2(a_delay2));

initial begin
    clk = 0;
```

```
    forever #10 clk = ~clk;
end

initial begin
    reset = 1; a = 0;
    #10;
    reset = 0;
    #10; a = 0;
    #10; a = 1;
    #10; a = 1;
    #10; a = 1;
    #10; a = 1;
    #10; a = 0;
    #10; reset = 1;
    #10;
    $finish;
end

initial begin
    $monitor("time = %0t | clk = %b | reset = %b | a = %b | a_delay1 = %b | a_delay2 = %b | exp_op = %b",$time, clk, reset, a, a_delay1, a_delay2, exp_op);
end
endmodule
```

Schematics:

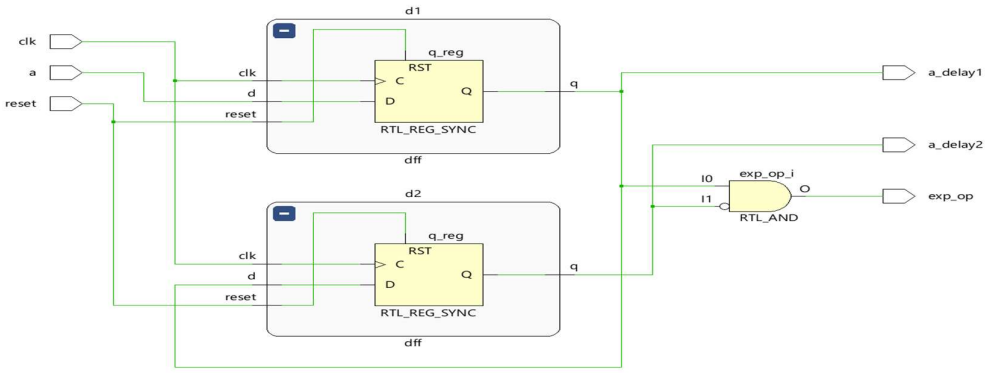

Figure 3: RTL Schematic

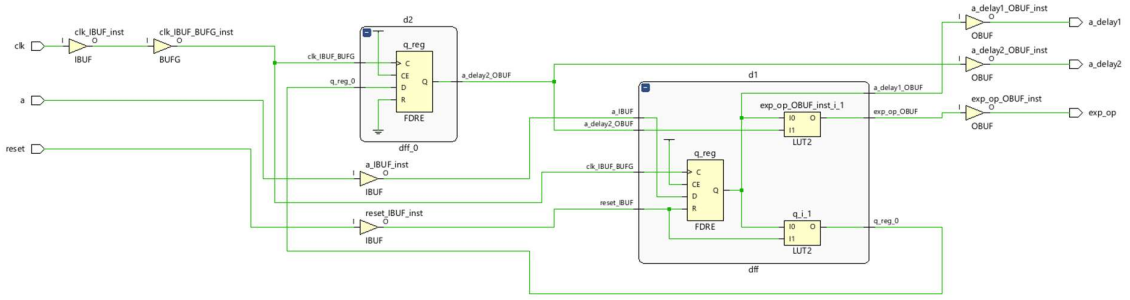

Figure 4: Synthesized Schematic

Slice Table:

```
1. Slice Logic
--------------

+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*             |    1 |     0 |          0 |     53200 | <0.01 |
|   LUT as Logic          |    1 |     0 |          0 |     53200 | <0.01 |
|   LUT as Memory         |    0 |     0 |          0 |     17400 |  0.00 |
| Slice Registers         |    2 |     0 |          0 |    106400 | <0.01 |
|   Register as Flip Flop |    2 |     0 |          0 |    106400 | <0.01 |
|   Register as Latch     |    0 |     0 |          0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |          0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     13300 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
```

Figure 5: Slice logic table

Number of slice LUT's used = 1

Timing diagram:

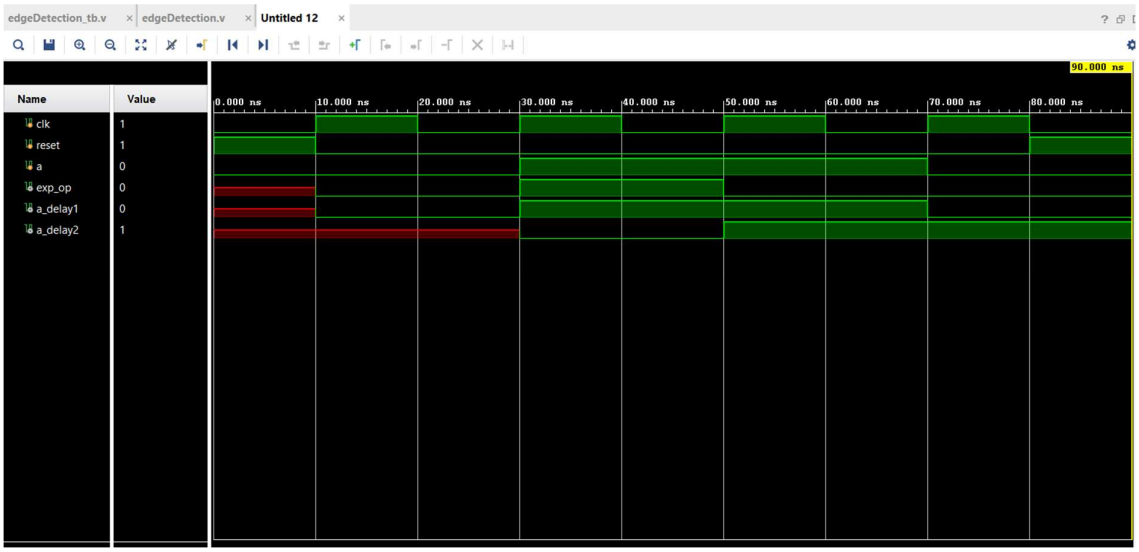

Figure 6: Timing diagram