D-FF with input of AND gate

Block diagram:

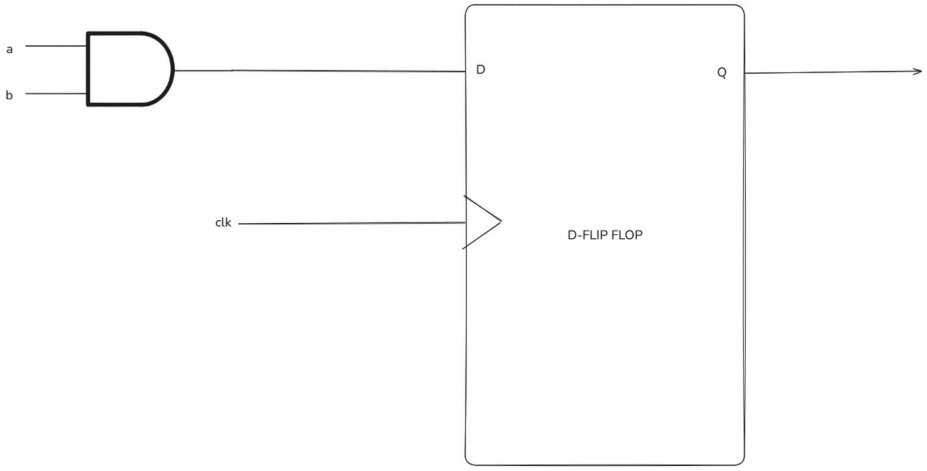

Figure 1: Block diagram

Verilog code:

```
module Dff_with_andGate(
   input clk,
   input reset,
   input a,
   input b,
   output reg q
   );

   always @(posedge clk) begin
   if (reset) begin
   q <= 1'b0;
   end
   else begin
   q <= a&b;
   end
   end
endmodule
```

Schematics:

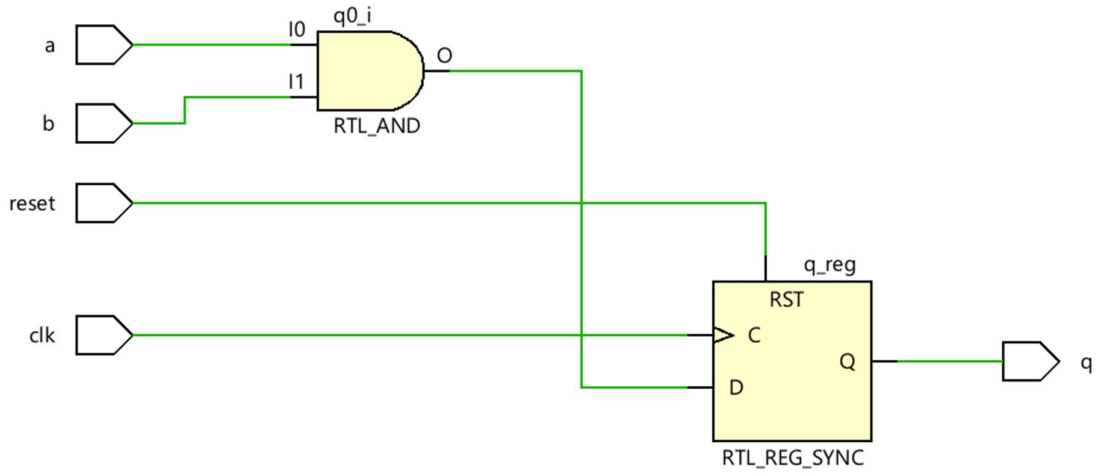

Figure 2: RTL Schematic

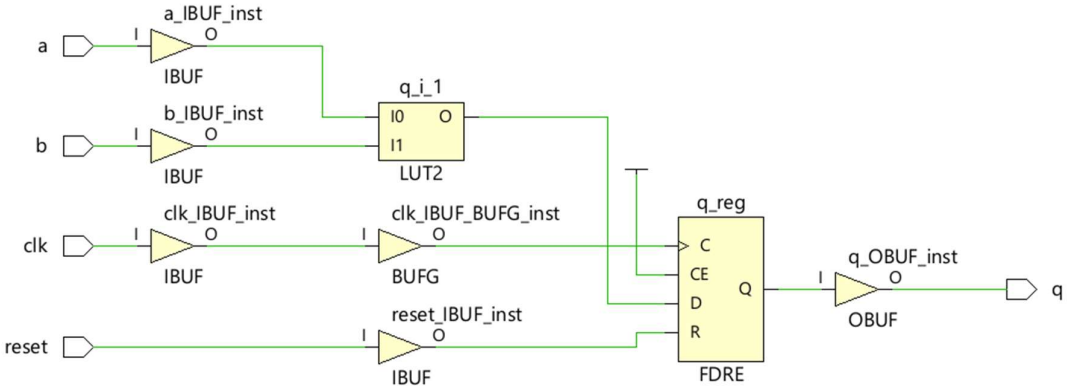

Figure 3: Synthesized Schematic

LUT:

Cell Properties

q_i_1

I1	I0	O=I0 ...
0	0	0
0	1	0
1	0	0
1	1	1

Figure 4: LUT2

Testbench code:

```
module Dff_with_andGate_tb;

reg clk;

reg reset;

reg a;

reg b;

wire q;


Dff_with_andGate a1(.clk(clk),.reset(reset),.a(a),.b(b),.q(q));


always #5 clk = ~clk;


initial begin

clk=0; reset=1; a=0; b=0;

#10;

reset=0;

#10; a=0; b=0;

#10; a=0; b=1;

#10; a=1; b=0;

#10; a=1; b=1;

#10; reset=1;

#10;

$finish;

end


initial begin

$monitor("Time=%0t | clk=%b | reset=%b | a=%b | b=%b | q=%b",$time, clk, reset, a, b, q);

end


endmodule
```

Timing diagram:

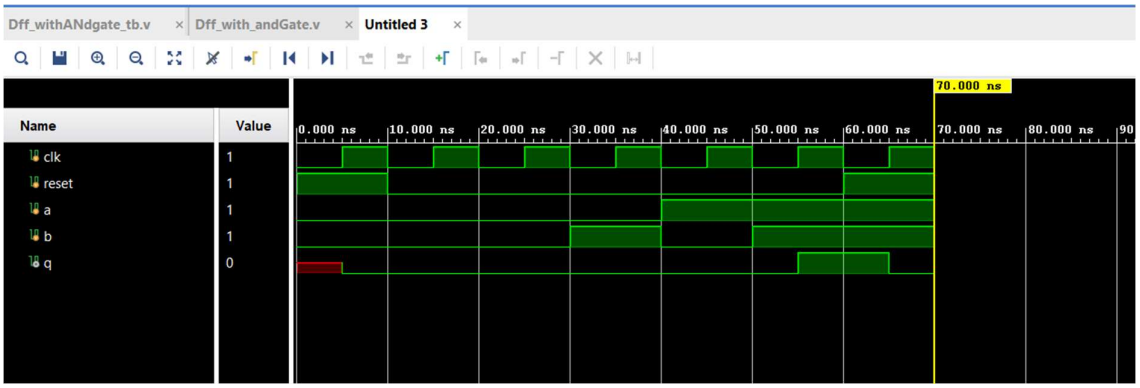

Figure 5: Timing diagram