2 bit Counter using JK FF and LUT

2-bit counter state diagram:

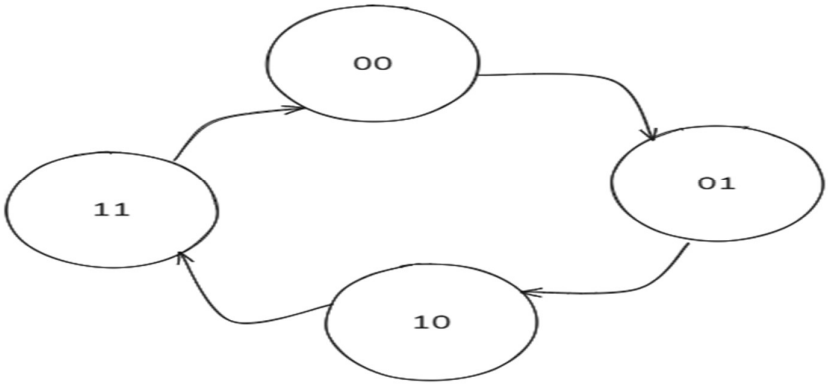

Figure 1: State diagram

D-FF truth table:

clk	D	Q	Q’
0	0	X	X
1	0	0	1
1	1	1	0

D-FF LUT table:

The D-FF directly passes the input D to output Q at next clock edge.

Q1	Q0	Q1+	Q0+	D1	D0
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	0

Block Diagram:

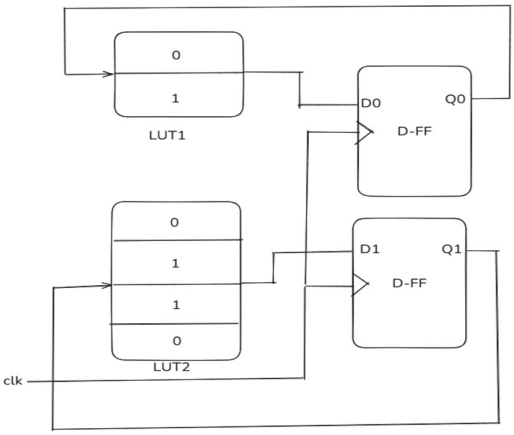

Figure 2: Block diagram for two bit counter

K-maps:

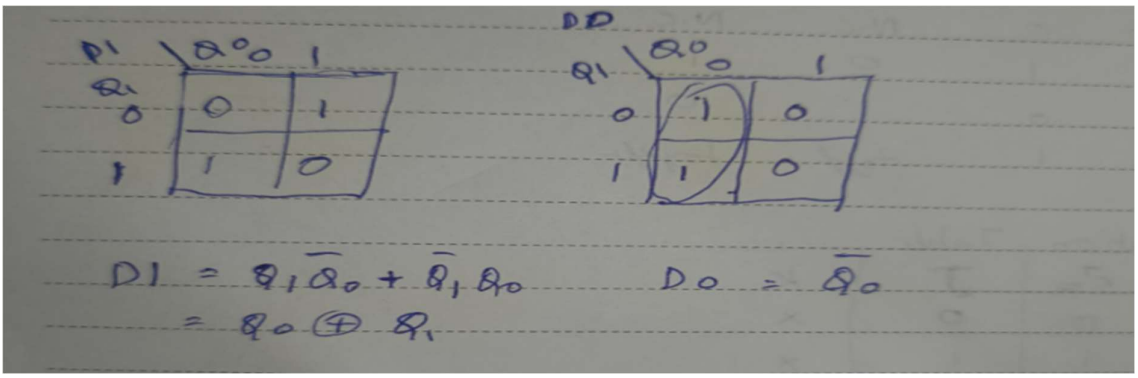

Figure 3: K-maps

Verilog Code:

```
module twoBit_counter (clk, reset, q);
   input wire clk;
   input wire reset;
   output reg [1:0] q;
   wire d0, d1;
   assign d0 = ~q[0];
   assign d1 = q[1] ^ q[0];

   always @(posedge clk) begin
      if (reset)
         q <= 2'b00;
      else
         q <= {d1, d0};
   end
endmodule
```

Schematics:

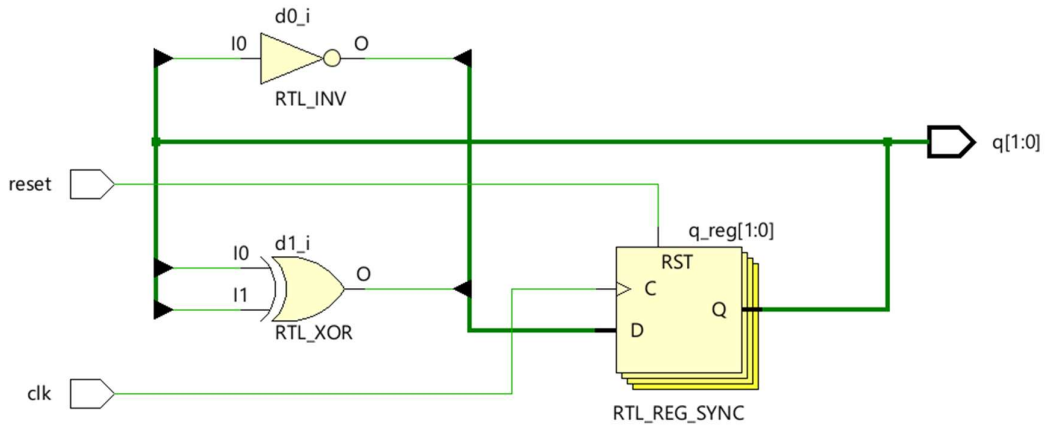

Figure 4: RTL Schematic

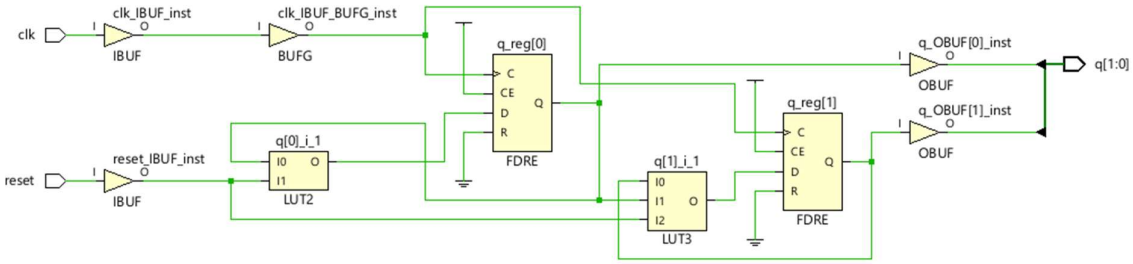

Figure 5: Synthesized Schematic

LUT's:

I1	I0	O=!I0 & !I1
0	0	1
0	1	0
1	0	0
1	1	0

Figure 7: LUT2

q[1]_i_1

I2	I1	I0	O=I0 & !I1 & !I2 + !I0 & I1 & !I2
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 6: LUT3