Block RAM

Verilog code:

```
module bram(
   input clk,
   input we,
   input [9:0] addr,
   input [31:0] din,
   output [31:0] dout
   );
   reg [31:0] mem [0:1023];

   always @(posedge clk) begin
   if(we) begin
   mem[addr]=din;
   end
   end
   assign dout = mem[addr];
endmodule
```

Schematics:

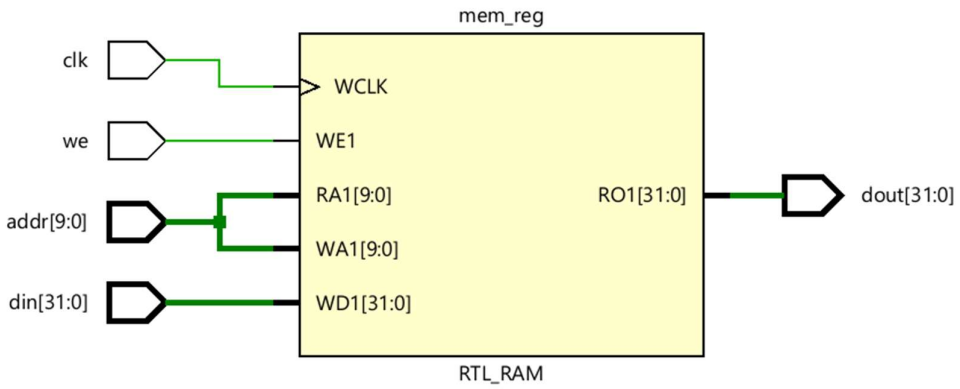

Figure 1: RTL Schematic

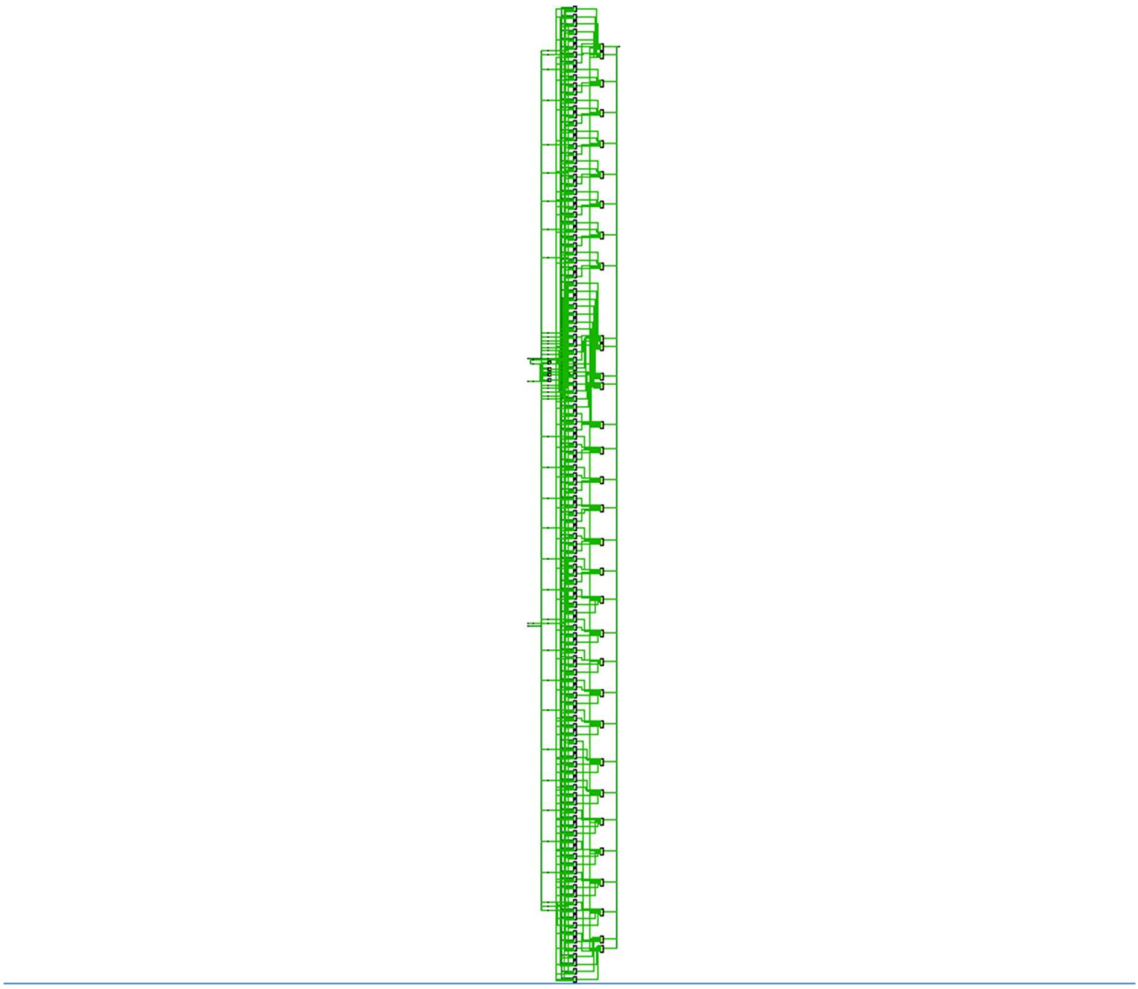

Figure 2: Synthesized Schematic

The design uses, **RAM256X1S** which is a 256bit deep by 1bit wide random access memory with synchronous write and asynchronous read capability. **This RAM is implemented using LUT resources of the devices which are known as SRAM, and does not consume any of the BRAM resources of the device**. **Also it uses LUT3 and LUT6**.

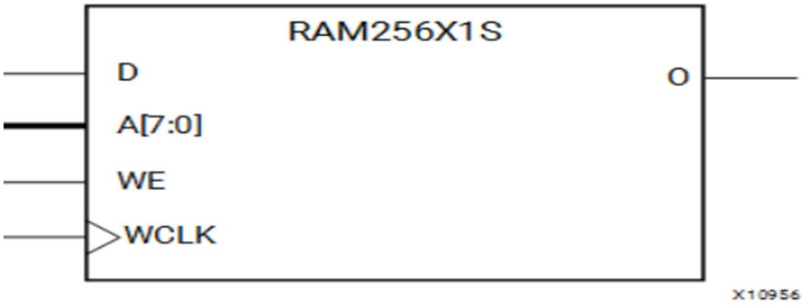

Figure 3: Block diagram of RAM256X1S