TRUE Dual Port BRAM

Block diagram:

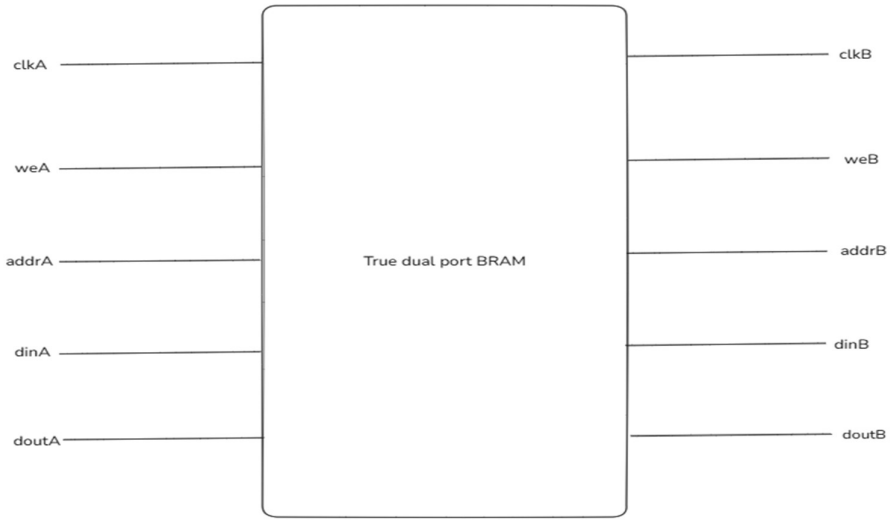

Figure 1: Block diagram

Verilog code:

```
module true_dualPort_BRAM(
input clkA,clkB,weA,weB,
input [13:0] addrA, addrB,
input [31:0] dinA, dinB,
output reg [31:0] doutA, doutB
   );
(* ram_type = "block" *)
reg [31:0] mem [0:16384];

always @(posedge clkA) begin
if (weA) begin
mem[addrA]<= dinA;
end
doutA<=mem[addrA];
```

```
end


always @(posedge clkB) begin
if (weB) begin
mem[addrB]<= dinA;
end
doutB<=mem[addrB];
end

endmodule
```

Schematics:

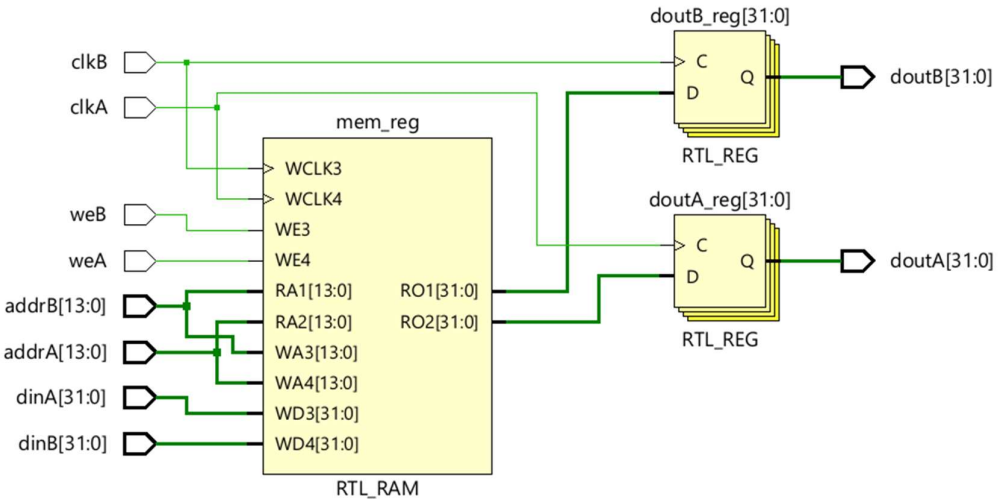

Figure 2: RTL Schematic

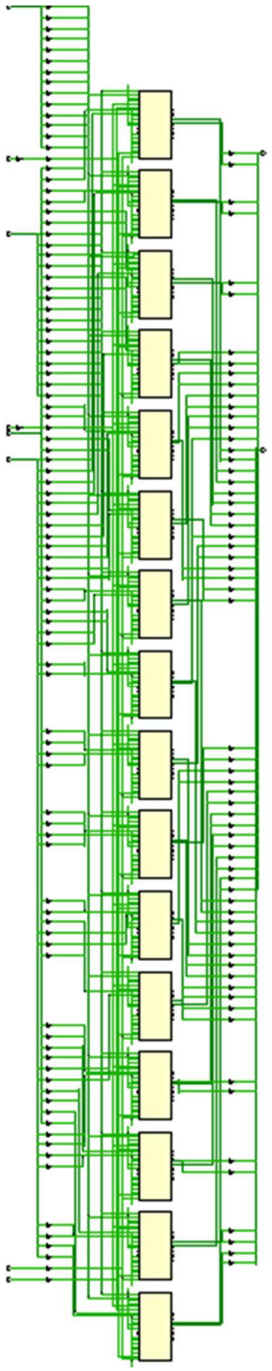

Figure 3: Synthesized schematic

Obseravation: Based on the give requrirement that is 32 bit width and 16K bit depth, 32*16Kb = 524288 bits (512 Kb). Therefore number of 36K block ram is 524288/36864 = 15 blocks.

Logic tables:

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	0	0	0	53200	0.00
LUT as Logic	0	0	0	53200	0.00
LUT as Memory	0	0	0	17400	0.00
Slice Registers	0	0	0	106400	0.00
Register as Flip Flop	0	0	0	106400	0.00
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Figure 4: Slice logic table

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	16	0	0	140	11.43
RAMB36/FIFO*	16	0	0	140	11.43
RAMB36E1 only	16				
RAMB18	0	0	0	280	0.00

Figure 5: Memory table