

# Estimation of LUT's using given function

**Given function:**  $a \& b \mid c \wedge d \& e \mid f \wedge g \& h$

**Verilog code:**

```
module EstimationOf_LUT_for_a_given_function(  
    input a,b,c,d,e,f,g,h,  
    output y  
);  
    assign y = a&b|c^d&e|f^g&h;  
endmodule
```

Schematics:

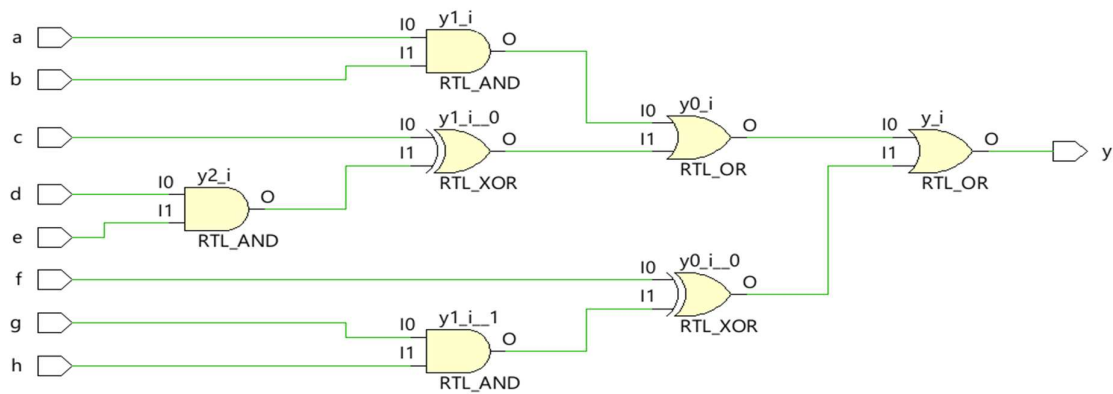


Figure 1: RTL Schematic

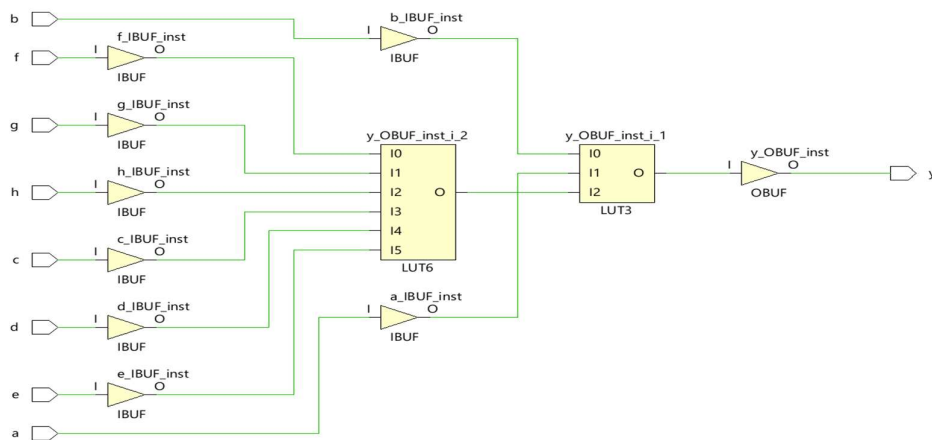


Figure 2: Synthesized schematic

Verilog code:

```
module EstimationOf_LUT_for_a_given_function(
    input a,b,c,d,e,f,g,h,
    output y
);
    assign y = a&b|c^d&e|f^g&h;
endmodule
```

Two LUT's are being used – LUT3 and LUT6

LUT's:

	A	B	C	D	E	F	G	
1	15	14	13	12	11	10	$O = !I0 \& !I1 \& !I2 + !I3 \& !I4 \& !I5 + !I0 \& !I2 + !I3 \& !I5 + !I0 \& !I1 \& !I2 + !I3 \& !I4 \& !I5$	
2	0	0	0	0	0	0		0
3	0	0	0	0	0	1		1
4	0	0	0	0	1	0		0
5	0	0	0	0	1	1		1
6	0	0	0	1	0	0		0
7	0	0	0	1	0	1		1
8	0	0	0	1	1	0		1
9	0	0	0	1	1	1		0
10	0	0	1	0	0	0		1
11	0	0	1	0	0	1		1
12	0	0	1	0	1	0		1
13	0	0	1	0	1	1		1
14	0	0	1	1	0	0		1
15	0	0	1	1	0	1		1
16	0	0	1	1	1	0		1
17	0	0	1	1	1	1		1
18	0	1	0	0	0	0		0
19	0	1	0	0	0	1		1
20	0	1	0	0	1	0		0
21	0	1	0	0	1	1		1
22	0	1	0	1	0	0		0
23	0	1	0	1	0	1		1
24	0	1	0	1	1	0		1
25	0	1	0	1	1	1		0
26	0	1	1	0	0	0		1
27	0	1	1	0	0	1		1
28	0	1	1	0	1	0		1
29	0	1	1	0	1	1		1
30	0	1	1	1	0	0		1
31	0	1	1	1	0	1		1
32	0	1	1	1	1	0		1
33	0	1	1	1	1	1		1
34	1	0	0	0	0	0		0
35	1	0	0	0	0	1		1
36	1	0	0	0	1	0		0
37	1	0	0	0	1	1		1
38	1	0	0	1	0	0		0
39	1	0	0	1	0	1		1
40	1	0	0	1	1	0		1
41	1	0	0	1	1	1		0
42	1	0	1	0	0	0		1
43	1	0	1	0	0	1		1
44	1	0	1	0	1	0		1
45	1	0	1	0	1	1		1
46	1	0	1	1	0	0		1
47	1	0	1	1	0	1		1
48	1	0	1	1	1	0		1
49	1	0	1	1	1	1		1
50	1	1	0	0	0	0		1
51	1	1	0	0	0	1		1
52	1	1	0	0	1	0		1
53	1	1	0	0	1	1		1
54	1	1	0	1	0	0		1
55	1	1	0	1	0	1		1
56	1	1	0	1	1	0		1
57	1	1	0	1	1	1		1
58	1	1	1	0	0	0		0
59	1	1	1	0	0	1		1
60	1	1	1	0	1	0		0
61	1	1	1	0	1	1		1
62	1	1	1	1	0	0		0
63	1	1	1	1	0	1		1
64	1	1	1	1	1	0		1
65	1	1	1	1	1	1		0
66								

Figure 3: LUT6

I2	I1	I0	O=I0 & I1 + I2
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Figure 4: LUT3

```
Project Summary x Device x Schematic x Utilization - Synth Design - synth_1 x
D:\Majorproject\my\anmayalinternship\anmayalinternship.runs\synth_1\EstimationOf_LUT_for_a_given_function_utilization_synth.rpt

Q [Icons] Read-only

19 2. Memory
20 3. DSP
21 4. IO and GT Specific
22 5. Clocking
23 6. Specific Feature
24 7. Primitives
25 8. Black Boxes
26 9. Instantiated Netlists
27
28 1. Slice Logic
29 -----
30
31 +-----+
32 | Site Type | Used | Fixed | Prohibited | Available | Util% |
33 +-----+
34 | Slice LUTs* | 2 | 0 | 0 | 53200 | <0.01 |
35 | LUT as Logic | 2 | 0 | 0 | 53200 | <0.01 |
36 | LUT as Memory | 0 | 0 | 0 | 17400 | 0.00 |
37 | Slice Registers | 0 | 0 | 0 | 106400 | 0.00 |
38 | Register as Flip Flop | 0 | 0 | 0 | 106400 | 0.00 |
39 | Register as Latch | 0 | 0 | 0 | 106400 | 0.00 |
40 | F7 Muxes | 0 | 0 | 0 | 26600 | 0.00 |
41 | F8 Muxes | 0 | 0 | 0 | 13300 | 0.00 |
42 +-----+
43 * Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, fo
44 Warning! LUT value is adjusted to account for LUT combining.
45 Warning! For any ECO changes, please run place_design if there are unplaced instances
46
```

Figure 5: Slice usage

Total number of slice LUT's = 2