NC State University

Department of Electrical and Computer Engineering

ECE 463/521: Fall 2015 (Rotenberg)

Project #1: Cache Design, Memory Hierarchy Design

by

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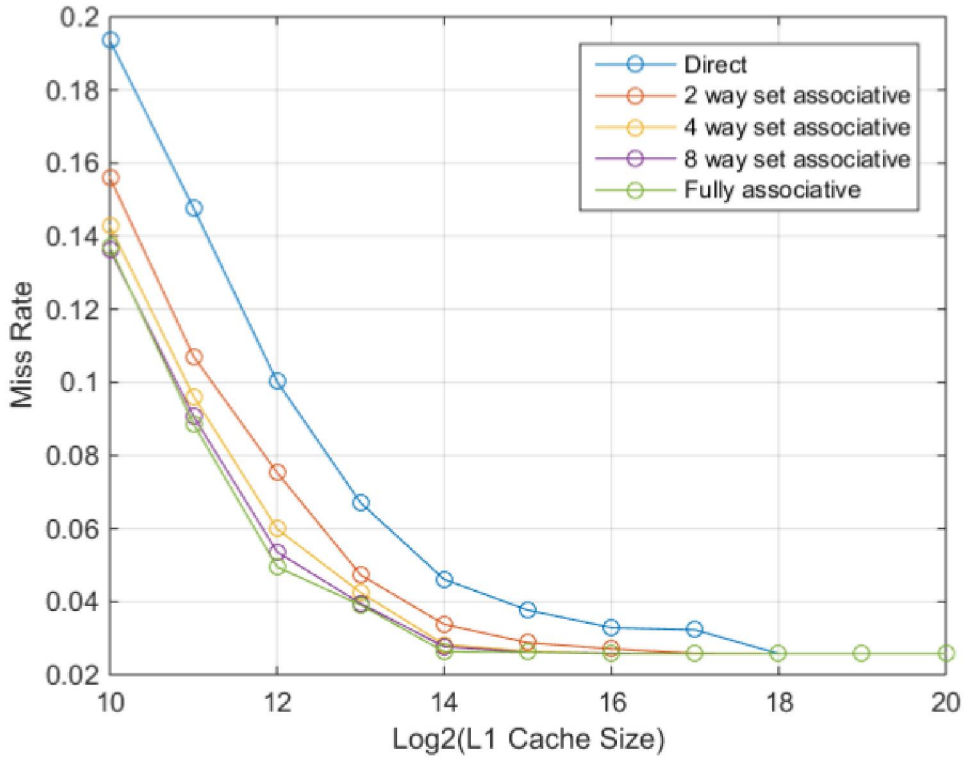
(sign by typing your name)

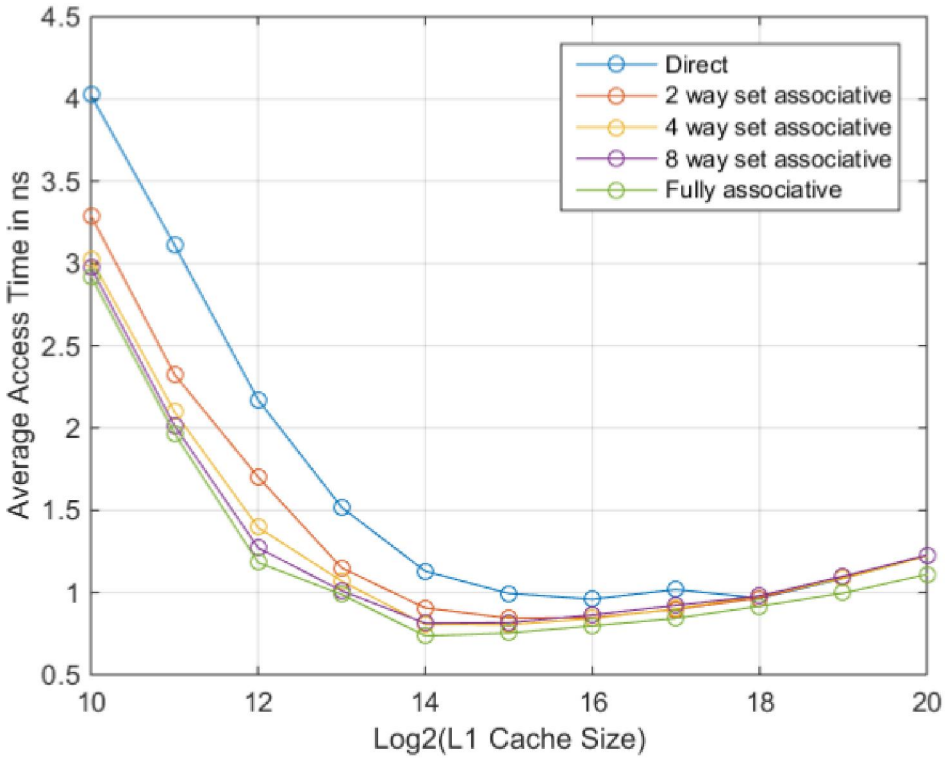
Course number: 521

GRAPH 1:



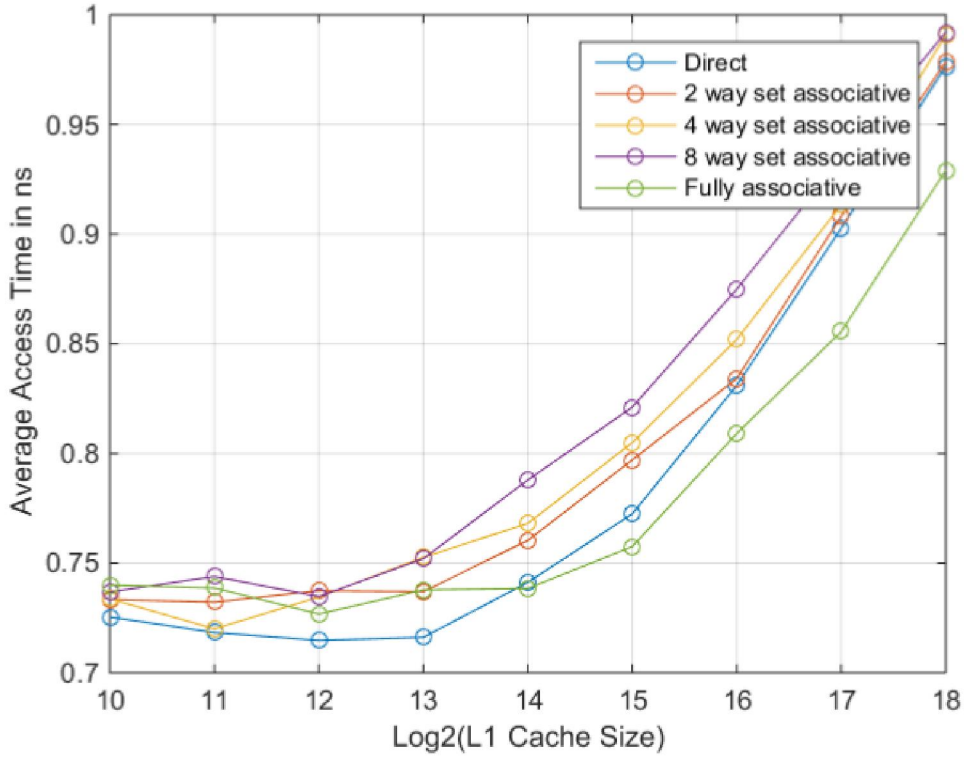
1. Increasing cache size decreases the miss rate until a certain point at which the rate of decrease plateaus. This is when the conflict miss rate is dominant.
2. For the fully associative cache, when it reaches a suitable size the miss rate stabilizes at 0.0258. This is the compulsory miss rate since by definition; fully associative caches do not have conflict misses and at high sizes the capacity misses are negligible.
3. We can estimate the conflict miss rate by subtracting the compulsory miss rate previously determined from the miss rate at high cache sizes for each associativity.

GRAPH 2:



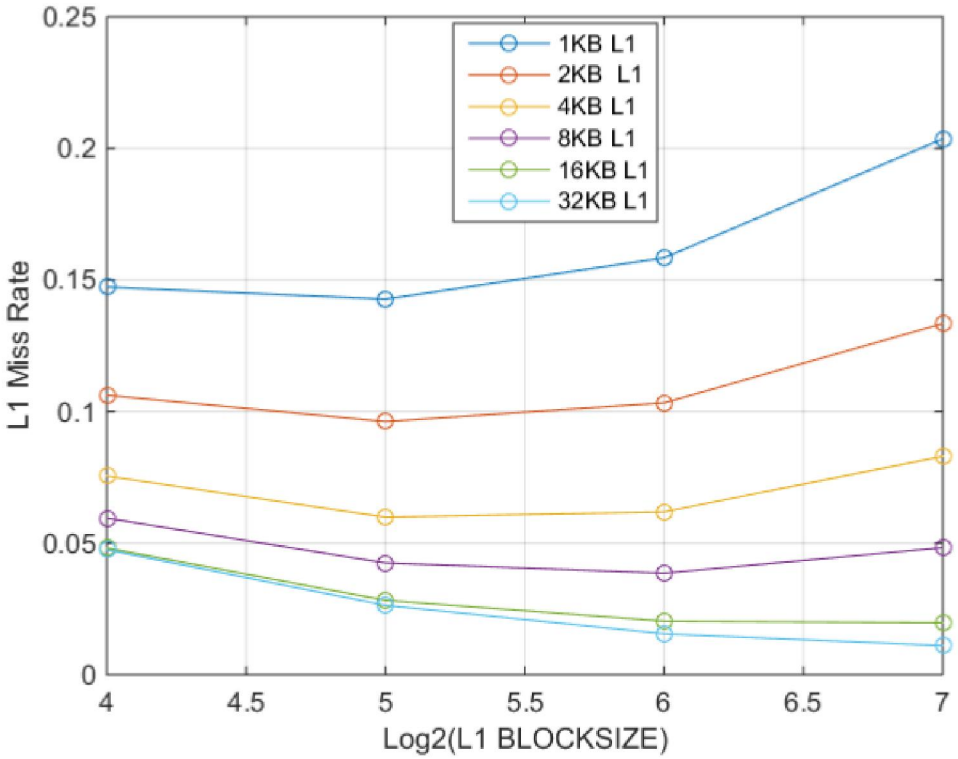
1. The fully associative cache with size 16KB, block size 32 has the lowest AAT. This is 0.7369 ns.

GRAPH 3:



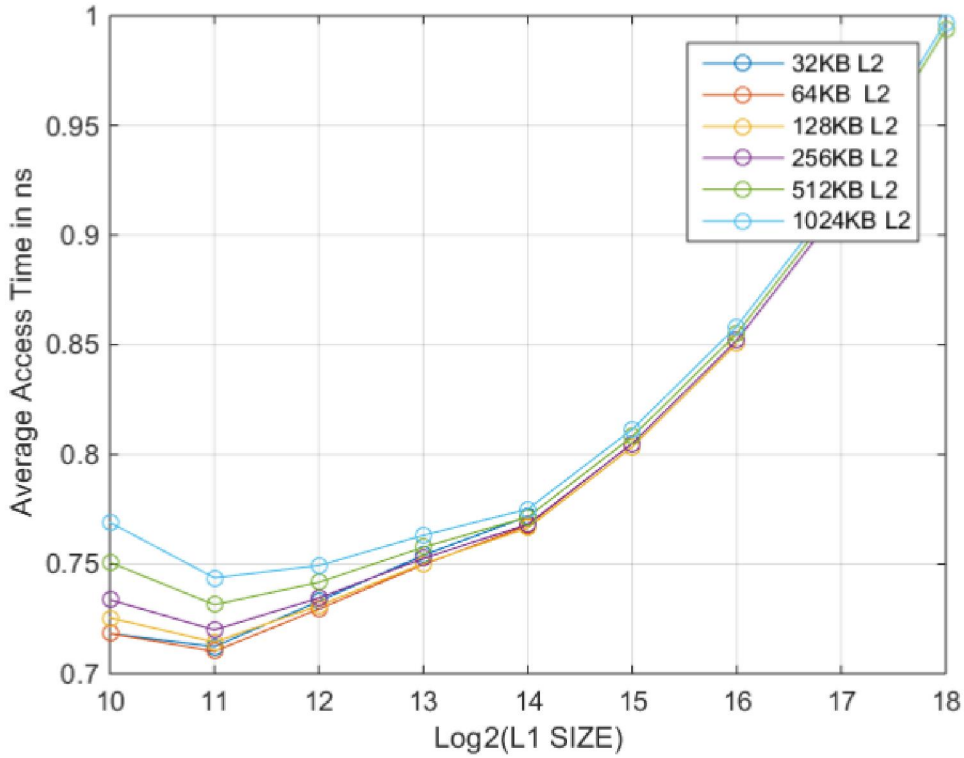
1. The 2 way set associative cache with a size of 8KB has a AAT of 0.7370ns which is very close to the best AAT obtained without L2 cache earlier.
2. The lowest AAT is that of the direct mapped cache with size 4KB, it has an AAT of 0.7148ns.

GRAPH 4:



1. As can be seen smaller caches work better with smaller block sizes and larger caches work better with medium block sizes. This is because smaller caches are more susceptible to cache pollution.
   Examining the yellow line, it is evident that for larger caches as you keep increasing the blocksize, the advantage gained from exploiting spatial locality is offsetted by cache pollution, resulting in a noticeable turn in the graph.

GRAPH 5:



1. The 32KB L2 with a 1KB L1 yields the lowest AAT of 0.7102ns.