CPU - Central Processing Unit

Clack the particular wise in CPU that trung on East

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at a steady sate to keep everything in Sync. In

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modern CPU's its measured in City is turn an East

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several billion times / second.

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quickly

Scott CPU - docent exist but shows how its eachitecture is

- CPU firs in motherboard which inhun connects all

the components

- Right side is RAM (Random Acces Memory)

* list of address and each is a piece of data.

Data can be accessed coederly as well as sandomly.

CPM sends address to RAM

RAM address is a series of 180's sepresents on Raff

If doesn't do anything months the CPM also them on enable / set

when enable is an RAM cends data at address to CPM. via data but.

this prover happen over Eonel.
- sends & sets the set wife then Ram
overweiter that data

Nata in RAM - Instanctions - tells CPU to do things. - to process. - Numbers output as number send to monitor to - Address Letter stored at character codel. Instanction Set at CPV load a number from RAM to CPU 2 nos typother ADD from CPU to RAM STORE compake - one & another Jumps F - condition check to another RAM address Jump - more to another address put device such of montal OUT input from device. ez: anessing Grane RAM LOAD Keyboald COMPARC JUMP IF= 1001110 BUT Aphy (yest o MONITOR avers again.

How proceering an instanction Control Unit - recieve orders from RAM under it one imp most is ALU - Azithmetic Legic Unit - perform aethmetic operation Inpuls ARB I L flogs. T C.VI ALU C.V

Typed C.V

Outputs approximan 1 Instanctions from RAM Can be ignoted depending on citration. ALU > 8 vile origint goes to Rejisted. Register - only job is to doce a number temporality acts like RAM. = it doesn't save anythin untill CPU them on the set wise. [Au] [cu] They cet | enable - Cu then the enable then only Reg. output what it just saved.

ingso course divised from but

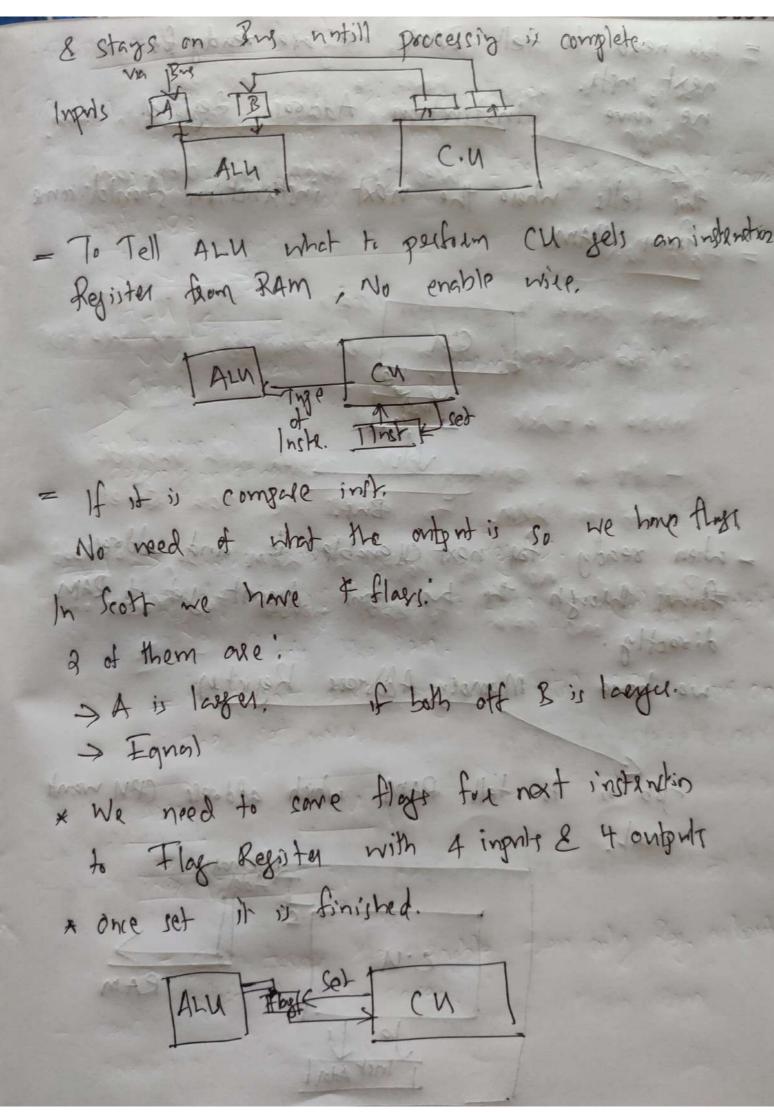
= Ontput of ALU Reg. connected to CPU Bul.) connects other components. It have some other Rejuters with some enable & let cu them set of a particular Reg to save the enter from a key to it.

8 tuens of enable of freet Rey so be to clear
the But. the But. TA-M TCU

Reg Reneble advantage of Box: disadvanlage:

= easily moving components = only one number of a time.

Too this we have a temporary Regular. for input B when cu proveds something in ALU
- it will move one of inputs to temp Reg 2 Tens Register doesn't regnile enable since it origins only to ALU. & dient conflict with any other, reg. other ingut comes directly from Bus



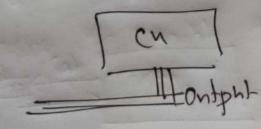
We need to tell RAM me are ready for next insta. ne have Instanction Address Register this tells where the next instanction should come from RAM. Bns. - when ready for next chemoble it. and address flows though the bir but dienst get to RAM directly. we have Memory Address Register to tell RAM which address CPU words Nox -Memory

* when Memory Address is Set it antimatically sends to RAM as there is no enable for MAR enable RAM - CV then enable the enable RAM wire RAM then sends the data at that address which then goes book to Instenction Register. = soved it there. - Its Jump IP equal inst. - As working by sunning one of its wise & Flag eynd wire through an AND Gote if both one on hisel ontary is also on Jump is Jano > Teigger Jump

Next das from RAM

equal 1 = Now outpuls to Monital.

* Scott process this in 6 clock ticks. For each instant



poets on left is used to plug in input /ontgot device) & each have a post address with them, through which the CPU amministed with them, Post address is used to send by data bus.

= Hard Deive

when power is off all data in RAM is list eo for storing data permenantela, me me HDD

Inside a ADSK - Its a spiriting Disk covered with magneti.

and om Alm. to access the data stores.

= Buts its not of Egt on RAM so, we need to load data to RAM inveded to process it