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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

First Semester MCA (2 Year) Degree Examination December 2021

Course Code: 20MCA103
Course Name: DIGITAL FUNDAMENTALS & COMPUTER ARCHITECTURE

Max. Marks: 60 Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks. Marks

1	Convert the decimal number 3.248×10^4 to a single precision floating point binary number.	(3)
2	Implement a full adder using 8:1 MUX.	(3)
3	Explain Serial in Serial out shift register with the help of circuit diagram.	(3)
4	How can you convert JK Flip flop to D Flip flop?	(3)
5	A program runs in 10 second on computer A, which has a 2 GHz clock. You are trying to help a computer designer build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but this increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should you tell the designer to target?	(3)
6	Describe the code sequence of C=A+B in Single Accumulator organization and Stack organization of instruction set architecture.	(3)
7	Explain any one of the bus arbitration schemes in DMA.	(3)
8	How to calculate branch target address in branch on equal(beq) instruction?	(3)
9	Write a short note on memory operations: a)Write back b) Write through	(3)
10	Explain different types of Read Only Memory (ROM).	(3)

PART B

Answer any one question from each module. Each question carries 6 marks.

Module I

11 Minimize the Boolean expression f(A,B,C,D)=∑(0,1,3,5,7,8,9,11,13,15)using Karnaugh map and realize it using NAND gate. (6)

OR

12 a Using Boolean algebra techniques,simplify the (3)

b expressionAB+A(B+C)+B(B+C) (3)

Express +19 and -19 in 2's complement form.

Module II

13 Explain the working of an edge triggered SR Flip flop in detail. (6)

OR

14 Design a 3 bit UP/DOWN synchronous counter. (6)

Module III

15 What you meant by addressing modes? Explain any three addressing modes that have been used in recent computers. (6)

OR

16 Explain the five classic components of a computer with figure. (6)

Module IV

17 Draw a single data path representation for R-type instruction. (6)

OR

18 How should two or more simultaneous interrupt requests be handled? Explain with figure. (6)

Module V

19 How the virtual address is converted into real address in a paged virtual memory system? Explain. (6)

OR

20 A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address. (6)

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