

**MADHAV INSTITUTE OF TECHNOLOGY & SCIENCE, GWALIOR**

(A Govt. aided UGC Autonomous &amp; NAAC Accredited Institute Affiliated to RGPV, Bhopal, M.P.)

**END SEM EXAMINATION – DEC, 2020**

(For Online Open Book &amp; Assignment plus Oral Based Examination only)

Class: B.E./B.Tech./M.E./M.Tech./M.C.A./B.Arch./MUP

Semester: .....V.....Subject Code: ....150504.... Subject Title: ....microprocessor P. Interfacing [P]....

Enrolment No.:

<u>0</u>	<u>9</u>	<u>0</u>	<u>1</u>	<u>C</u>	<u>S</u>	<u>1</u>	<u>8</u>	<u>1</u>	<u>0</u>	<u>0</u>	<u>7</u>
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Date of Examination: ....23/12/2020....Signature of the Candidate (*Must of same as available in the Institute*):

Code (*Candidate need to fill*):

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M	M	Y	Y	1	2	3	4

MM - Month of the birth of Candidate

YY - Year of the birth of Candidate

1,2,3,4 - Last four digits of Adhar Card/PAN Card/Voter Card

**IMPORTANT INSTRUCTIONS:**

1. Candidate must start writing from this page
2. Not any part of page / page should be left blank. This is necessary to reduce the size of the pdf file.
3. There should not be any cutting / overwriting in the enrolment number.
4. Answer must be to the point.
5. Students should take the printout of this page much before the start of the exam and complete the entries.

**Start Writing from here**

Q1  
(Ans) An Interrupt is a condition that halts the microprocessor temporary to work on a different task & return to its previous task. Interrupt is an event or signal that request attention of CPU.

When ever an interrupt occurs the processor completes the execution of the current instruction and starts the execution of an interrupt service routine (ISR) or interrupt handler. ISR is a programme that tells the processor what to do when interrupt occurs.

(Ans 1)(b)

Q1) (Ans b) In 8086, a 6-Byte Instruction queue is presented at the Bus Interface unit (BIU). It is used to prefetch and store at the max of 6 Bytes of instruction code from the memory. Due to this, overlapping instruction fetch with instruction fetch with instruction. Execution increases the production speed.

Once the Execution queue contains 6 Bytes of instruction the Execution unit (EU) fetches the instruction from the queue in FIFO order.

(Ans 1)c

Q1) (Ans c) In 8086 we have Base registers and Index registers. So ~~BIU~~ calculates EA by summing a displacement, the content of Base register and the content of Index register. The displacement is an 8 or 16 bit number that is contained in the instruction.

It is calculated calculated by using the formula

$$\text{Effective / Physical Address} = \text{segment address} \times 10H + \underbrace{\text{Effective Address}}_{\begin{array}{c} \uparrow \\ \text{S} \\ \uparrow \end{array}} + \underbrace{\text{offset Address}}_{\begin{array}{c} \uparrow \\ \oplus \\ \uparrow \\ \text{Offset Address} \\ \times 10H \end{array}}$$

Ans(1)d

(Ans d) memory → The memory in 8086 is organised into 4 segments, Each the segment register contains the starting location of segment.

→ The complete memory of 8086 is of 1 MB, that is 20 bits addressable memory is available

Note

Now this complete memory of 1 MB is divided into smaller segments each of 64 K addressable

Namely →

- (a) Extra segment Data segment
- (b) code segment
- (c) Stack segment
- (d) Extra segment

Each of these segments are addressed by an address stored in corresponding segment registers → CS (code segment), SS (Stack segment), DS (Data segment), ES (Extra segment)

These register contain a 16 bit Base address that points to the lowest address byte of the segment.

Each segment is made up of contiguous memory locations. It is an independently separately addressable unit. Starting Address will always be changing it will not be fixed.

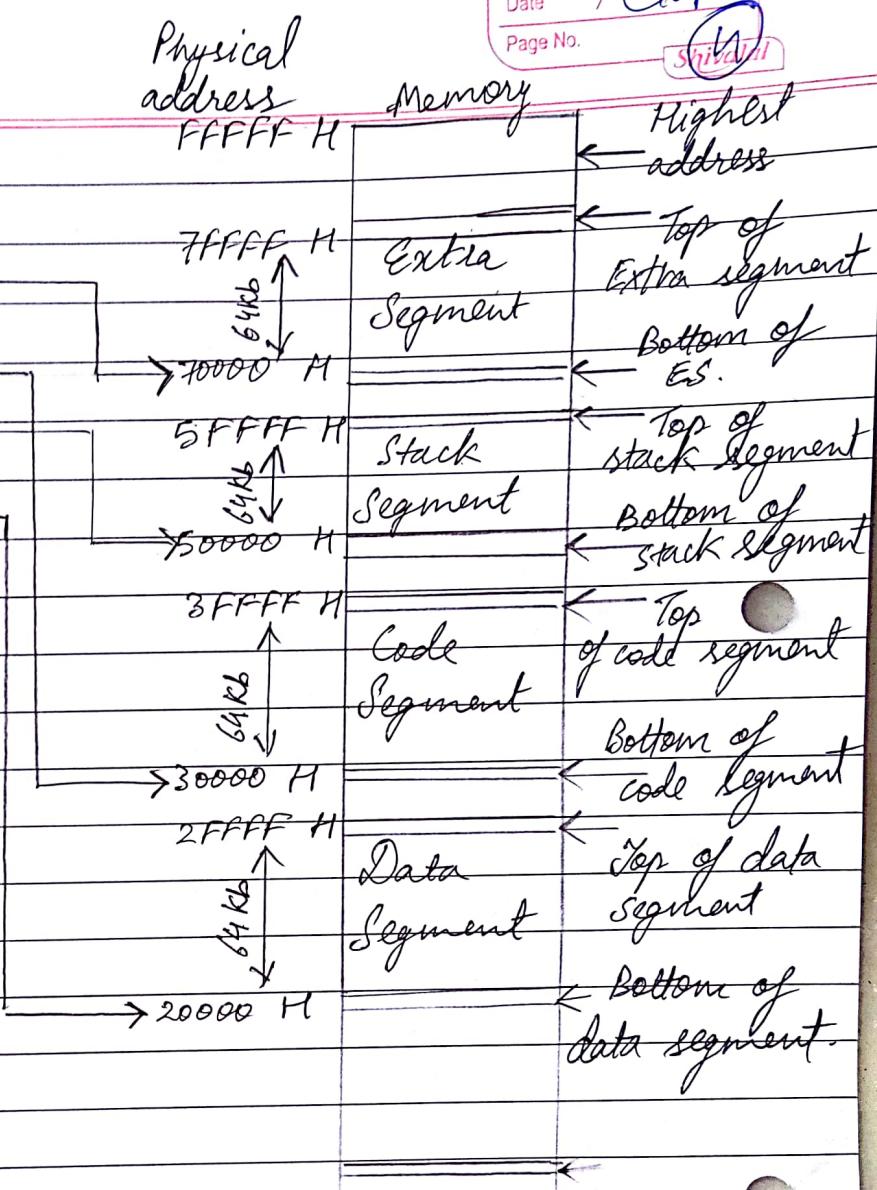
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Shivam

Your Segment  
registers in BIU

ES	7	0	0	0
CS	3	0	0	0
SS	5	0	0	0
DS	2	0	0	0



↳ memory organisation in 8086 !

(1) Code Segment Register (CS) → This is used for addressing memory location of code segment of the memory where the Executable Program is stored.

(2) Data Segment Register (DS) → This points to the Data Segment of the memory where that Data is stored.

(3) Extra Segment Register (ES) → This also refers to the segment in the memory which is Extra <sup>Data</sup> Segment in the memory.

(4) Stack Segment Register (SS) → It is used for addressing stack segment of the memory. The Stack segment is the segment which is used to store stack Data.

\* → Conversion to Physical Address

The no of Address lines in 8086 is 20 Bits whereas as the no of Data lines is 16 Bits. The four segment Register actually contains the upper 16 Bits of the starting addresses of the four segments.

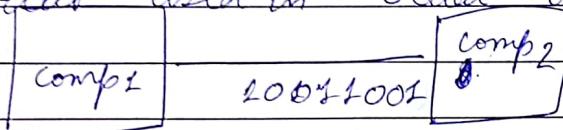
Effective Address is calculated by multiplying Segment Register value with 10<sup>4</sup> & adding offset value to it.

Ques 4.

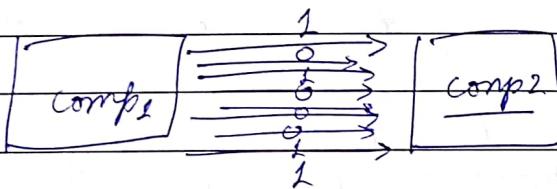
= Q(1)

Ans (a) Serial Transmission → In serial transmission, data - bit flows from one computer to another computer in bi-direction. In this transmission, one bit flows at one clock pulse. In serial transmission, 8 bits are transferred at a time having a start and stop bit.

The circuit used in serial is simple.



Parallel Transmission → In Parallel Transmission, many bits are flow together simultaneously from one comp. to another computer. Parallel transmission is faster than serial transmission to transmit the bits. Parallel transmission is used for short distance.



↳ The circuit used in Parallel Transmission is relatively complex.

Q(2)

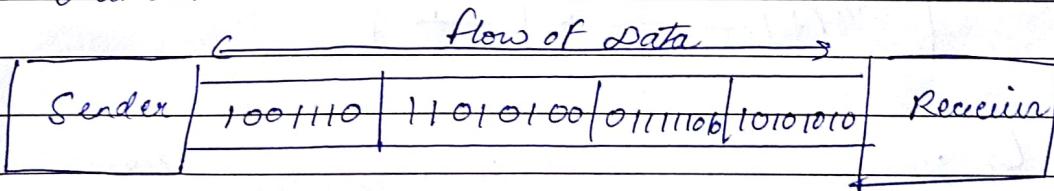
Ans(b) 8251 USART (universal synchronous asynchronous receiver transmitter) acts as an mediator between microprocessor and peripheral to transmit serial data into

Parallel form and vice versa.

- (1) It takes data serially from Peripheral (outside devices) and converts into Parallel Data.
- (2) After converting Data into Parallel form, it transmits it to CPU.
- (3) similarly it receives Parallel data from microprocessor & converts it into serial form.
- (4) After converting data into serial form, it transmits it outside device.

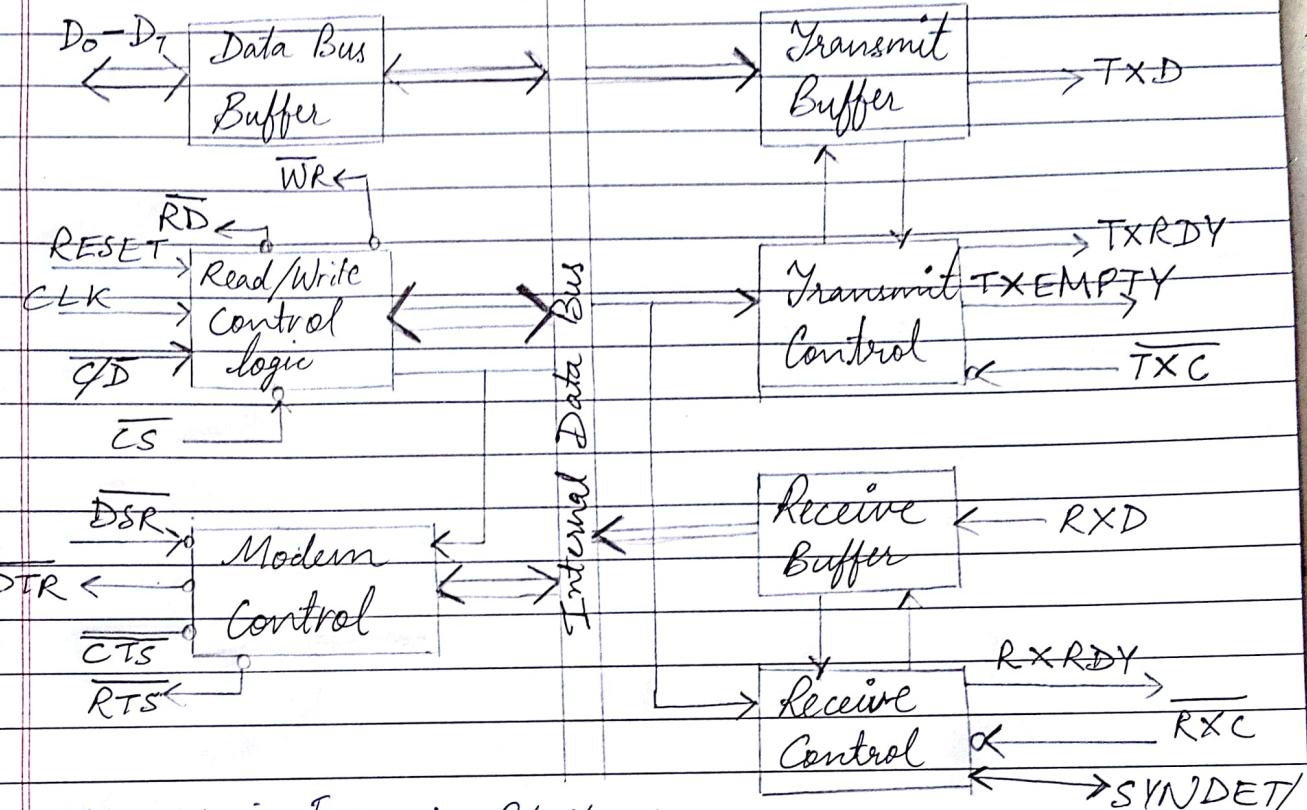
Synchronous →

(Ans) (i) In Synchronous transmission, data is sent in form of blocks or frames. Other transmission is the full duplex type. Between sender & receiver the synchronization is compulsory. It is more efficient & more reliable than Asynchronous. There is no gap present between the data.



(ii) Parity → A Parity Bit or a check bit is a bit added to a string of binary code. Parity bits are used as the simplest form of error detecting code. Parity bits are -

(Ans d)

Block diagram of 8251 USART

It contains following blocks →

(1) Read / write control logic →

It is a control block for overall working by selecting the operation to be done. The operation depends on the input signals as →

	$\bar{CS}$	$C/D$	$\bar{RD}$	$\bar{WR}$	operation
1	X	X	X	X	Invalid
0	0	0	0	1	$CPU \leftarrow 8251$ (data)
0	0	1	1	0	$CPU \rightarrow 8251$ (data)
0	1	0	0	1	Status control ( $CPU \leftarrow 8251$ )
0	1	1	1	0	$CPU \rightarrow 8251$ (control 8251)

In this way this unit selects one of the three registers, data buffer, control, status register

(ii) Transistor Buffer  $\rightarrow$  This block is used for Parallel to Serial conversion. It receives a parallel bus as input and produces a serial signal as output. The serial signal is transmitted through a transmission line to another computer system. The serial signal is converted back into parallel format at the receiving end.

- QSF : **QSF** set Read signal to off signal
  - QTR : **QTR** Terminal Ready is an off signal
  - CTS : **CTS** is an output signal which can be used as an off signal
  - RTS : **RTS** is an off signal used to set the driver RTS.

Analog device converts analog signals to digital signals and vice versa that helps the communication to exchange data between telephone lines or cable circuit. The following are advantages of fiber optics.

(3) modern control (modulator / active controller)  $\rightarrow$

(5) Transmit Control → This Block is used to control the data transmission with the help of following pins.

- TXRDY → It means transmitter is ready to transmit Data character.
- TXEMPTY → An output signal which indicates that TXEMPTY Pin has transmitted all the data characters and Transmitter is empty now.
- TXC → An active - low input Pin which controls the data transmission rate of transmitted Data.

(6) Receive Buffer → This Block acts as a Buffer for the received Data.

- RXD → An I/P signal which receives the Data.

(7) Receive Control → This Block controls the receiving Data.

- RXRDY → An input signal, indicates that it is ready to receive the Data.
- RXC → An Active - low input signal which controls the data transmission rate of received Data.
- SYNDET / BD → An I/P or O/P terminal. External synchronous mode = I/P terminal and asynchronous mode = O/P terminal.

Ques 5

(Ans a) RS1 and RS0 bits in the PSW register are used to select different memory locations (Bank 0 to Bank 4) in the RAM.

RS0 → Register Bank selector Bit 0

RS1 → Register Bank selector Bit 1

We can select corresponding Register Bank Bit using this

RS1	RS0	Value	
0	0	00H	Bank 0
0	1	08H	Bank 1
1	0	10H	Bank 2
1	1	18H	Bank 3

(Ans b) microprocessor consists of only a central Processing unit, whereas micro controller contains a CPU, memory, I/O all integrated in 1 chip.

(a) microprocessor is complicated whereas microcontroller is straight forward.

(b) microprocessor is expensive whereas microcontroller is inexpensive.

(c) microprocessor have large number of instructions to process whereas in microcontroller it has

fewer instructions to Process.

- (d) It has one - chip oscillator.

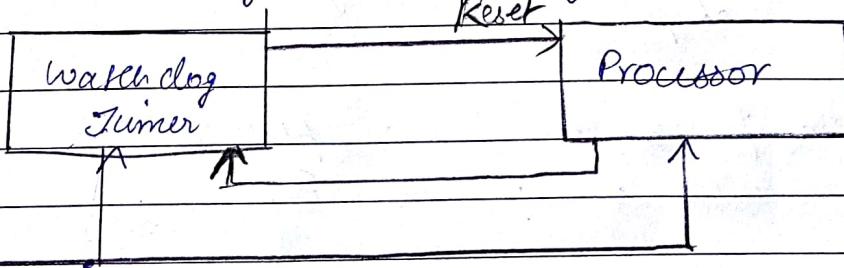
Ans

A watch dog timer is a specialized timer module that helps a microprocessor to recover from malfunctions. If a watch dog timer reaches the end of its count period; it resets the entire processor system.

In order to prevent this a processor must perform some type of specific action that resets the watchdog.

A watchdog timer is a piece of hardware that can be used to automatically detect software anomalies and reset the processor.

Below is a typical watchdog setup →

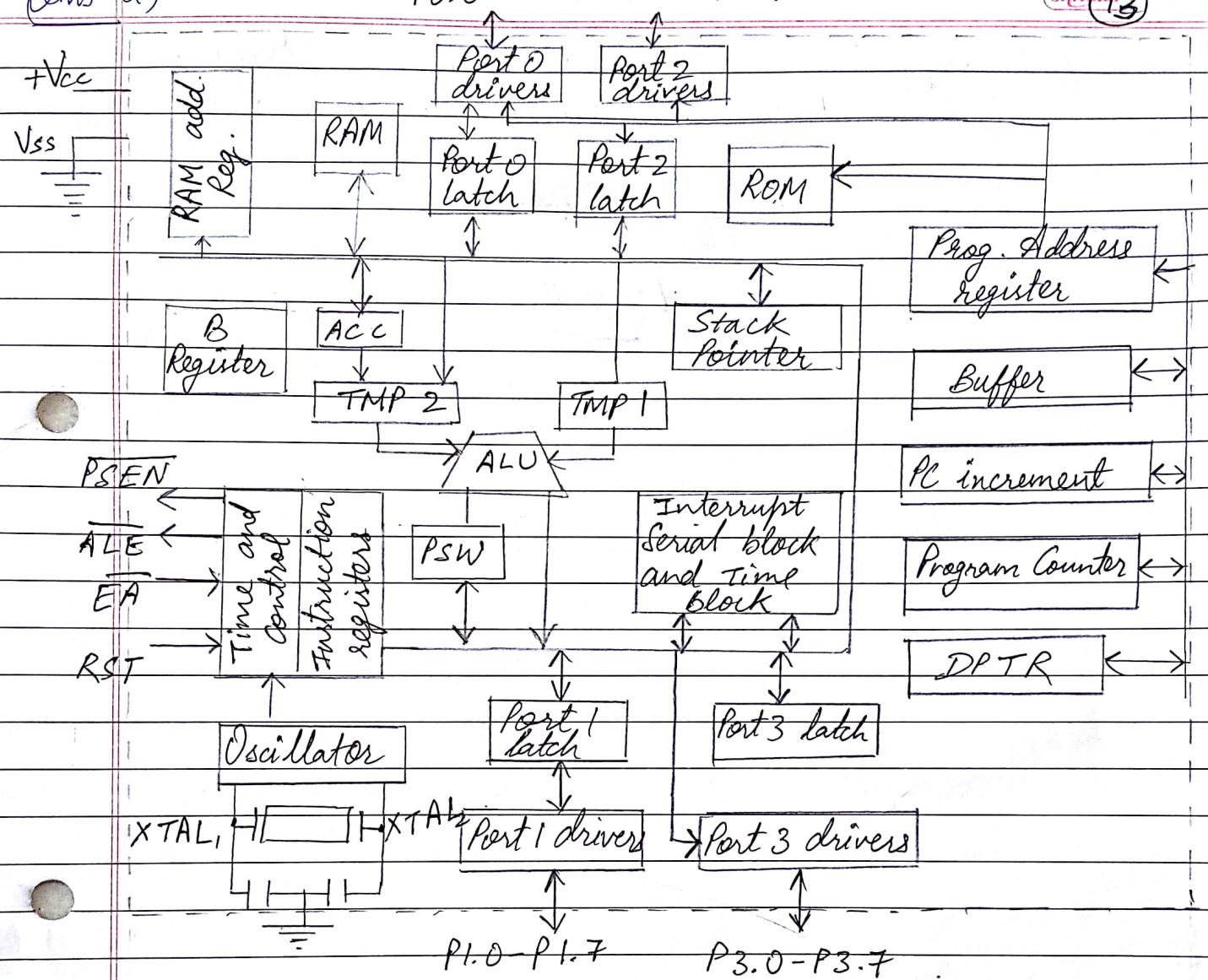


Clock

The process of restarting the watchdog timer's counter is sometimes called 'kicking the dog'.

(Ans - d)  
5)

P0.0 - P0.7 P2.0 - P2.7

~~8051~~ 8051 Block DiagramApplications of microcontroller 8051

- (2) Application of microprocessor 8051 in medical applications - Patient Health monitoring system with location details by GPS over GSM Project.

Pujala

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(b)oral

(2) Application of microcontroller 8051 in  
electronics :- EVM - Electronic voting machine.

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