ECE 2029 INTRODUCTION TO DIGITAL CIRCUIT DESIGN

WPI

Lab 1: Build and Simulate Digital Logic Circuits

Sign-Off Sheet

Date: 3/20/19

Student 1: [redacted] **ECE mailbox:** 1

Student 2: [redacted] **ECE mailbox:** 238

YOU ARE RESPONSIBLE TO COMPLETE ALL THE ASSIGNMENTS IN THE CHECK LIST BELOW IN ORDER TO GET FULL CREDIT FOR THE LAB...

After getting this sheet signed-off by the TA, please upload it on CANVAS to receive the GRADE!!

Check List	
Assignments	**TA Sign-off**
Pre-Lab (MUST be completed before the start of the lab) Watch Videos Complete the truth table	Renuka 03/20/2019
Part 1: Verifying Digital Logic using Tinkercad	03/20/2019
Part 2: Verify the Rules and regulations of Boolean Algebra using Logisim	YZ 03/20
Project File(s) Upload on CANVAS Screenshots of circuit(s) from TinkerCAD .c/.circ file for Logisim	YZ 03/20

Due Date: 03/27/2019

***Both Students MUST be present at Sign-off for any and all parts!!**

PRE-LAB

Complete the truth table for the Basic Digital Logic Gates below:

Also drive the Boolean expression for each logic gate.

AND Gate

A	B	Output
0	0	
0	1	
1	0	
1	1	

NOT Gate

A	Output
0	
1	

XOR Gate

A	B	Output
0	0	
0	1	
1	0	
1	1	

OR Gate

A	B	Output
0	0	
0	1	
1	0	
1	1	

NAND Gate

A	B	Output
0	0	
0	1	
1	0	
1	1	

NOR Gate

A	B	Output
0	0	
0	1	
1	0	
1	1	

Part 1: Verifying Digital Logic using Tinkercad

OR, AND, NAND, NOR, and XOR gates.

1. Use one gate for each IC 7400 (NAND), 7402 (NOR), 7408 (AND), 7432 (OR), 7486 (XOR) and verify the logic. See Fig. 2 to identify input and output pins for each gate. Pins 7 and 14 are ground (0 V) and V_{cc} (5 V).
2. [IC7400]Connectinputpins1and2usingjumperwirestoapplylogic(0GND,15V).Connect output pin 3 to LED as shown in Fig 3 as an example for the NAND gate.

Remember: LED ON = Logic 1 (High) and LED OFF = Logic 0 (Low)

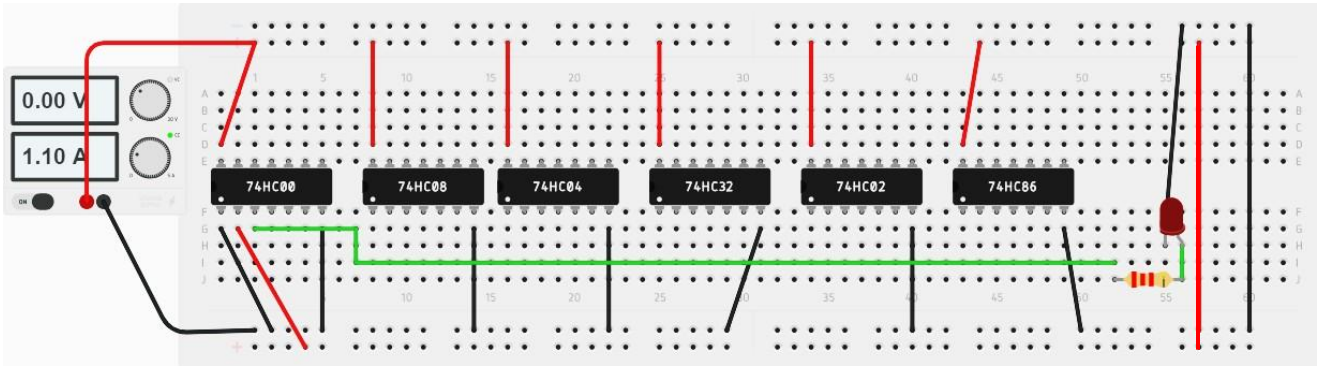


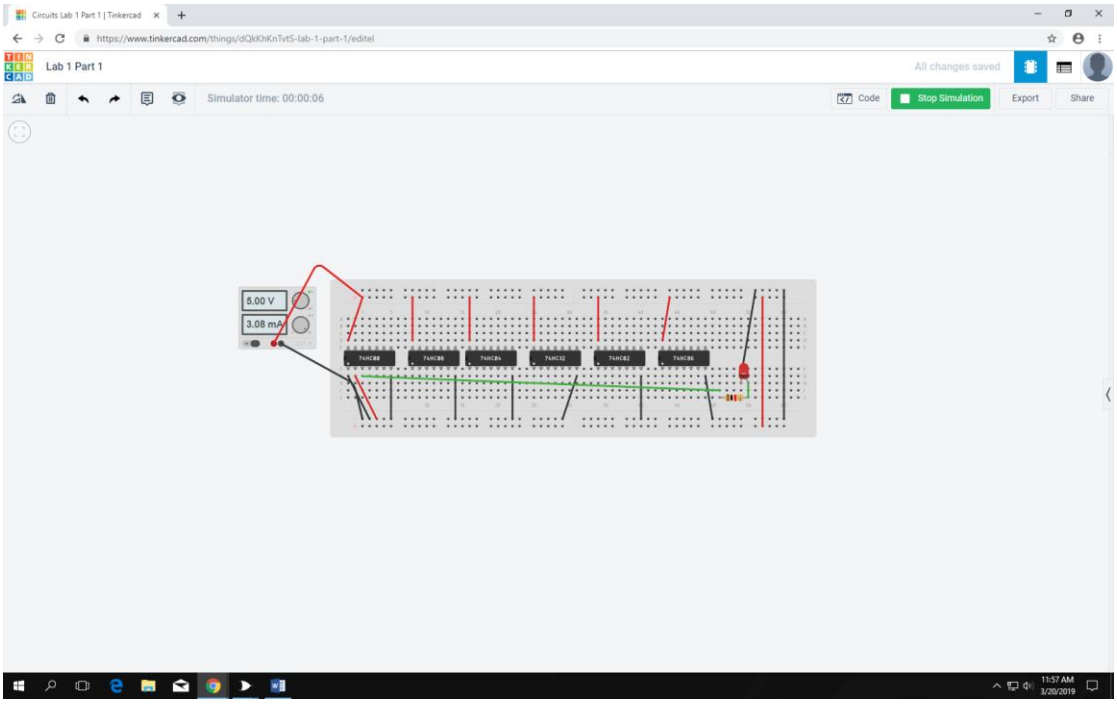
Fig. 3

3. Apply the logic levels 0 and 1 in the sequence shown in table 1. Record the output logic levels. Repeat the recordings for each digital logic gate.

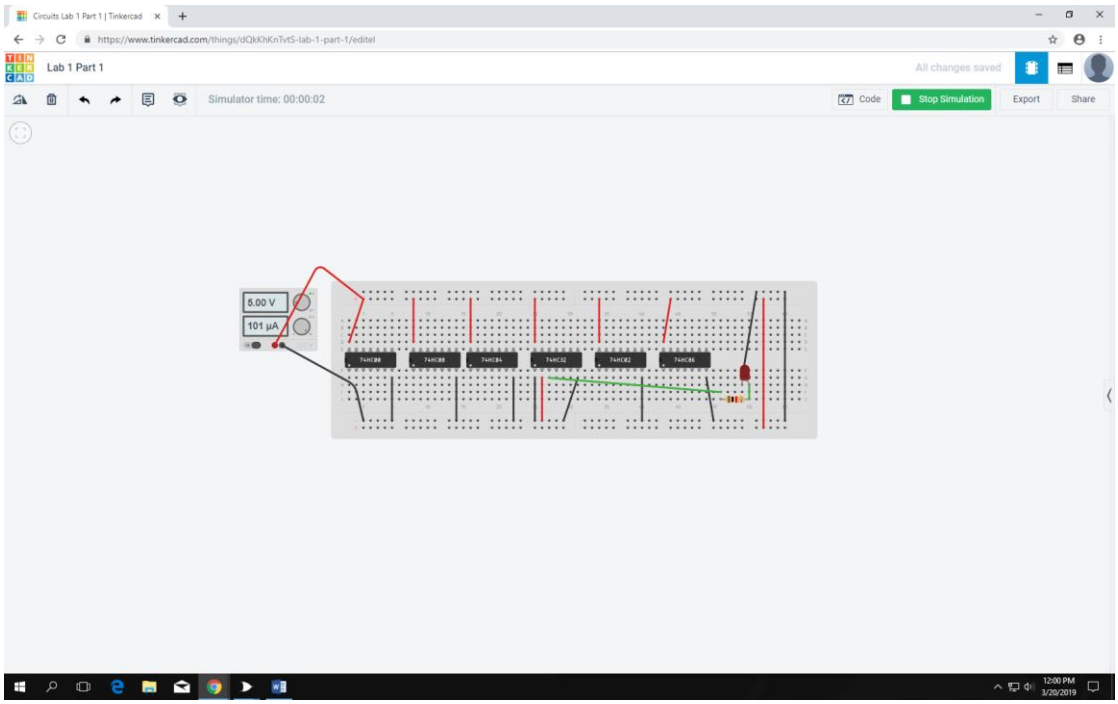
Table 1 Output Response

Input Pins		Output Pin				
		Pin 3				
Pin 1	Pin 2	OR	AND	NAND	NOR	XOR
0	0					
0	1					
1	0					
1	1					

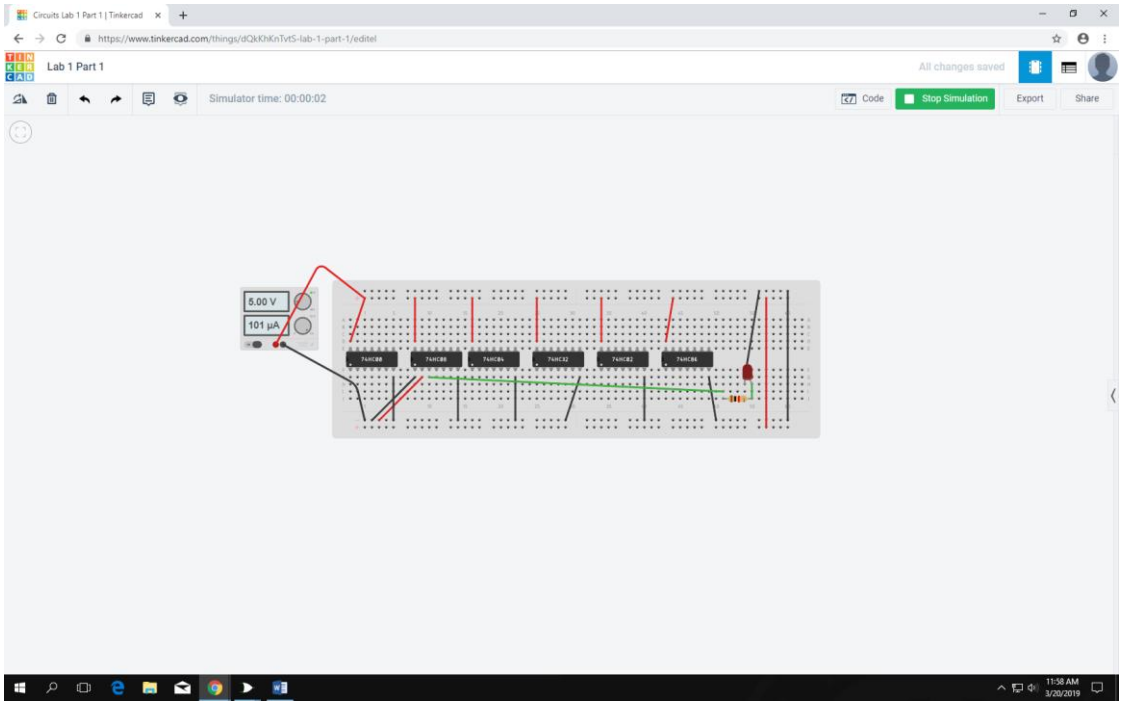
NAND - Logic set to: input 1= 0, input 2 = 0



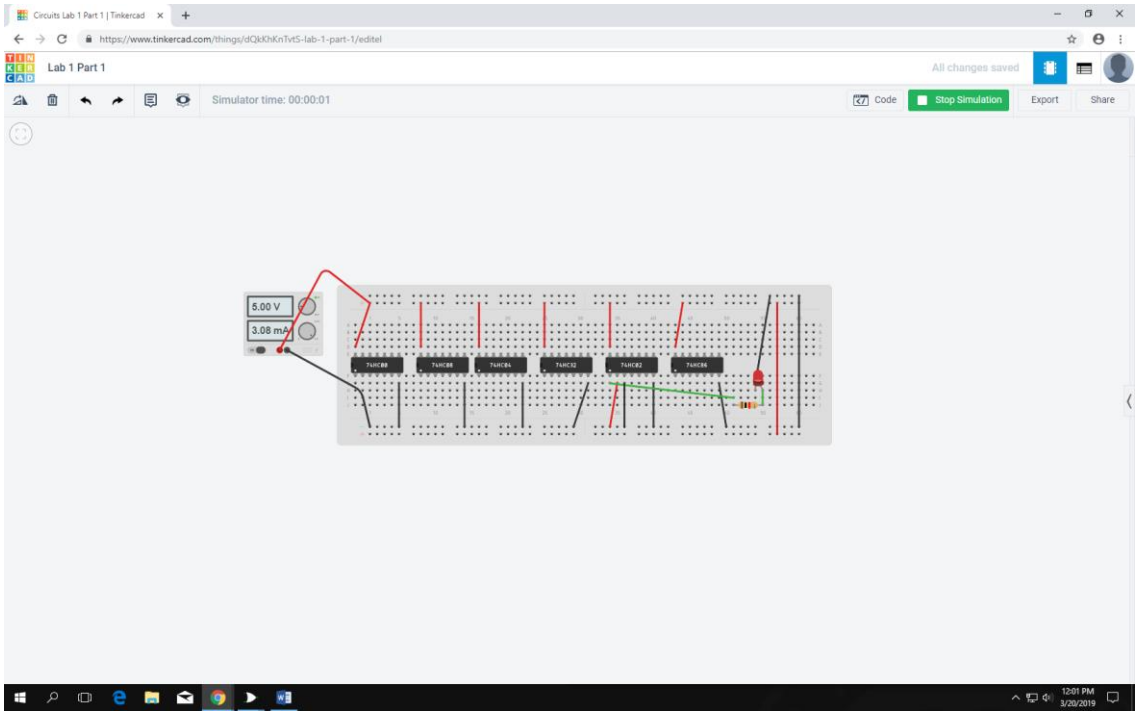
OR - Logic set to: input 1= 0, input 2 = 0



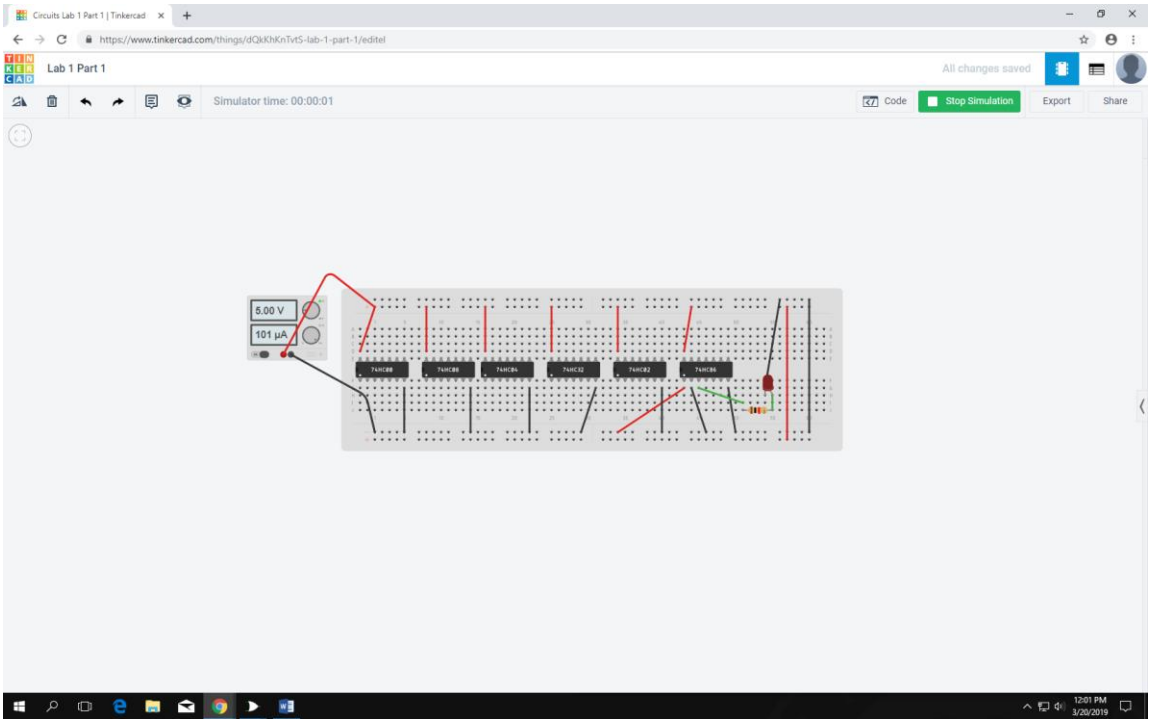
AND- **Logic set to: input 1= 0, input 2 = 0**



NOR- Logic set to: input 1= 0, input 2 = 0



XOR - Logic Set to: input 1= 0, input 2 = 0



4. Use an inverter gate from **IC 7404** whose input pin is pin 1 and whose output pin is pin 2. Apply the logic levels 0 and 1 in the sequence shown in table 2. Record the output logic levels.

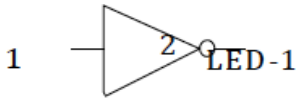
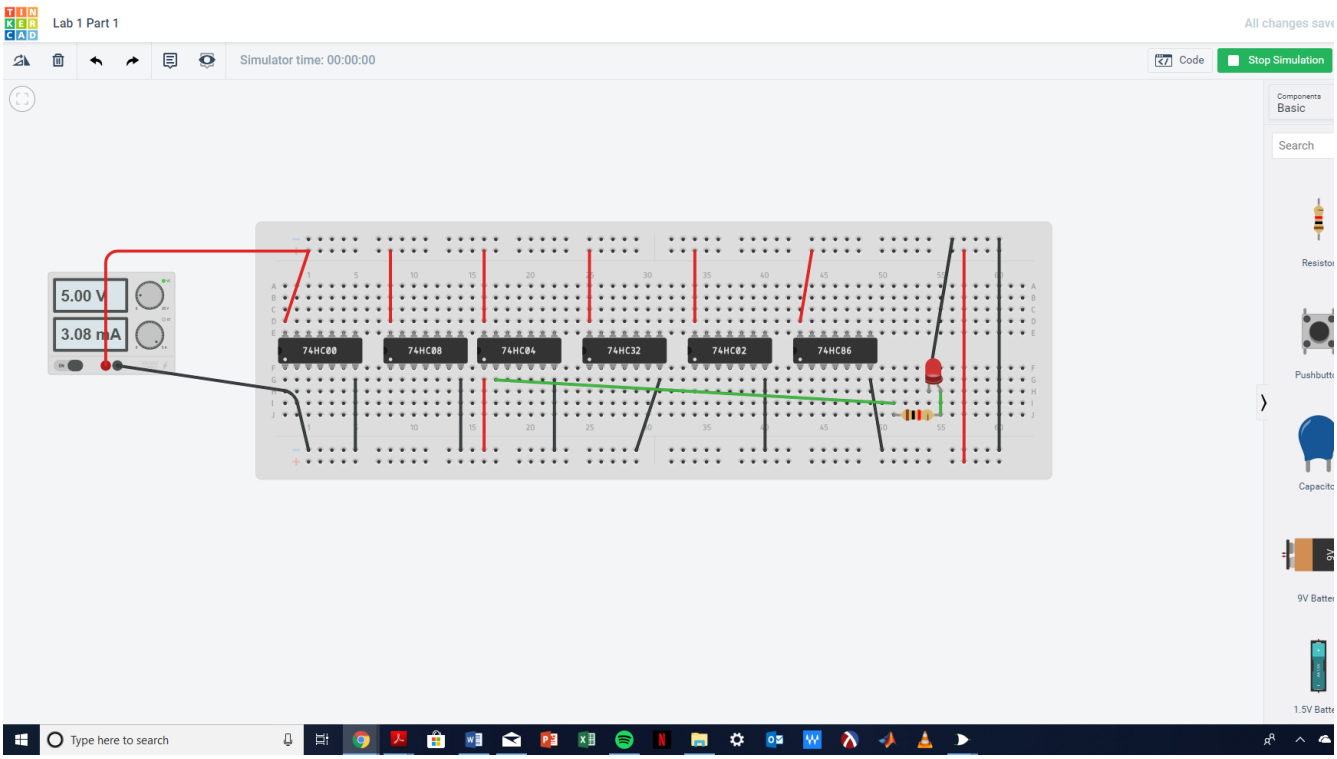


Fig.4 Inverter gate

Table 2.

Pin 1	Pin 2
0	
1	

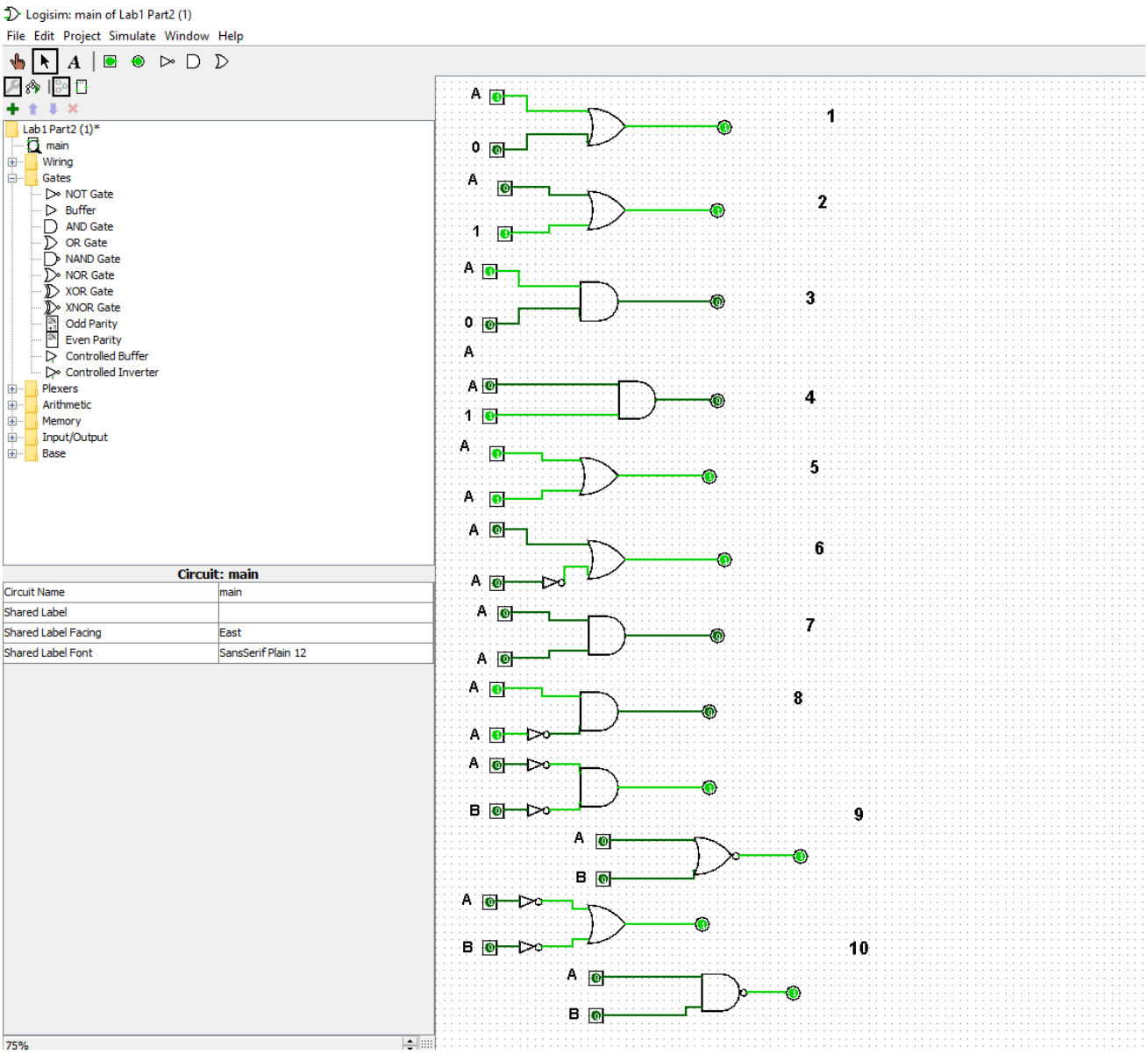
(NOT – Logic Set to input 0)



Part2:VerifytheRulesandregulationsofBooleanAlgebrausingLogisim

Using digital logic gates, design a digital circuit to verify the following expressions:

1. A+0 =A
2. A+1 = 1
3. A .0 = 0
4. A .1 =A
5. A+A = A 6. A+A' =1
7. A.A =A 8. A.A' =0
9. A'. B' = (A+B)'
10. A'+B' = (A.B)'



Build the following circuit using Logisim and verify the logic. Record the values in the table below:

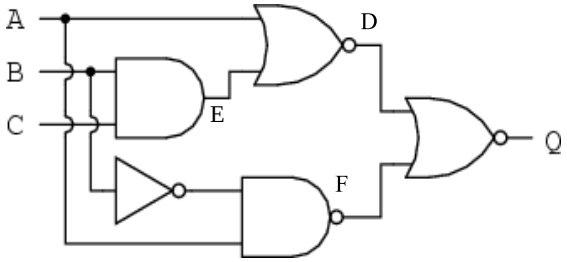
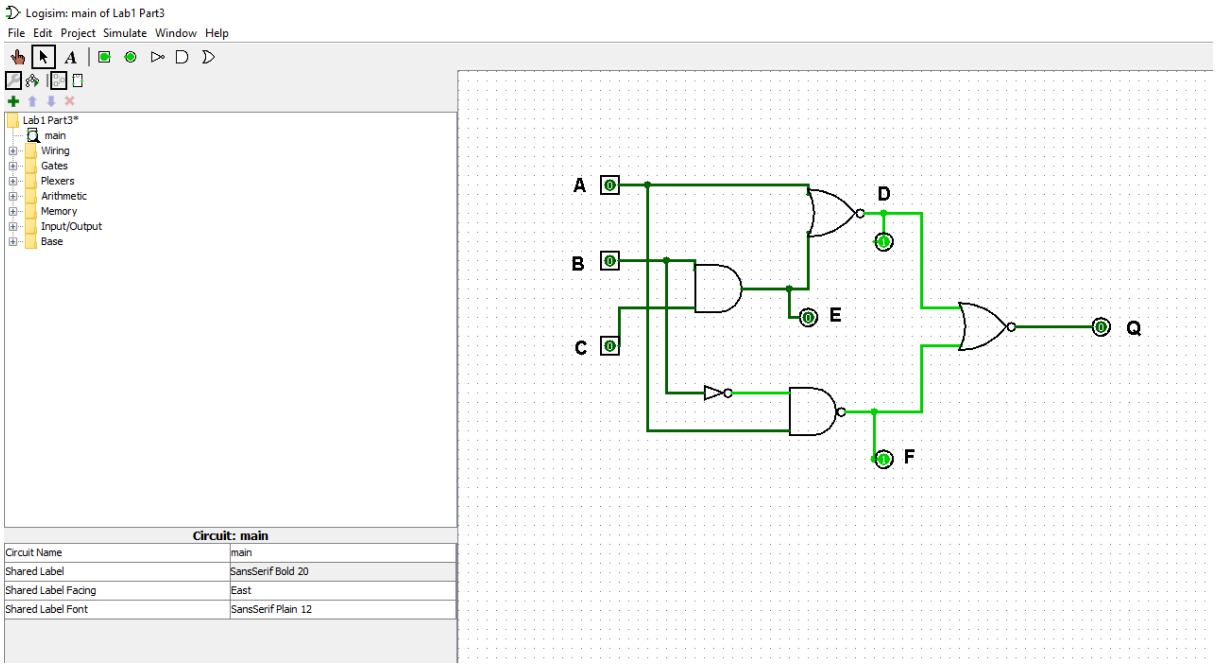


Fig. 5

Table 3 Output Response of Circuit in Fig. 5



Inputs			Outputs			
A	B	C	D	E	F	Q
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

Verify the recorded values for Q in the table 3 by analyzing the circuit using Logisim and get the Boolean expression for Q.