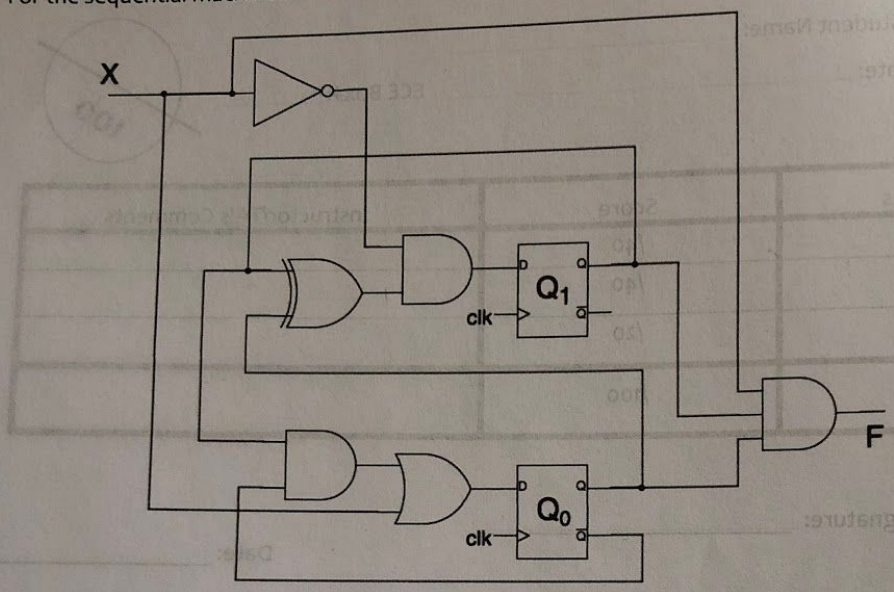
Problem 1 – 40 points total

For the sequential machine shown:



a) Determine the Boolean expressions for next state logic and output logic from the circuit. That is, express $Q1^+$, Qo^+, and F as logic expressions in terms of Q1, Qo, and X.
(Do not write $Q1^+$, Qo^+ logic expressions in terms of F since F is the output)

(15 pts)

$F = X \cdot Q_1 \cdot Q_0$

$Q_1^* = \overline{X} \cdot (Q_0 \oplus Q_1)$

$Q_0^* = (Q_1 \cdot \overline{Q}_0) + X$

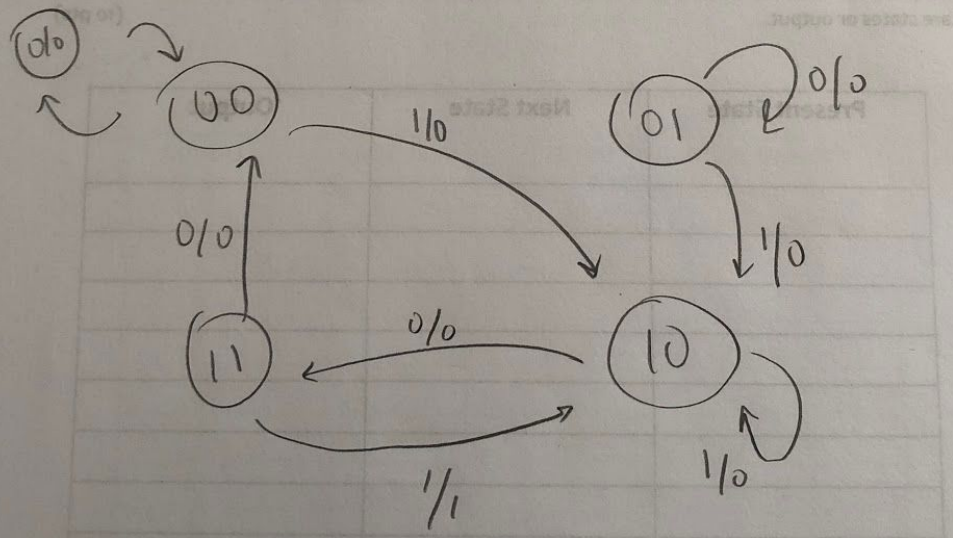
b) Fill in the state table, given below:

(15 pts)

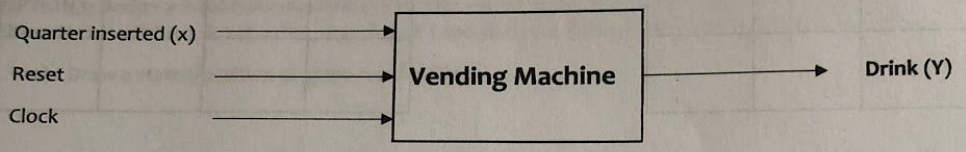
Present State	Input	Next State	Output
Q_0Q_1	X	$Q_0^+Q_1^+$	F
0 0	0	0 0	0
0 0	1	1 0	0
0 1	0	0 1	0
0 1	1	1 0	0
1 0	0	1 1	0
1 0	1	1 0	0
1 1	0	0 0	0
1 1	1	1 0	1

c) Draw a state transition diagram for this sequential machine.

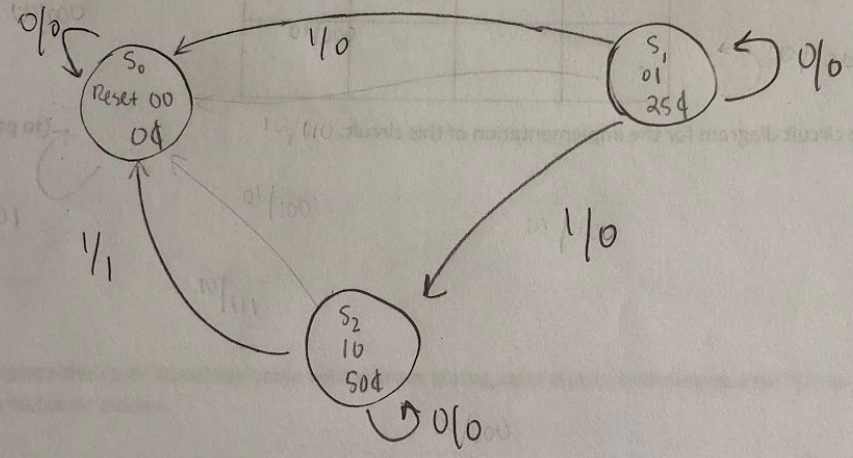
(10 pts)



OPTION 2: Design a controller for a vending machine. It sells soda only and each cost 75 cents. The machine accepts quarter coins only and one quarter at a time. Once it receives 75 cents, it automatically dispenses a soda can and back to the initial reset state. You do not need to consider the changes or coin return scenarios.



a) Draw a state transition diagram for this vending machine controller. (5 pts)



b) List a state transition table with input, output, current states, and next states. (10 pts)

Present State	Input	Next State	Output
Q_1 Q_0	X	Q_1^+ Q_0^+	Y
0 0	0	0 0	0
0 0	1	0 1	0
0 1	0	0 1	0
0 1	1	1 0	0
1 0	0	1 0	0
1 0	1	0 0	1
1 1	0	X X	X
1 1	1	X X	X

c) Derive the logic expression for the input of each D-Flip Flop and output Y. (15 pts)

Q_1^+

Q_1, Q_0	00	01	11	10
0	0	0	X	1
1	0	1	X	0

Q_0^+

Q_1, Q_0	00	01	11	10
0	0	1	X	0
1	1	0	X	0

$Q_0^+ = \bar{X}Q_0 + XQ_1$

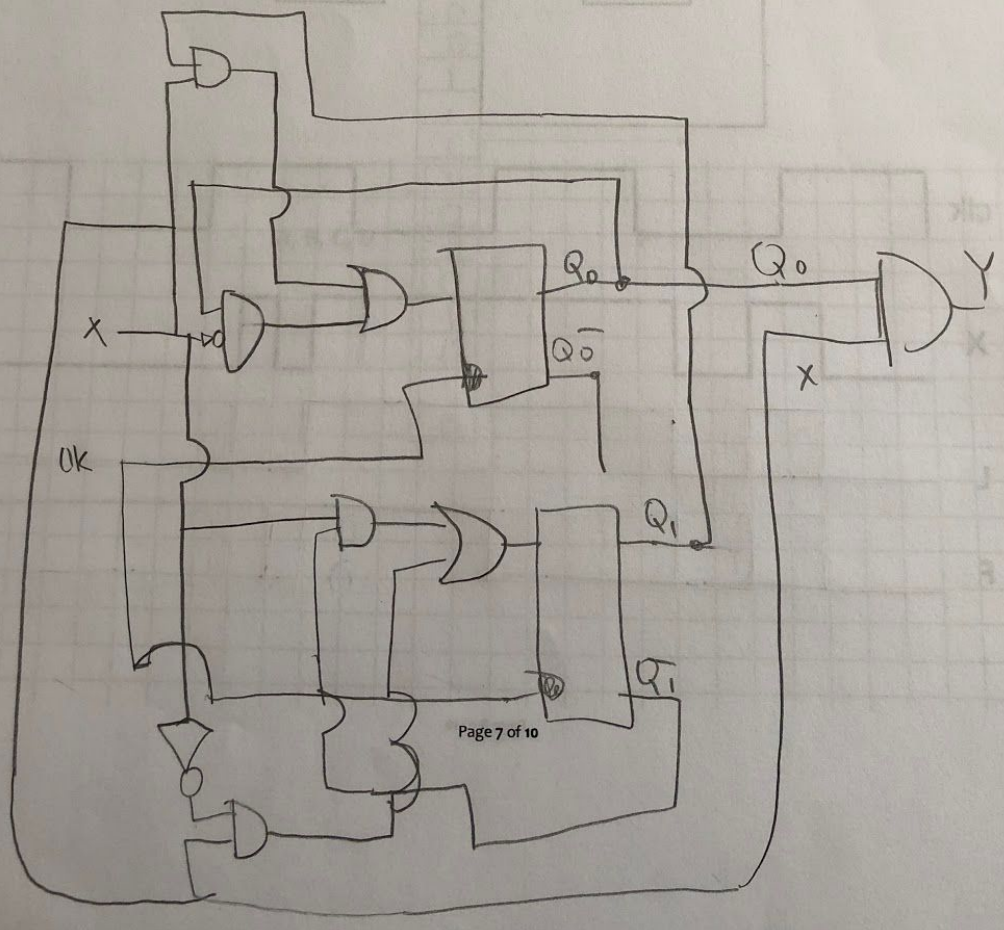
$Q_1^+ = X\bar{Q}_0\bar{Q}_1 + \bar{X}Q_1$

$Y = XQ_0$

Y

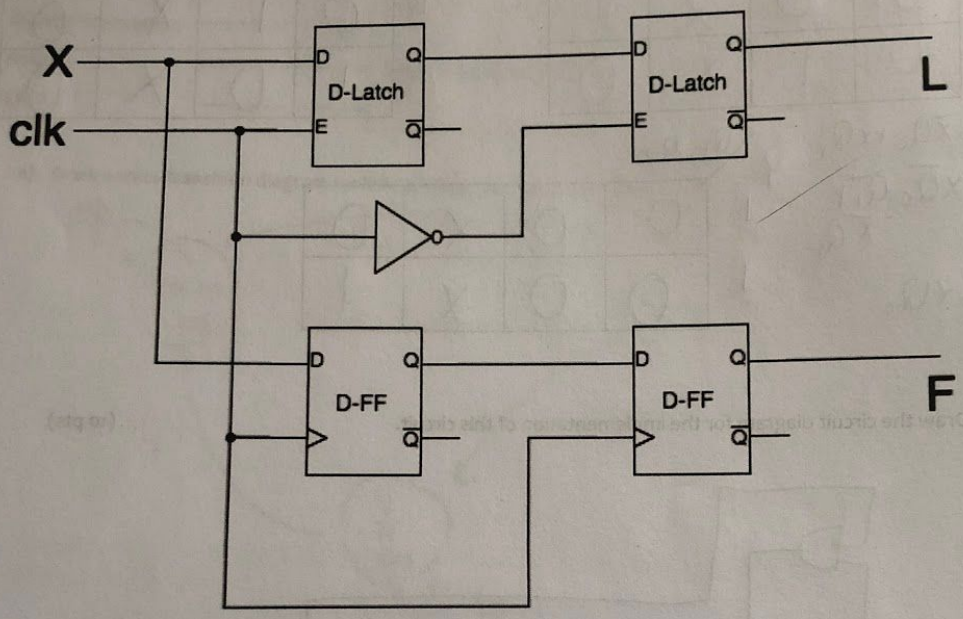
Q_1, Q_0	00	01	11	10
0	0	0	X	0
1	0	0	X	1

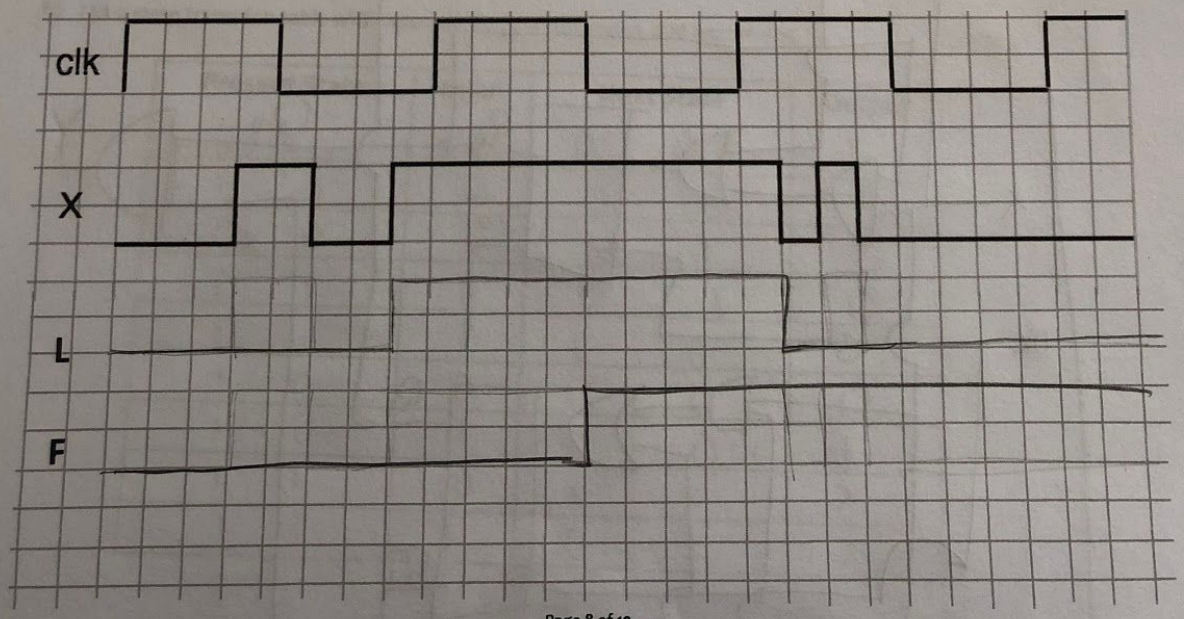
d) Draw the circuit diagram for the implementation of this circuit. (10 pts)



Problem 3– 20 points total

a) Given the circuit diagram below, complete the waveform for L and F. Assume the D-Flip Flops are rising-edge triggered and initialized to 0. (15 pts)





b) FPGA implements combinational logic using look-up tables (LUTs). Assume the size of each LUT is only 16-bit that is equivalent to a memory space with 4-bit input and 1-bit output. Fill the LUT contents to implement logic function: (Hint: Use logic cells in K-Map to derive output) (5 pts)

$Y = B'D' + A'BD + CD' + AD'$

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	1	1	1
11	1	0	0	1
10	1	0	0	1

Fill the memory contents: