Homework #3

Problem 1 – 35 points total

We will design part of a set of logic circuits that tests numbers for divisibility for certain prime numbers as part of an information encryption system. The binary number A is represented by a four bit unsigned number: A = (a_3; a_2; a_1; a_0) where a_0 is the least significant bit, etc. The circuit you must design will have a single **output, F**, which must take on the value of **1** if A is divisible by 3 or 7 and zero otherwise, except when A = 0 (which is "technically" divisible by any number) for which case we want **F = 0.**

(a) Give the truth table for F as a function of a_3; a_2; a_1; a_0. **(5 pts)**

	a_0	a_1	a_2	a_3	**F**
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	1
13	1	1	0	1	0
14	1	1	1	0	1
15	1	1	1	1	1

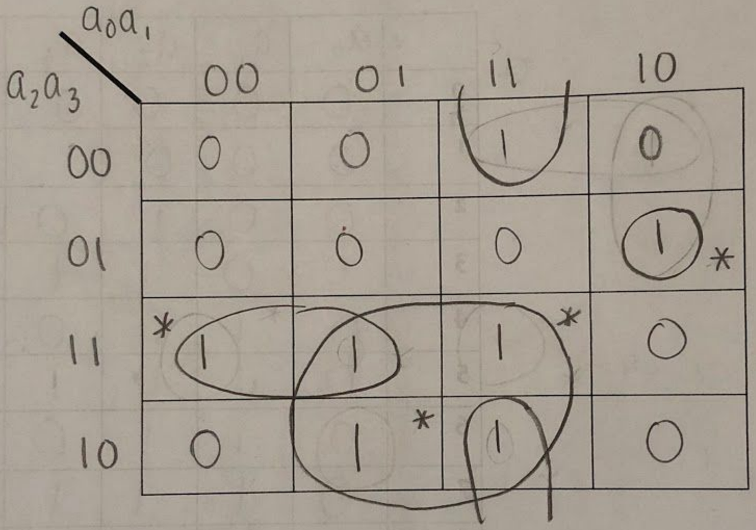
(b) Write out the canonical sum of Minterms expression for F. **(5 pts)**

F = $\bar{a}_0\bar{a}_1a_2a_3 + \bar{a}_0a_1a_2\bar{a}_3 + a_0\bar{a}_1\bar{a}_2a_3 + a_0a_1\bar{a}_2\bar{a}_3 + a_0a_1a_2a_3 +$

$\bar{a}_0a_1a_2a_3 + a_0a_1a_2\bar{a}_3$

(c) Obtain a simplified expression for F using a Karnaugh Map. **(5 pts)**

Label essential prime implicants (EPI) with asterisk sign on the K-Map!

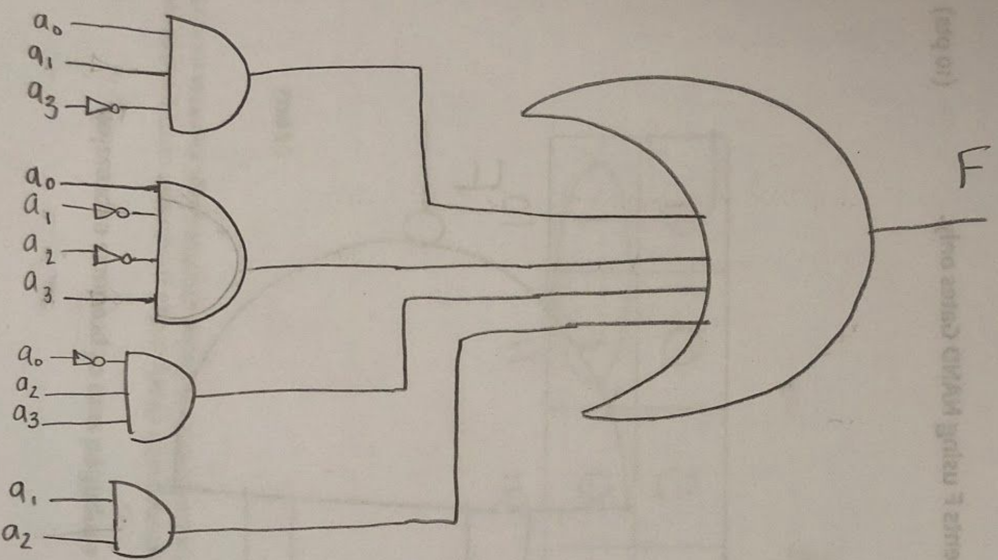


a_2a_3 \ a_0a_1	00	01	11	10
00	0	0	1	0
01	0	0	0	1 *
11	* 1	1	1 *	0
10	0	1 *	1	0

F = $a_1a_2 + a_0a_1\overline{a_3} + \overline{a_0}a_2a_3 + a_0\bar{a}_1\bar{a}_2a_3$

$\underline{a_1 a_2} + \underline{a_0 a_1 \bar{a}_3} + \underline{\bar{a}_0 a_2 a_3} + a_0 \bar{a}_1 \bar{a}_2 a_3$

(d) Draw the combinational logic circuit diagram that implements F. **(5 pts)**



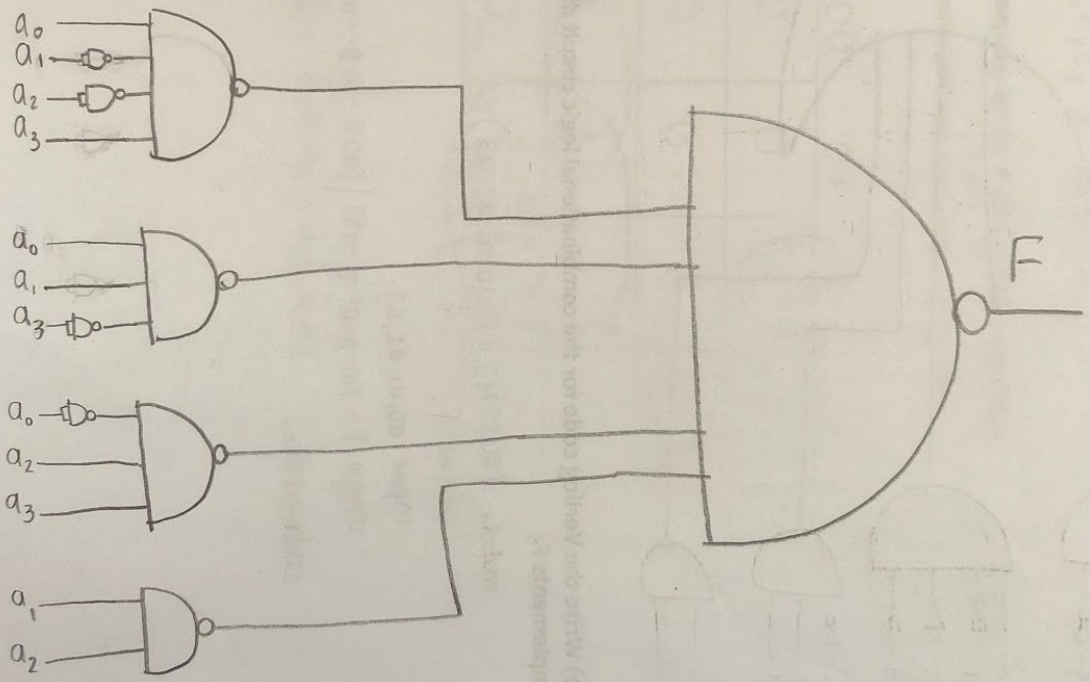
(e) Write the Verilog code for the combinational logic circuit diagram that implements F. **(5 pts)**

```
module PROBLEM1 (F, a0, a1, a2, a3);
    output F;
    input a0, a1, a2, a3;
    assign F= (a0 & a1 &~a3) | (a0 &~a1 & ~a2 & a3) | (~a0 & a2 & a3) | (a1 & a2);
endmodule
```

(f) Draw the combinational logic circuit diagram that implements F using NAND Gates only. (

$$\bar{\bar{F}} = \overline{\overline{a_1a_2 + a_0a_1\overline{a_3} + \overline{a_0}a_2a_3 + a_0\bar{a}_1\bar{a}_2a_3}}$$

$$\bar{\bar{F}} = \overline{\overline{a_1a_2} \cdot \overline{a_0a_1\bar{a}_3} \cdot \overline{\bar{a}_0a_2a_3} \cdot \overline{a_0\bar{a}_1\bar{a}_2a_3}}$$



Problem 2 - 20 points total

For each of the following truth tables, use a Karnaugh map to produce a **simplified sum of products expression.**

The X's in the tables indicate "don't cares". Be sure to show your Karnaugh map with clearly circled groups that correspond to your sum of products solution. Please draw your final Karnaugh maps, clearly labeled and the resulting simplified logic expressions next to them.

(5 pts)

(a) Three Variable Map

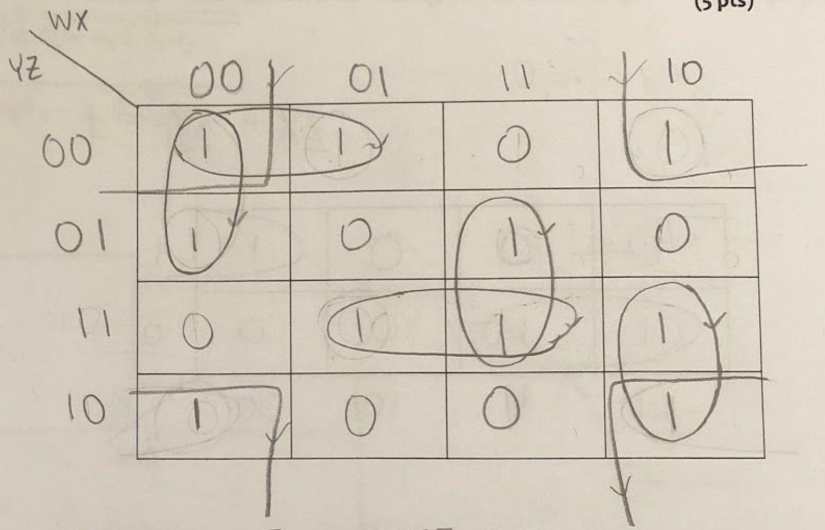
X	Y	Z	A
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

X \ YZ	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$F = \bar{X}Y + X\bar{Z}$

(b) Four Variable Map **(5 pts)**

W	X	Y	Z	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1



YZ \ WX	00	01	11	10
00	1	1	0	1
01	1	0	1	0
11	0	1	1	1
10	1	0	0	1

F = $WXZ + W\bar{X}Y + \bar{W}\bar{X}\bar{Y} + \bar{X}\bar{Z} + XYZ + \bar{W}\bar{Y}\bar{Z}$

(c) Three Variable Map (5 pts)

X	Y	Z	C
0	0	0	0
0	0	1	1
0	1	0	X
0	1	1	1
1	0	0	0
1	0	1	X
1	1	0	0
1	1	1	X

Z \ XY	00	01	11	10
0	0	X	0	0
1	1	1	X	X

C = Z

(d) Four Variable Map (5 pts)

W	X	Y	Z	D
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	X
0	1	1	0	1
0	1	1	1	X
1	0	0	0	1
1	0	0	1	X
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	X
1	1	1	1	0

D = $W'X + Y'X' + ZX' + Y'Z$

WX \ YZ	00	01	11	10
00	1	1	1	0
01	1	X	X	1
11	0	1	0	X
10	1	X	1	0

Problem 3 - 45 points total

For the function given:

$$F = (A + B + C) . (A + B' + C) . (A + B' + C') . (A' + B' + C')$$

(a) Produce a truth table that expresses F as a function of A, B, and C. **(5 pts)**
Note: You can do this on Logisim also.

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b) Use a Karnaugh map to produce a simplified sum of products form. (Show both the Karnaugh map and Sum of Product expression.) **(5 pts)**

C \ AB	00	01	11	10
0	0	0	1	1
1	1	0	0	1

SOP = $A\overline{C} + \overline{B}C$

3a)

$$(A+B+C)\cdot(A+B'+C)\cdot(A+B'+C')\cdot(A'+B'+C')$$

$$(0,0,0)\quad \overset{0}{(0+0+0)}\cdot\overset{1}{(0+1+0)}\cdot\overset{1}{(0+1+1)}\cdot\overset{1}{(1+1+1)} = 0$$

$$(0,0,1)\quad \overset{1}{(0+0+1)}\cdot\overset{1}{(0+1+1)}\cdot\overset{1}{(0+1+0)}\cdot\overset{1}{(1+1+0)} = 1$$

$$(0,1,0)\quad \overset{1}{(0+1+0)}\cdot\overset{0}{(0+0+0)}\cdot\overset{1}{(0+0+1)}\cdot\overset{1}{(1+0+1)} = 0$$

$$(0,1,1)\quad \overset{1}{(0+1+1)}\cdot\overset{1}{(0+0+1)}\cdot\overset{0}{(0+0+0)}\cdot\overset{1}{(1+0+0)} = 0$$

$$(1,0,0)\quad (1+0+0)\cdot(1+1+0)\cdot(1+1+1)\cdot(0+1+1) = 1$$

$$(1,0,1)\quad (1+0+1)\cdot(1+1+1)\cdot(1+1+0)\cdot(0+1+0) = 1$$

$$(1,1,0)\quad (1+1+0)\cdot(1+0+0)\cdot(1+0+1)\cdot(0+0+1) = 1$$

$$(1,1,1)\quad (1+1+1)\cdot(1+0+1)\cdot(1+0+0)\cdot(0+0+0) = 0$$

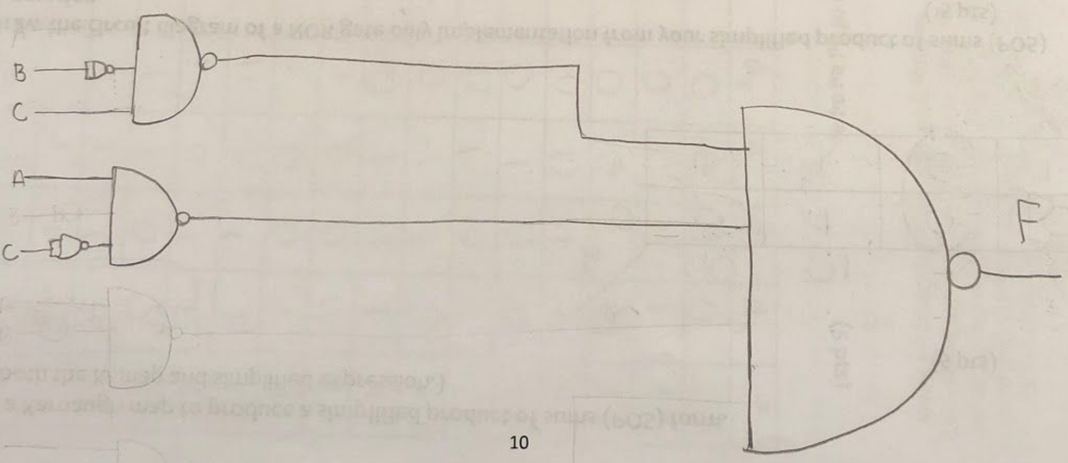
(c) Draw the circuit diagram of a NAND gate only implementation from your simplified sum of products (SOP) expression. (15 pts)

$$\bar{F} = \overline{\overline{A\bar{C} + \bar{B}C}}$$

Demorgan's Law

$$\bar{\bar{F}} = \overline{\underbrace{\underbrace{\overline{A\bar{C}}}_{\text{NAND}} \cdot \underbrace{\overline{\bar{B}C}}_{\text{NAND}}}_{\text{NAND}}}$$

2-level NAND Implementation



(d) **Use a Karnaugh map to produce a simplified product of sums (POS) form.**
(Show both the K- map and simplified expression.)

(5 pts)

$$\boxed{POS = (C+A).(B'+C')}$$

A \ BC	00	01	11	10
0	0	1	0	0
1	1	1	0	1

(e) **Draw the circuit diagram of a NOR gate only implementation from your simplified product of sums (POS) expression.**

(15 pts)

$F = ((C+A).(C'+B'))$

Double complement

$$\bar{\bar{F}} = \overline{\overline{((C+A).(C'+B'))}} = \overline{\underbrace{\overline{(C+A)}}_{NOR} + \underbrace{\overline{(C'+B')}}_{NOR}}$$

Demorgan's law

NOR

2 level implementation of NOR Gate