Lab 1 – Build and Simulate Logic Circuits

OBJECTIVE

1) To study the function of basic logic gates: AND, OR, INVERT, NAND, XOR, and NOR.
2) To study the representation of these functions by truth tables, logic diagrams and Boolean algebra.
3) To build and simulate logic circuits, observe and verify the output response.

THEORY

AND — A multi-input circuit in which the output is 1 only if all inputs are 1. The symbolic representation of the AND gate is shown in Fig. 1a.

OR — A multi-input circuit in which the output is 1 when any input is 1. The symbolic representation of the OR gate is shown in Fig. 1b.

INVERT — The output is 0 when the input is 1, and the output is 1 when the input is 0. The symbolic representation of an inverter is shown in Fig. 1c.

NAND — AND followed by INVERT. The symbolic representation of the NAND gate is shown in Fig 1d.

NOR — OR followed by INVERT as shown in Fig 1e.

EX-OR — The output of the Exclusive –OR gate, is 0 when it's two inputs are the same and its output is 1 when its two inputs are different.

Truth Table — Representation of the output logic levels of a logic circuit for every possible combination

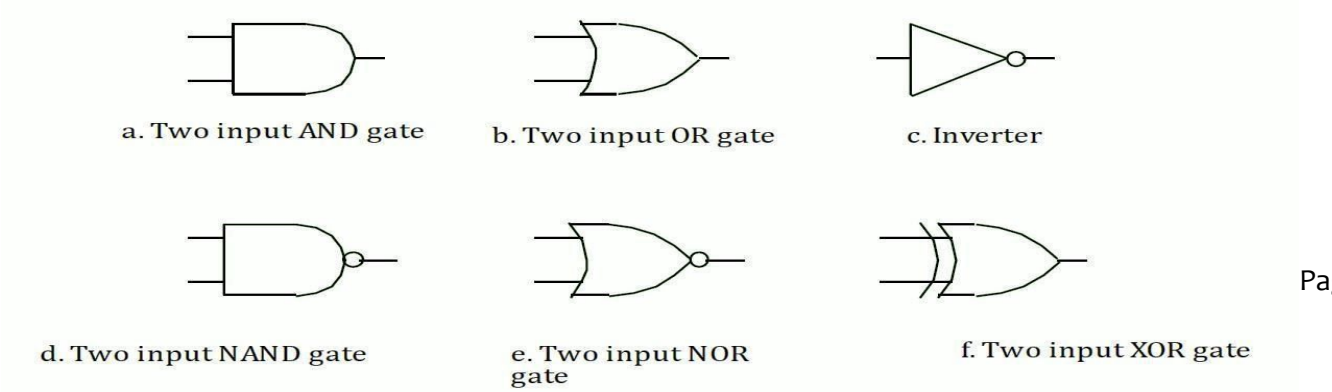


Fig.1 Symbols for digital logic gates

EQUIPMENT

A computer connected to internet.

SIMULATION USING TINKERCAD FROM AUTODESK

> **Tinkercad** is a free, online 3D design and 3D printing app for everyone. It helps you to prototype your electronic designs completely within the browser, before building them in real life.

Visit https://www.tinkercad.com/, create an account and log in. No installation required.

Watch the tutorials on how to get started on TinkerCAD at the links provided in the pre-lab.

> **Logisim** – already installed on machines in AK 317 and AK113. Also available for FREE at the following link: https://sourceforge.net/projects/circuit/files/latest/download.

Logisim is a logic simulator which permits circuits to be designed and simulated using a graphical user interface.

Watch the tutorials on how to get started on Logisim at the links provided in the pre-lab.

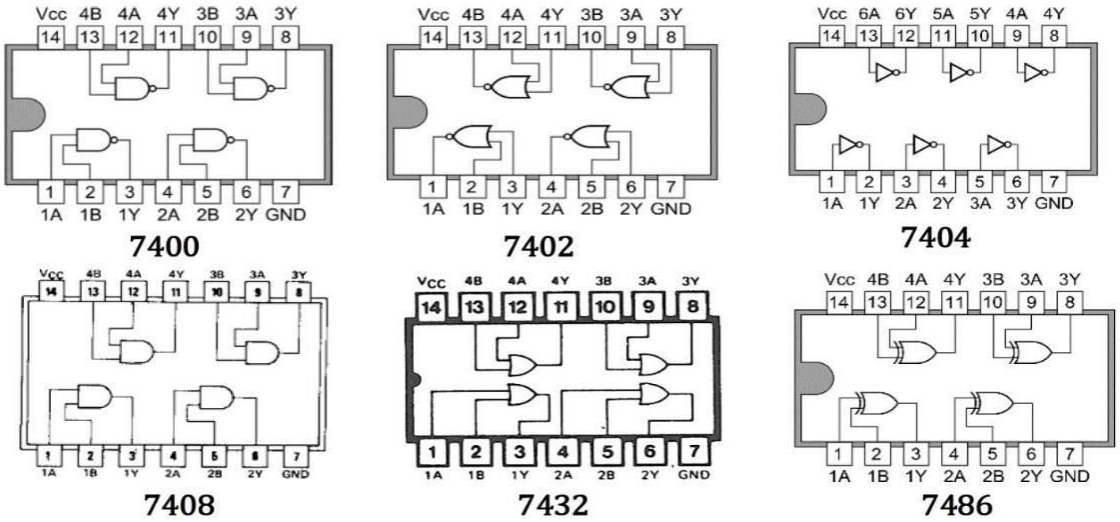
COMPONENTS

1) IC Type 7432 Quadruple 2-input OR gates
2) IC Type 7408 Quadruple 2-input AND gates
3) IC Type 7400 Quadruple 2-input NAND gates
4) IC Type 7402 Quadruple 2-input NOR gates
5) IC Type 7486 Quadruple 2-input XOR gates
6) IC Type 7404 Hex Inverters/NOT gate

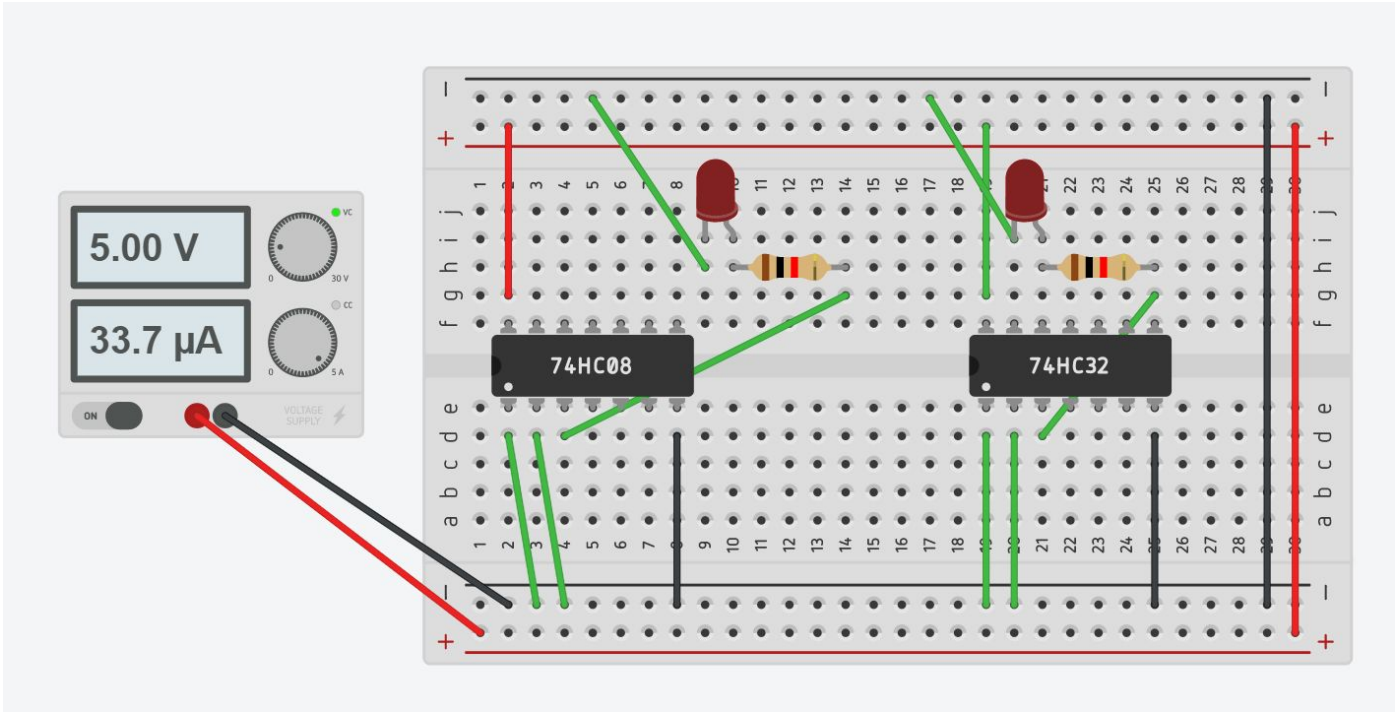
Note: See Fig. 2 for pin configurations.

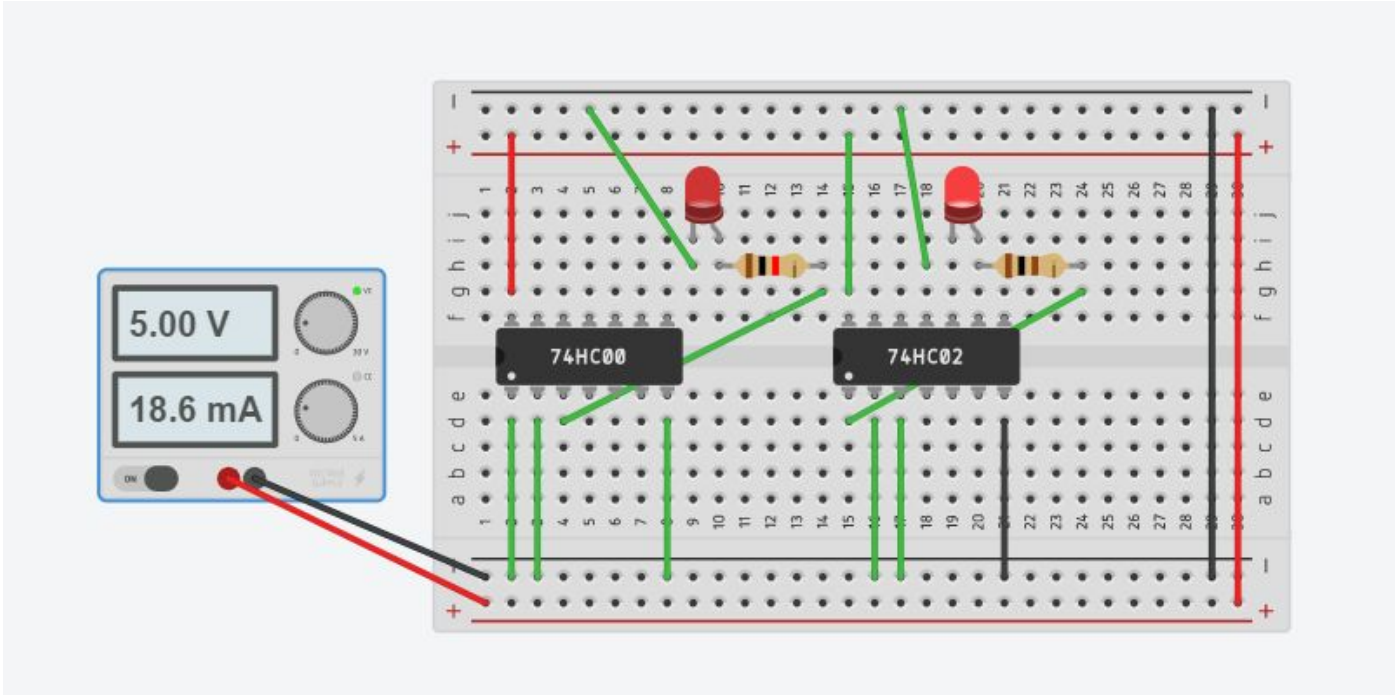
Part 1: Verifying Digital Logic using Tinkercad

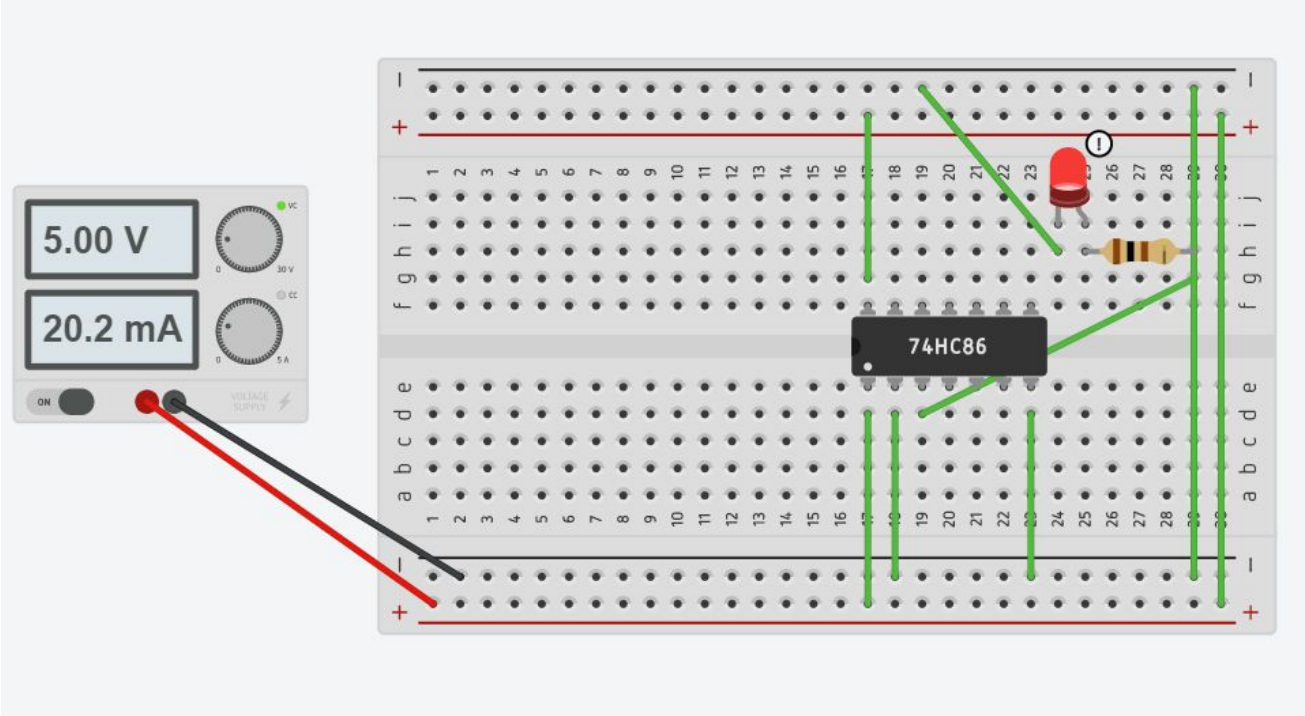
OR, AND, NAND, NOR, and XOR gates.



1. put pins for each gate. Pins 7 and 14 are ground (0 V) and V_{cc} (5 V).







2. [IC 7400] Connect input pins 1 and 2 using jumper wires to apply logic (0 GND, 1 5V). Connect output pin 3 to LED as shown in Fig 3 as an example for the NAND gate.

Remember: LED ON = Logic 1 (High) and LED OFF = Logic 0 (Low)

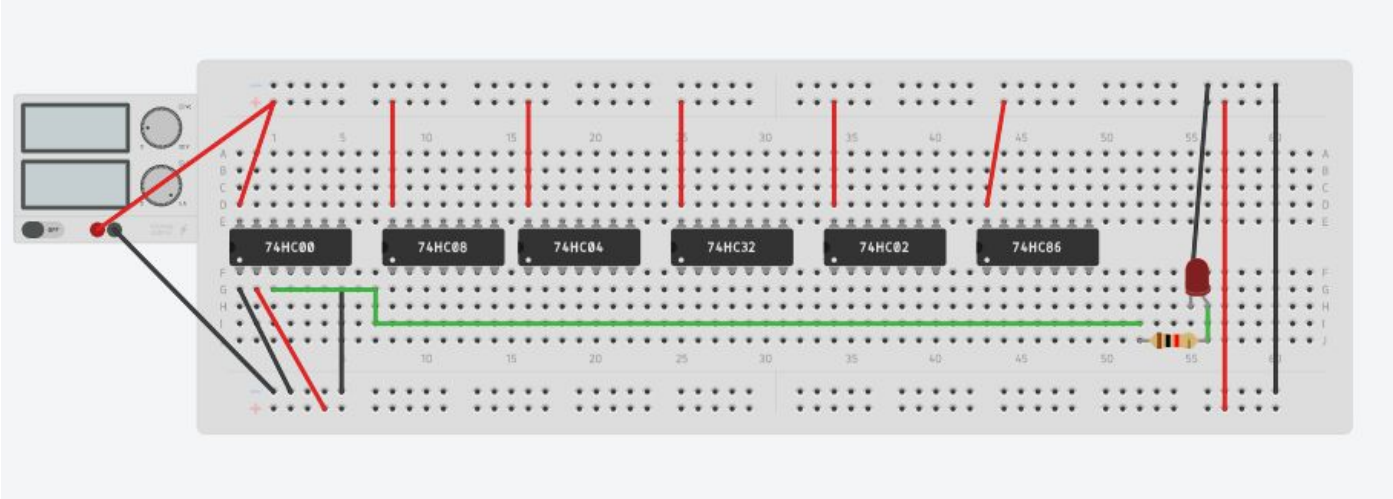


Fig. 3

3. Apply the logic levels 0 and 1 in the sequence shown in table 1. Record the output logic levels. Repeat the recordings for each digital logic gate.

Table 1 Output Response

Input Pins		**Output Pin**				
Pin 1	**Pin 2**	**Pin 3**				
		OR	**AND**	**NAND**	**NOR**	**XOR**
0	0	0	0	1	1	0
0	1	1	0	1	0	1
1	0	1	0	1	0	1
1	1	1	1	1	0	0

4. Use an inverter gate from **IC 7404** whose input pin is pin 1 and whose output pin is pin 2. Apply the logic levels 0 and 1 in the sequence shown in table 2. Record the output logic levels.

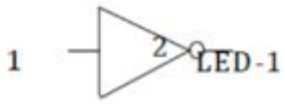
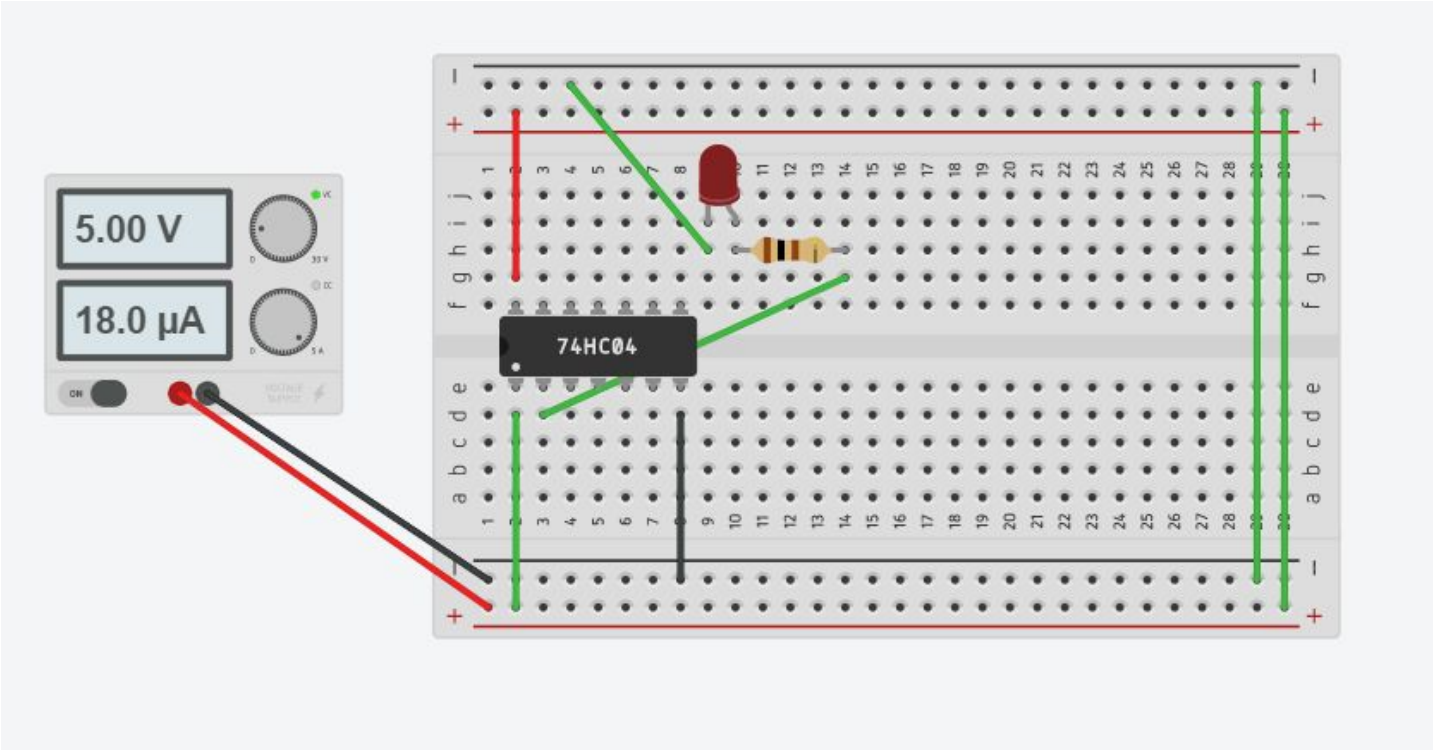
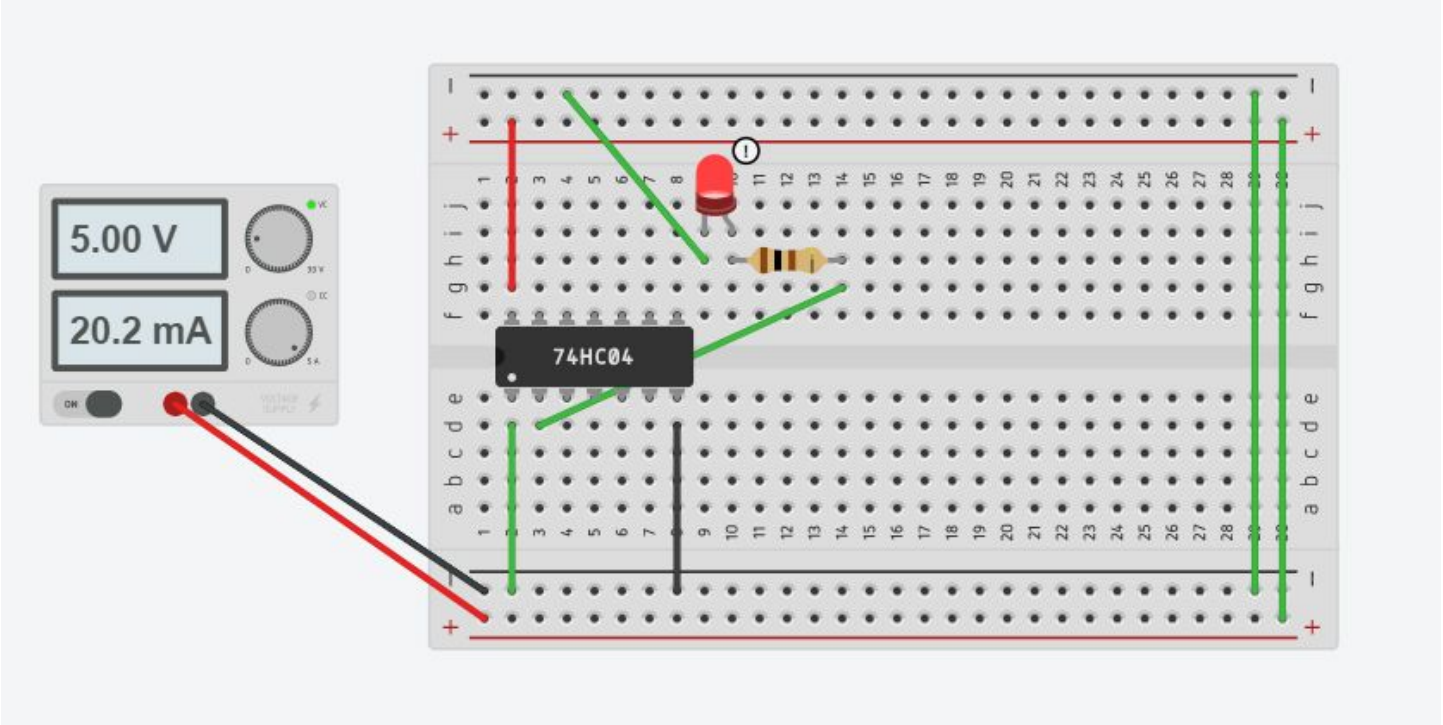


Fig.4 Inverter gate

Table 2.

Pin 1	Pin 2
0	1
1	0

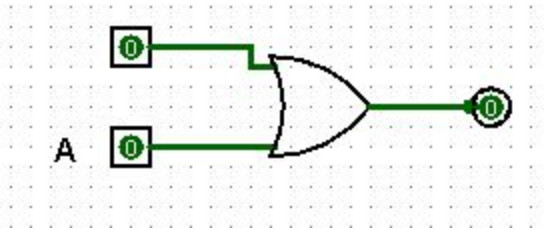




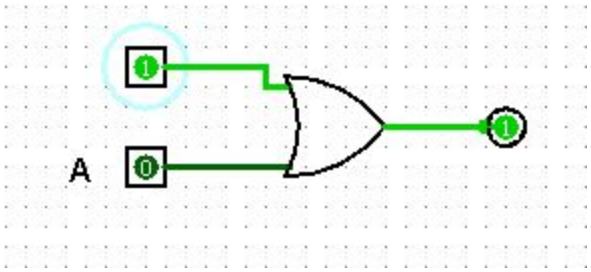
Part 2: Verify the Rules and regulations of Boolean Algebra using Logisim

1. Using digital logic gates, design a digital circuit to verify the following expressions:

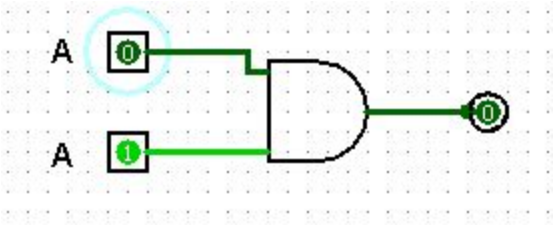
    1. A+0=A



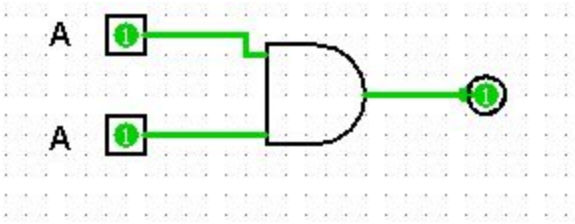
    2. A+1=1



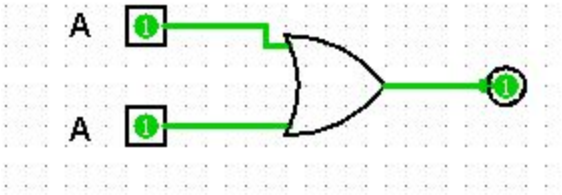
3. A.0=0



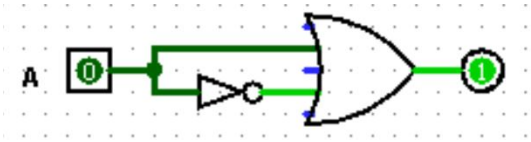
4. A.1=A



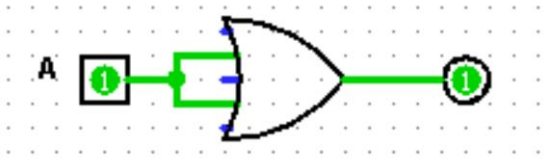
5. A+A=A

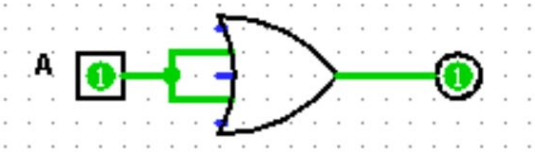


6. A+A' = 1

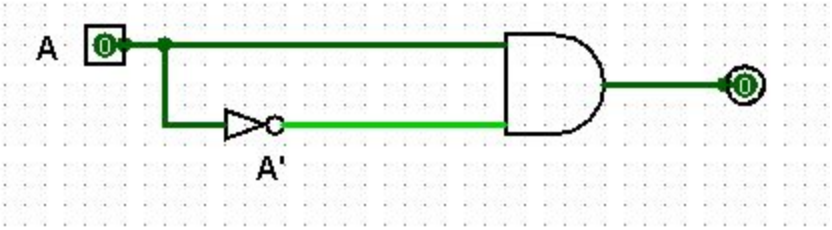


7. A.A=A

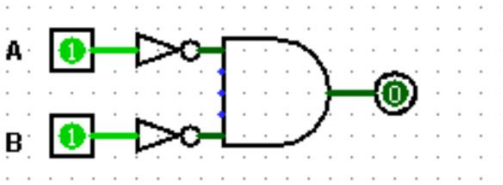


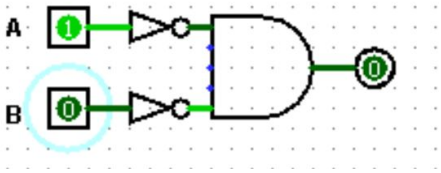


8. A.A' = 0

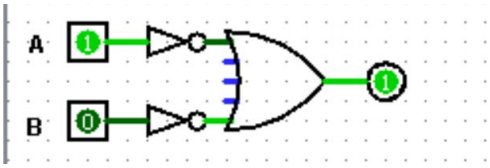


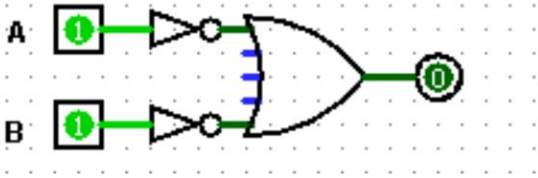
9. A'. B' = (A+B)'





10. A'+B' = (A.B)'





2. Build the following circuit using Logisim and verify the logic. Record the values in the table below:

D

E

F

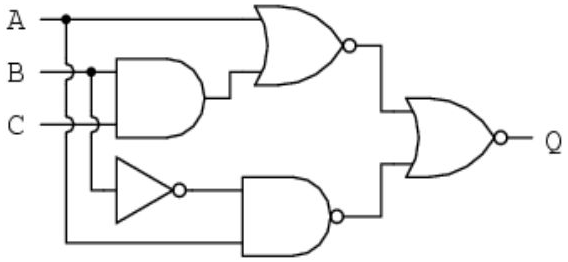


Fig. 5

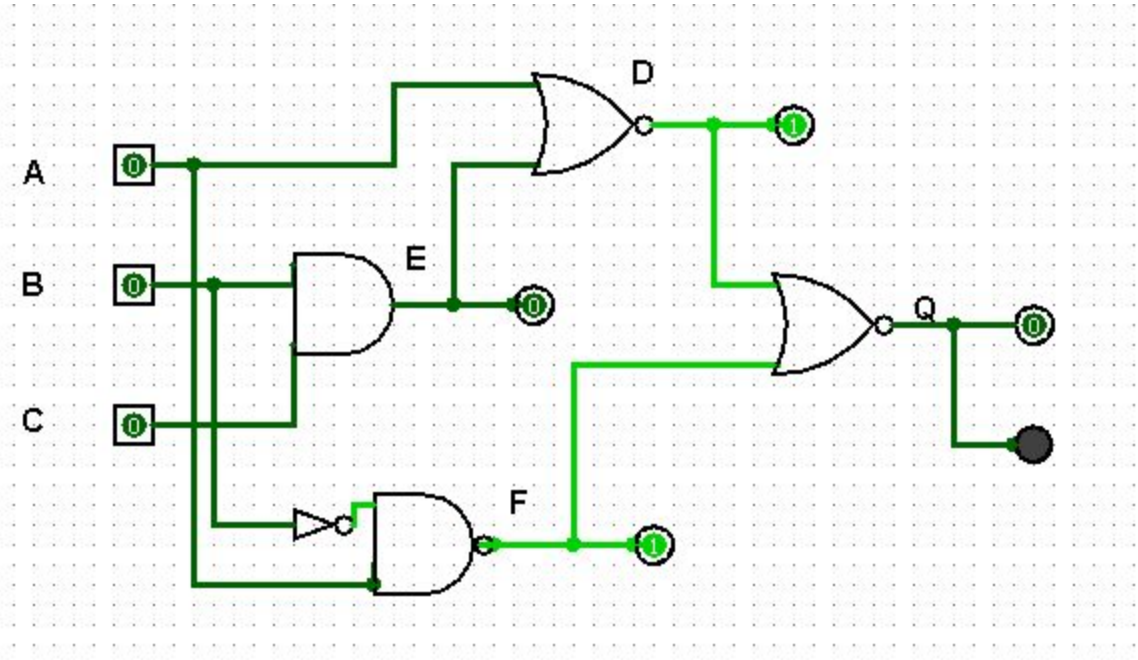


Table 3 Output Response of Circuit in Fig. 5

Inputs			Outputs			
A	B	C	D	E	F	Q
0	0	0	1	0	0	1
0	0	1	1	0	0	1
0	1	0	1	0	0	1
0	1	1	0	1	0	1
1	0	0	0	0	1	0
1	0	1	0	0	1	0
1	1	0	0	0	0	1
1	1	1	0	1	0	1

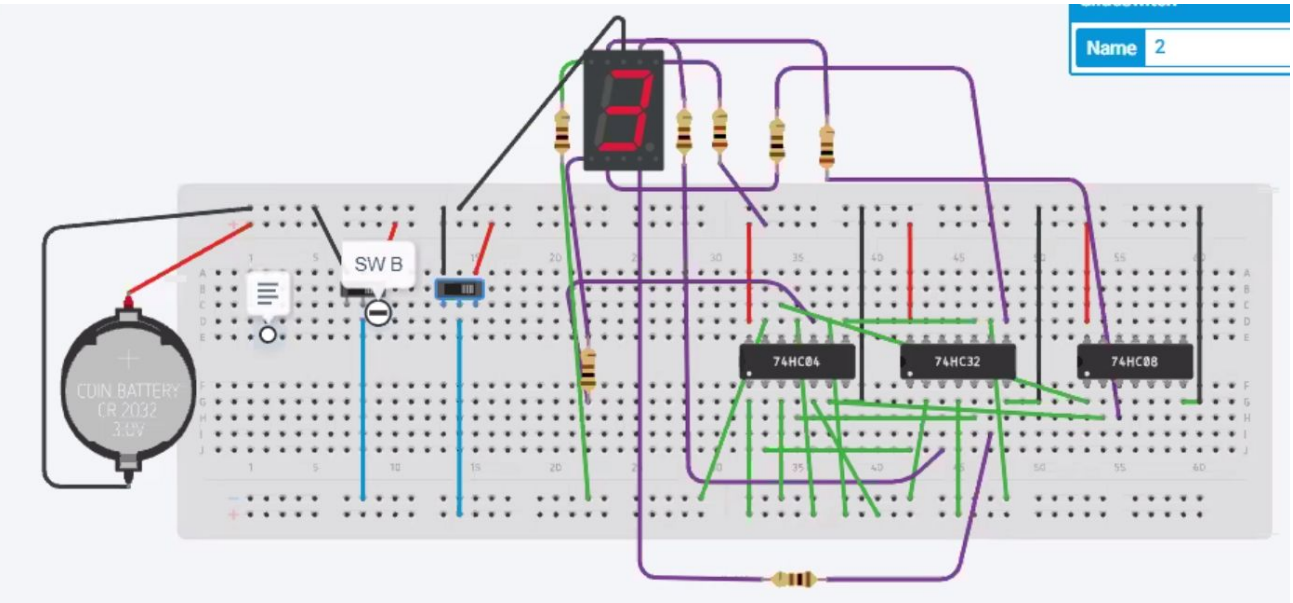
3. Verify the recorded values for Q in the table 3 by analyzing the circuit using Logisim and get the Boolean expression for Q.

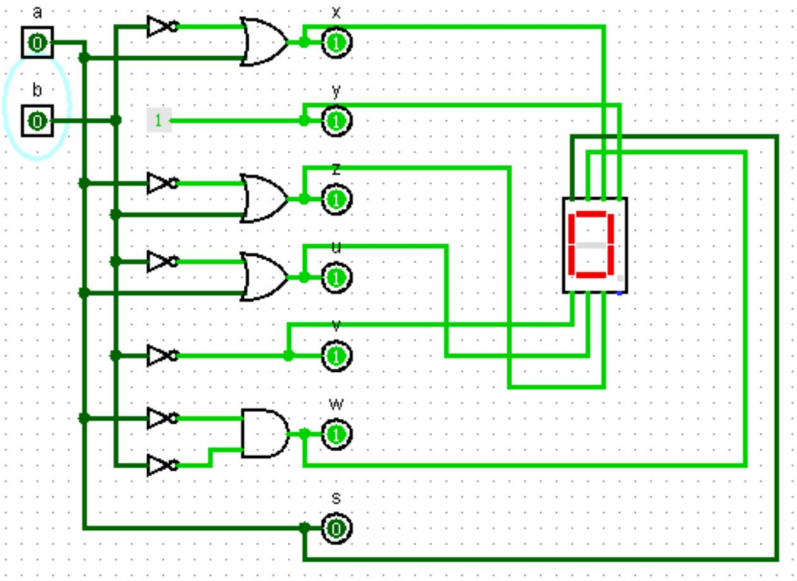
Q = ~a ~b + ~a ~c

Part 3: 2-bit input Seven Segment Display

Watch the video at the following link and repeat it.

https://youtu.be/C1omzzwVdhM





Note: Submission details are available on the sign-up sheet.

ECE 2029 INTRODUCTION TO DIGITAL CIRCUIT DESIGN

Lab 1: Build and Simulate Digital Logic Circuits using Logisim and TinkerCAD Sign-Off Sheet

Student 1:

Student 2:

COMPLETE ALL THE ASSIGNMENTS IN THE CHECKLIST BELOW IN ORDER TO GET FULL CREDIT!

Check List	
Assignments	**TA Sign-off**
Pre-Lab (MUST be completed before the start of the lab) • Watch Videos (see links at the bottom of the next page) and Read Lab Write-up • Complete the truth table • Download Logisim at: https://sourceforge.net/projects/circuit/files/latest/download	
Part 1: • Verifying Digital Logic using Tinkercad	
Part 2: • Verify the Rules and regulations of Boolean • Algebra using Logisim	
Part 3: • 2-bit input Seven Segment Display	

Submission Details: ***(see the example submission on CANVAS)***

- **Sign-off sheet, pre-lab work, and screenshots of circuit(s) from TinkerCAD/Logisim, all embedded in single .pdf document.**
- **Record 2-3 minute video showing that you've completed all the assignments in the checklist.**
- **Upload both .pdf and video files on CANVAS individually.**

Due Date: 04/14/2020 [Sec D04] 04/15/2020 [Sec D01, D02, D03]

*****Both Students MUST be present (Zoom) at Sign-off for any and all parts!!***

PRE-LAB

Complete the truth table for the Basic Digital Logic Gates below: Also drive the Boolean expression for each logic gate.

AND Gate

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

NAND Gate

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

XNOR Gate

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

XOR Gate

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

NOT Gate

A	Output
0	1
1	0