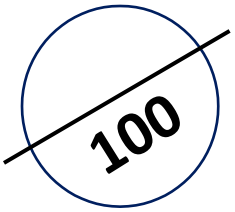
ECE 2029 Introduction to Digital Circuit Design

HOMEWORK # 5

Due: 2 pm on Friday, 05/08



Student Name: _____ Date:_____

ECE Box#:_____

Problems	Score	Instructor/TA's Comments
1)	/5	
2)	/20	
3)	/10	
4)	/20	
5)	/10	
6)	/15	
7)	/20	
Total	/100	

TA's/Instructor's Signature: _____ Date: _____

Important (TIPS)

1. **Show all the process work neatly, don't just jump to answer**. Partial credit may be given. **Box/highlight your answer**.
2. Read the problem carefully, don't assume. Look for the simple, straightforward way to solve the problem. Don't overdo yourself.
3. To make the grading easier, please return your homework on this problem sheet.
4. If you need to use an extra piece of paper, please staple it on and number your solutions just like below!

Please turn it into the ECE2029 box located at the ECE department office AK202 above the shelf just when you walk-in.

Problem 1 - 5 points total

a) My TV remote has a single MENU button that cycles between 6 different menus that make adjustments to the picture and sound. When I press the MENU button I go the color balance settings, then if I hit the button again I go to the brightness. I must then press the button again to get to get to the sound settings, etc. Finally after pressing the MENU button to enter language settings if I press MENU again I exit the menu mode. Is my TV remote's menu access system employing combinational or sequential logic? Explain.

b) A household alarm systems has 4 motion sensors (1 per room) and a single system enable or arming switch by the door. If the system is armed (enabled) and any of the motion sensors is activated (i.e. is logic 1) then the alarm sounds. If the system is not enabled then the alarm will not sound whether the motions sensors are activated or not. Is this home security system employing combinational or sequential logic? Explain.

Problem 2 - 20 points total

a) Draw the gate-level schematic diagram only for a simple S-R latch, for an S-R Latch with Enable (CE) and for a D-latch with Enable (CE) – 5 pts

S-R Latch

S-R Latch with Enable (CE)

D-Latch with Enable (C)

b) Also, fill in the function (or truth) tables for each – 15 pts

S-R Latch

S	R	Q	Q'

S-R Latch with Enable (CE)

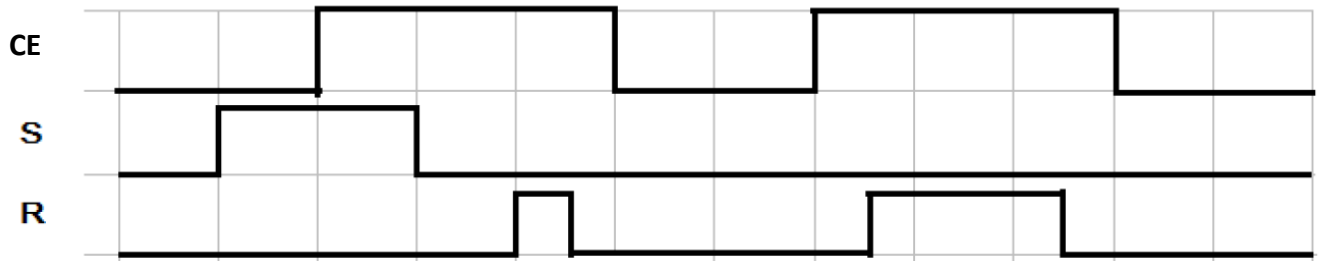
CE	S	R	Q	Q'

D-Latch with Enable (CE)

CE	D	Q	Q'

Problem 3- 10 points total

Trace the behavior of a level-sensitive SR latch for the input pattern in the figure below. Assume S1, R1, and Q are initially 0. Complete the timing diagram, assuming the logic gates have a tiny but non-zero delay.

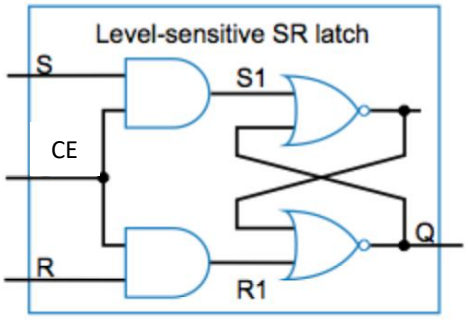


S1 ……

R1 ……...

Q ……

CE	S	R	S1	R1	Q	Qn (Q-NOT)



Problem 4 - 20 points total

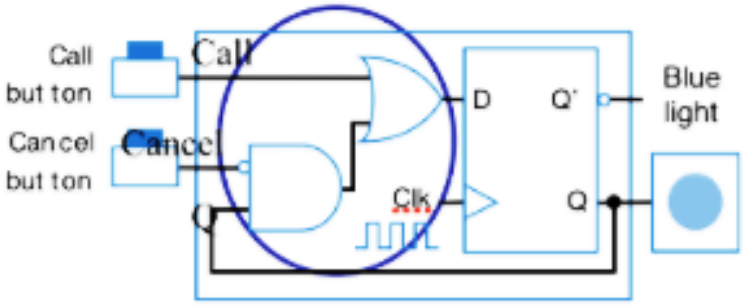
Analyze the Flight Attendant Call Button using D-Flip Flop as shown below, bottom right:
(Complete all steps. Assume that a button press is logic 1 and not pressed is logic 0)

1) Draw the circuit (including D FF as shown in figure) and identify Next State logic, State Memory and Output logic blocks – **5 pts**

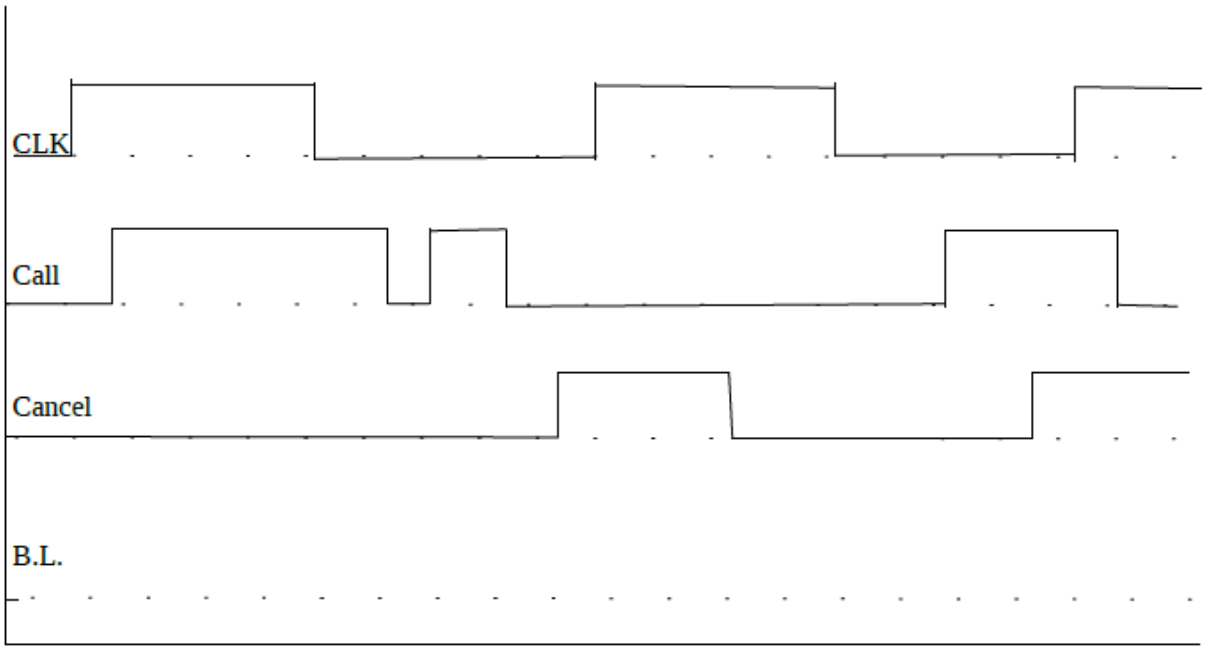
2) Write expressions for Next State and Output logic **– 5 pts**

3) Fill in the a transition table (shown below) – 5 pts

Call	Cancel	Q	D



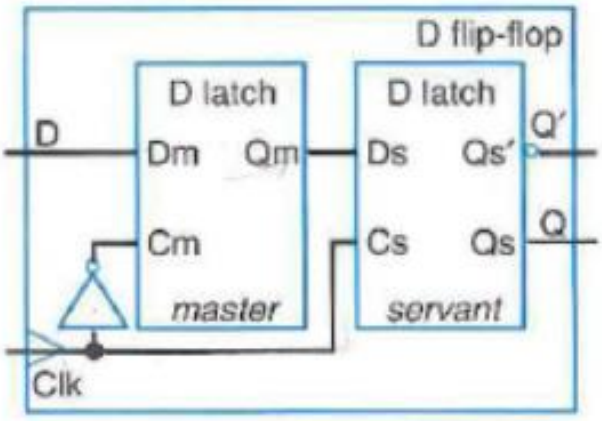
4) Assume some little kid is pressing the buttons. Finish timing diagram (below) ignoring propagation delays – 5 pts (Assume Blue Light, B.L. = 0 initially)

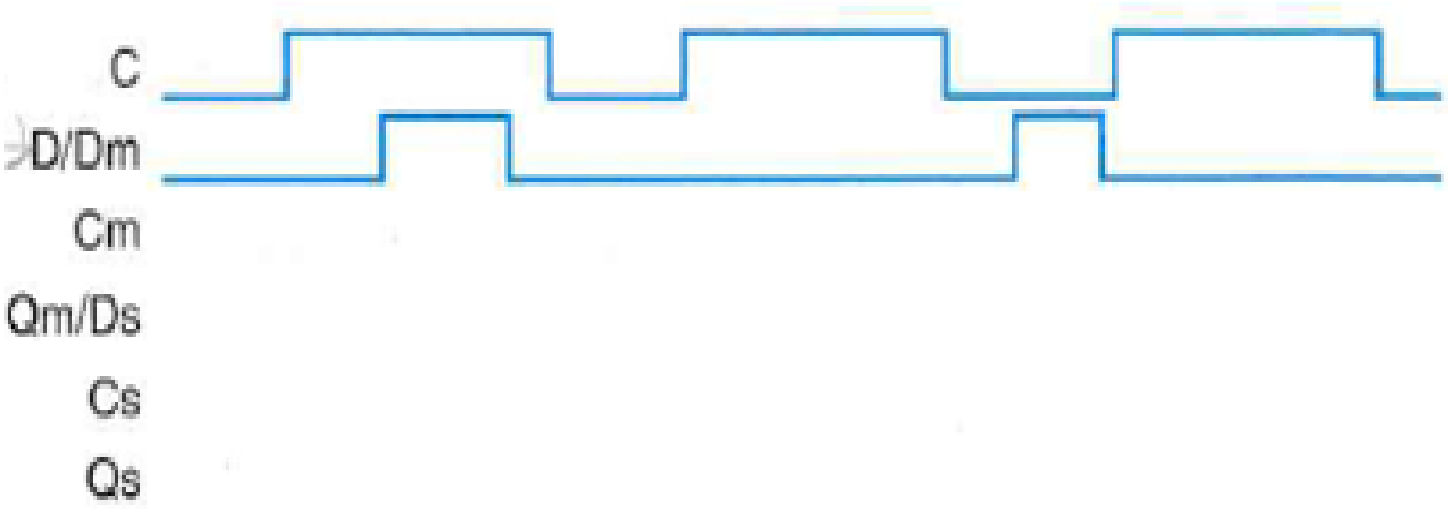


Problem 5 – 10 points total

Edge- Triggered D Flip-Flop using a Master Servant Design.

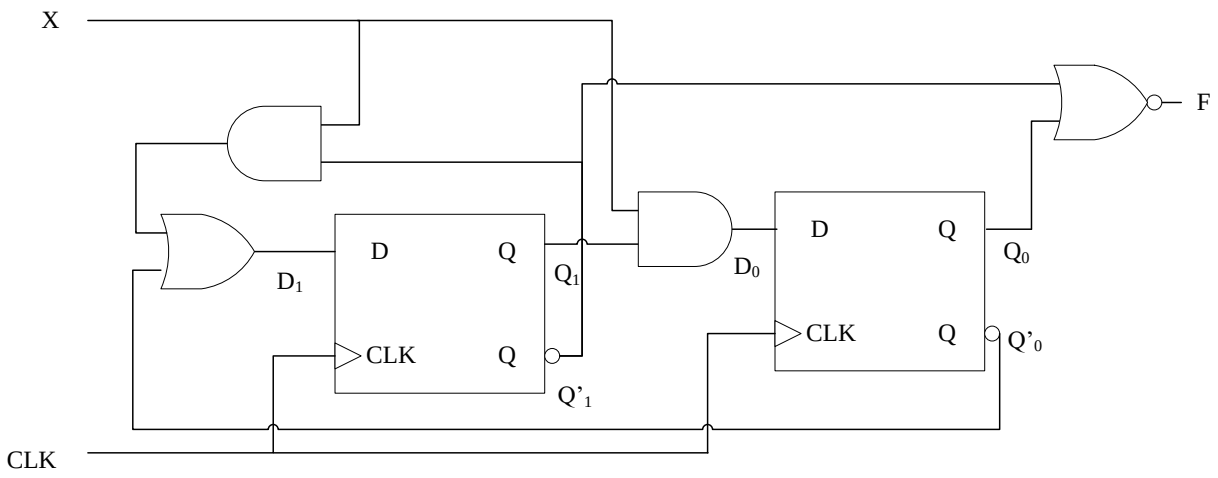
A D flip flop implementing an edge triggered bit storage block, internally using two D-latches as shown below, explain the working of the flip flop in master servant arrangement and complete the timing diagram (ignore any propagation delays).





Problem 6 -15 points total

For the sequential machine in the circuit diagram:



a) Determine Boolean expressions for next state logic and output logic from the circuit. That is, express D_1, D_0 and F as logic expressions in terms of Q_1, Q_0 and X.

b) Fill in the state table, given below.

Present State	Input	Next State	Output
Q_1 Q_0	X	Q_1^+ Q_0^+	F
0 0	0		
0 0	1		
0 1	0		
0 1	1		
1 0	0		
1 0	1		
1 1	0		
1 1	1		

c) Draw a state transition diagram for this sequential machine.

Problem 7 -20 points total

The following sequential circuit is a Pulse Distributor:

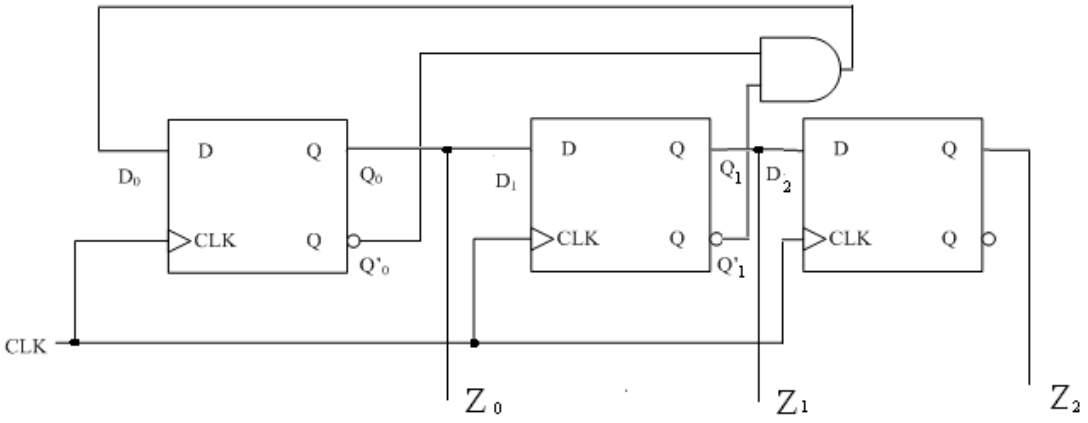


Figure 1

Notice: This sequential circuit does not have the input signal and the output Z is the present state of D flip-flop. The initial condition of output is set as 000.

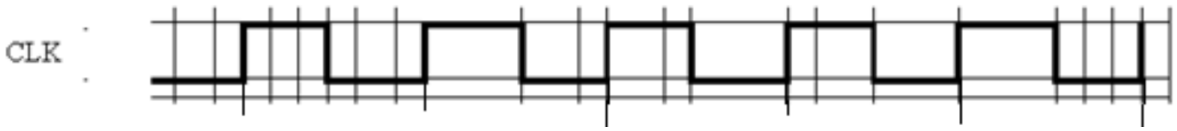
a) Determine Boolean expressions for next state logic and output logic from the circuit. That is, express D2, D1, D0 and Z2, Z1, Z0 as logic expressions in terms of Q2, Q1 and Q0. (do not write D logic expression in terms of Z since Z is the output)

b) Fill in the state table, given below.

Present State(Output)	Next State
$Q_2\ Q_1\ Q_0$	$Q_2^+\ \ Q_1^+\ \ Q_0^+$
0 0 0	
0 0 1	
0 1 0	
0 1 1	
1 0 0	
1 0 1	
1 1 0	
1 1 1	

c) Draw a state transition diagram for this sequential machine and timing diagram with CLK, Z_0, Z_1, and Z_2.

d) From the timing diagram, what the function of this sequential circuit.



Q0

Q1

Q2