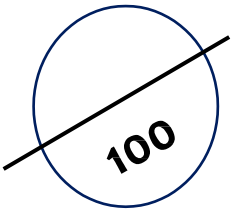
ECE 2029 Introduction to Digital Circuit Design

Exam # 2

Student Name: _____

Date:_____ ECE Box#:_____



Problems	Score	Instructor/TA's Comments
1)	/40	
2)	/40	
3)	/20	
Total	/100	

TA's/Instructor's Signature: _____

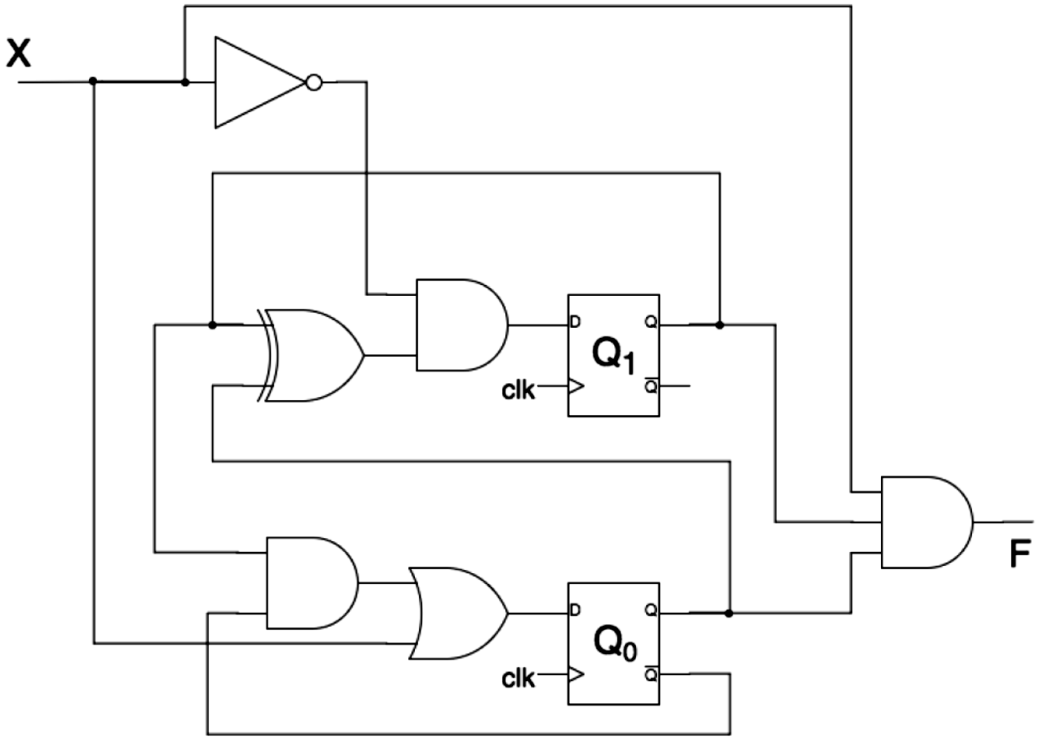
Date: _____

Important (TIPS)

1. This is an open book, open lecture notes test! Calculators are permitted, but no pre-stored formulas or network communication are allowed!
    a. Collaboration, and other outside assistance are not allowed!
    b. **Show all your work neatly**. Partial credit may be given. **Box/highlight your answer**.
    c. Read the problem carefully, don't assume. Look for the simple, straightforward way to solve the problem. Don't overdo yourself.
2. Don't get entangled in unnecessary work.
    a. As in real life, some problems may give you more information than you need. Don't assume that all information must be used! It's your job to decide what's relevant to the solution.
    b. Manage your time wisely! Before you begin working, look through all the problems and decide how best to complete as much of the exam as possible in the allotted time. The point value of each part is indicated in brackets.
3. Please turn you Camera on, if you don't have a webcam, use your cellphone to join the meeting.

Problem 1 – 40 points total

For the sequential machine shown:



a) Determine the Boolean expressions for next state logic and output logic from the circuit. That is, express Q_1^+, Q_0^+, and F as logic expressions in terms of Q_1, Q_0, and X.
(Do not write Q_1^+, Q_0^+ logic expressions in terms of F since F is the output)

(15 pts)

b) Fill in the state table, given below: (15 pts)

Present State	Input	Next State	Output

c) Draw a state transition diagram for this sequential machine. (10 pts)

Problem 2– 40 points total

Note: Problem 2 has two options. You have the choice to pick any of the option. Please do not attempt both of them. Use D-FF to implement the FSM.

OPTION 1: Design a finite state machine (FSM) that counts from zero to four and then goes back to zero. Such that the output Y will be 0 → 1 → 2 → 3 → 4 → 0 → 1 and so forth. This system is purely drive by the clock.

a) Draw a state transition diagram for this FSM. (5 pts)

b) Complete the state transition table with current states, next states, and output. Use "D" to denote any don't care states or output. (10 pts)

Present State	Next State	Output

c) Derive the logic expression for the input of each D Flip-Flop and output. (15 pts)

d) Draw the circuit diagram for the implementation of this circuit. (10 pts)

OPTION 2: Design a controller for a vending machine. It sells soda only and each cost 75 cents. The machine accepts quarter coins only and one quarter at a time. Once it receives 75 cents, it automatically dispenses a soda can and back to the initial reset state. You do not need to consider the changes or coin return scenarios.

a) Draw a state transition diagram for this vending machine controller. (5 pts)

b) List a state transition table with input, output, current states, and next states. (10 pts)

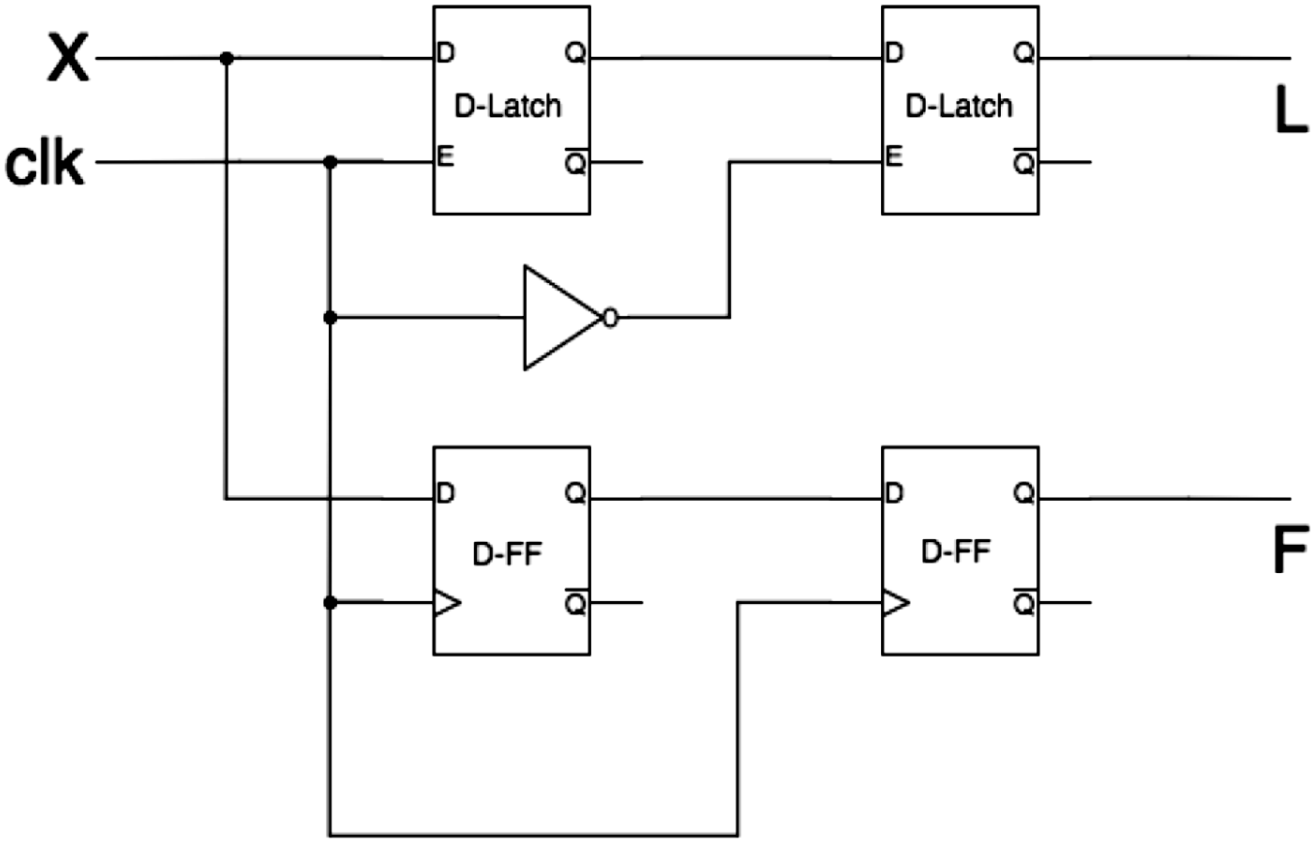
Present State	Input	Next State	Output

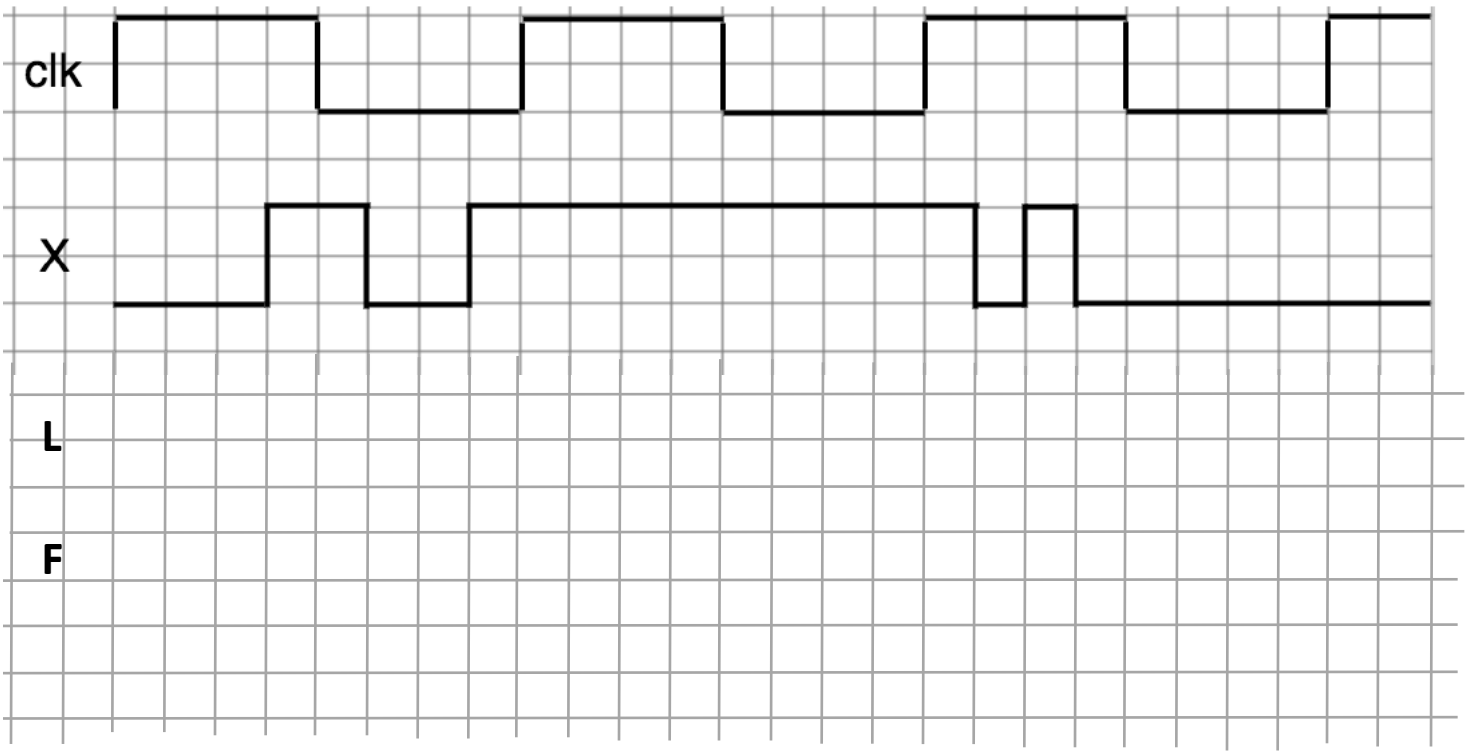
c) Derive the logic expression for the input of each D-Flip Flop and output Y. (15 pts)

d) Draw the circuit diagram for the implementation of this circuit. (10 pts)

Problem 3– 20 points total

a) Given the circuit diagram below, complete the waveform for L and F. Assume the D-Flip Flops are rising-edge triggered and initialized to 0. (15 pts)





b) FPGA implements combinational logic using look-up tables (LUTs). Assume the size of each LUT is only 16-bit that is equivalent to a memory space with 4-bit input and 1-bit output. Fill the LUT contents to implement logic function: (Hint: Use logic cells in K-Map to derive output) (5 pts)

Y = B'D' + A'BD + CD' + AD'

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	1	1	1
11	1	0	0	1
10	1	0	0	1

Fill the memory contents: