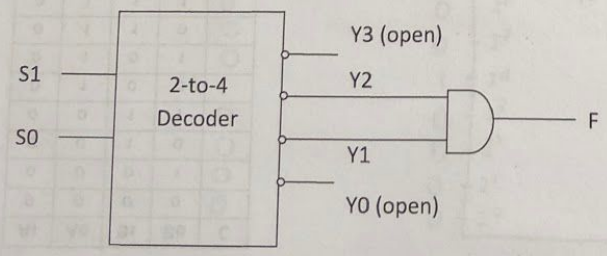
Homework #4

Problem 1 – 10 points total

The following truth table describes the logic function of **low-active** 2-to-4 decoder. Using the decoder and a 2-input AND gate, we can build a logic circuit function F. Note that Y0 and Y3 are not connected. Complete the truth table below and derive the logic expression of F (with S0 and S1 as input and F as output); then indicate clearly what type of logic gate this circuit functions.

S1	S0	Y3	Y2	Y1	Y0	F
0	0	1	1	1	0	1
0	1	1	1	0	1	0
1	0	1	0	1	1	0
1	1	0	1	1	1	1

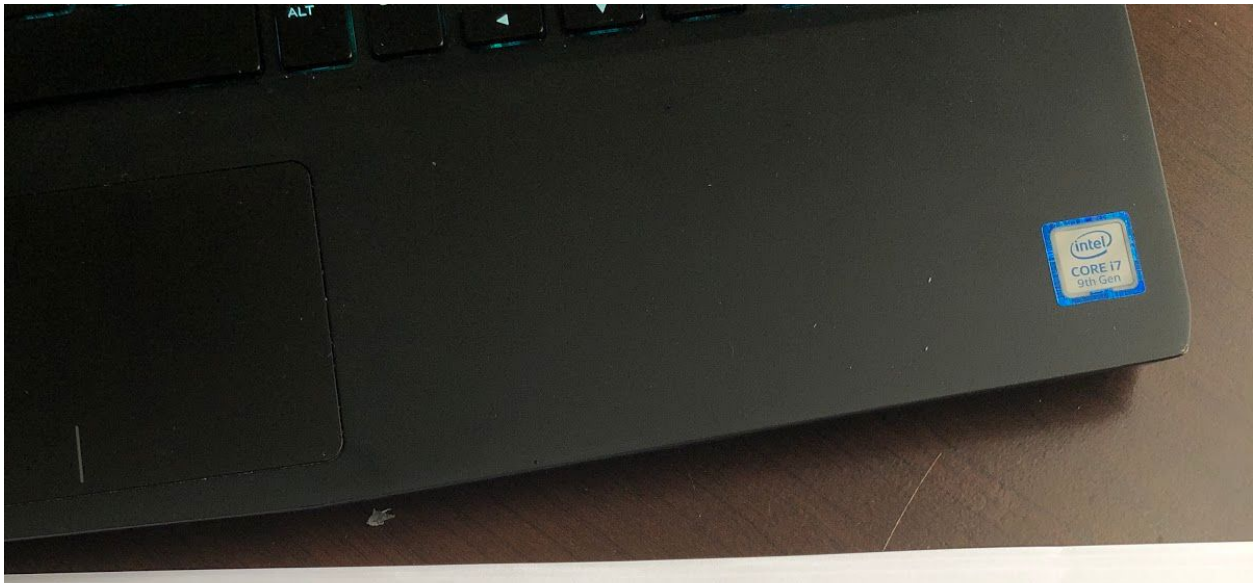
S_1	S_0	F
0	0	1
0	1	0
1	0	0
1	1	1



$F = \bar{A}\bar{B} + AB$

2 cont.

```
module Comparator (C, A0, A1, B0, A1);
    output C;
    input A1, A0, B1, B0;
    assign C = A1 & ~B1 & ~B0 | A1 & ~B1 | A1 & A0 & ~B0 ;
endmodule
```



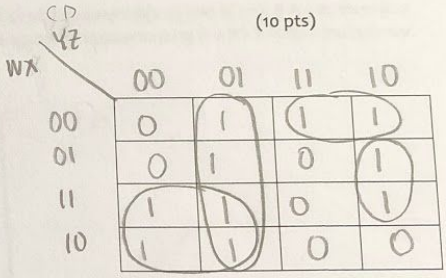
Problem 3 - 50 points total (10 pts)

For the function F described by the truth table:

W	X	Y	Z	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

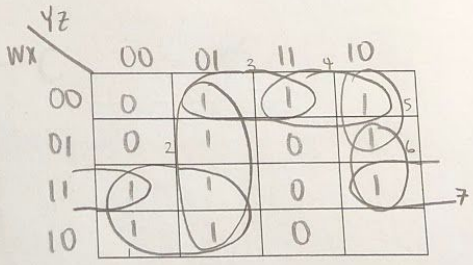
With hazards: F =

$Y'Z + WY' + W'X'Y + XYZ'$



Without hazards: F =

$Y'W + Y'Z + ZW'X' + YW'X' + YW' + YX + Z'WX$



a) Use a Karnaugh map (above) to produce simplified sum of products (SOP) expressions of F, one with and one without hazards?

What type of hazard is associated with sum of products expressions? Static-1 hazard

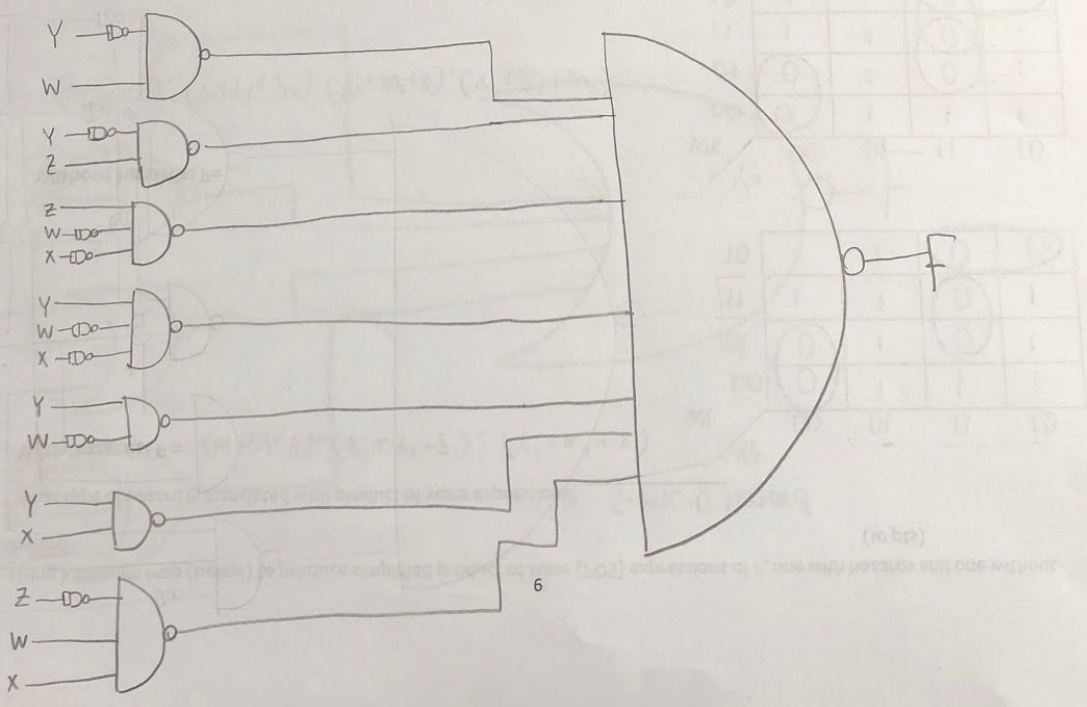
b) Draw the combinational logic circuit diagram for an implementation of sum of product logic expression without hazard using NAND gates ONLY. (15 pts)

$\bar{F} = \overline{Y'W + Y'Z + ZW'X' + YW'X' + YW' + YX + Z'WX}$

Demorgan's Law

$\bar{\bar{F}} = F = \overline{Y'W} \cdot \overline{Y'Z} \cdot \overline{ZW'X'} \cdot \overline{YW'X'} \cdot \overline{YW'} \cdot \overline{YX} \cdot \overline{Z'WX}$

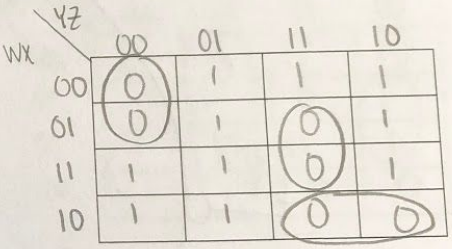
2-Level NAND Implementation



c) Using Karnaugh map (below) to produce simplified product of sums (POS) expressions of F, one with hazards and one without hazards. (10 pts)

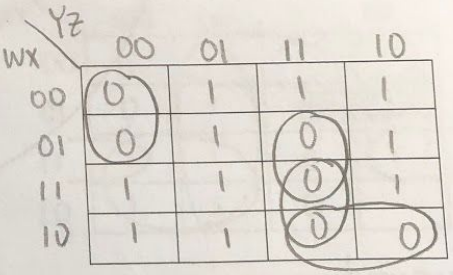
What type of hazard is associated with product of sums expressions? Static-0 hazard

With hazards: F = $(w + y + z).(x' + y' + z').(y' + w' + x)$



Without hazards: F=

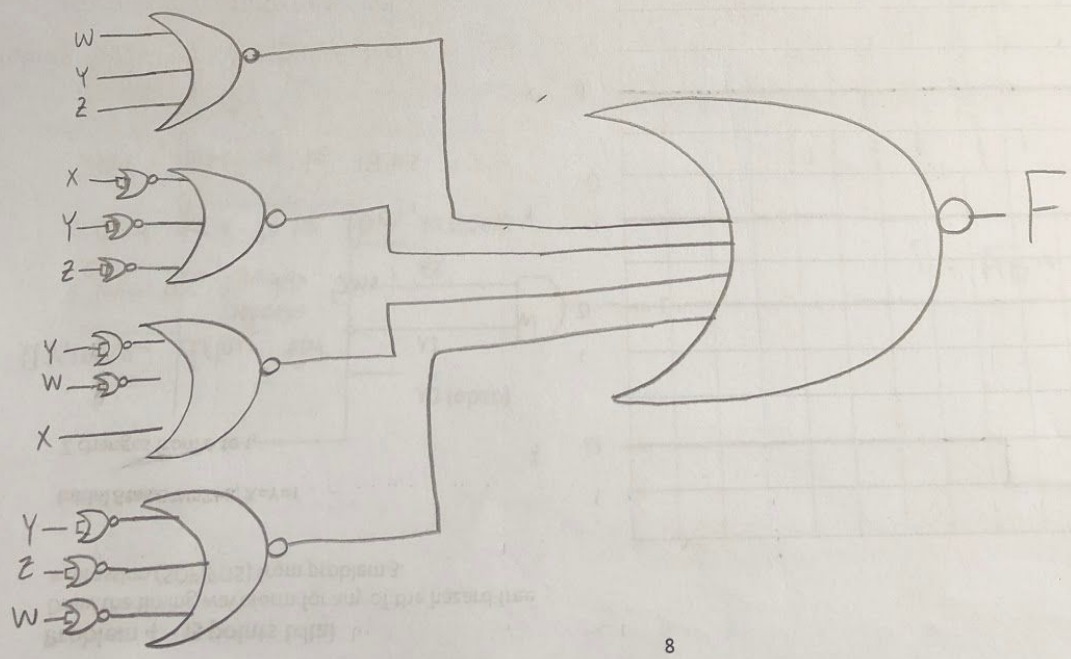
$(w+y+z).(x'+y'+z').(y'+w'+x).(y'+z'+w')$

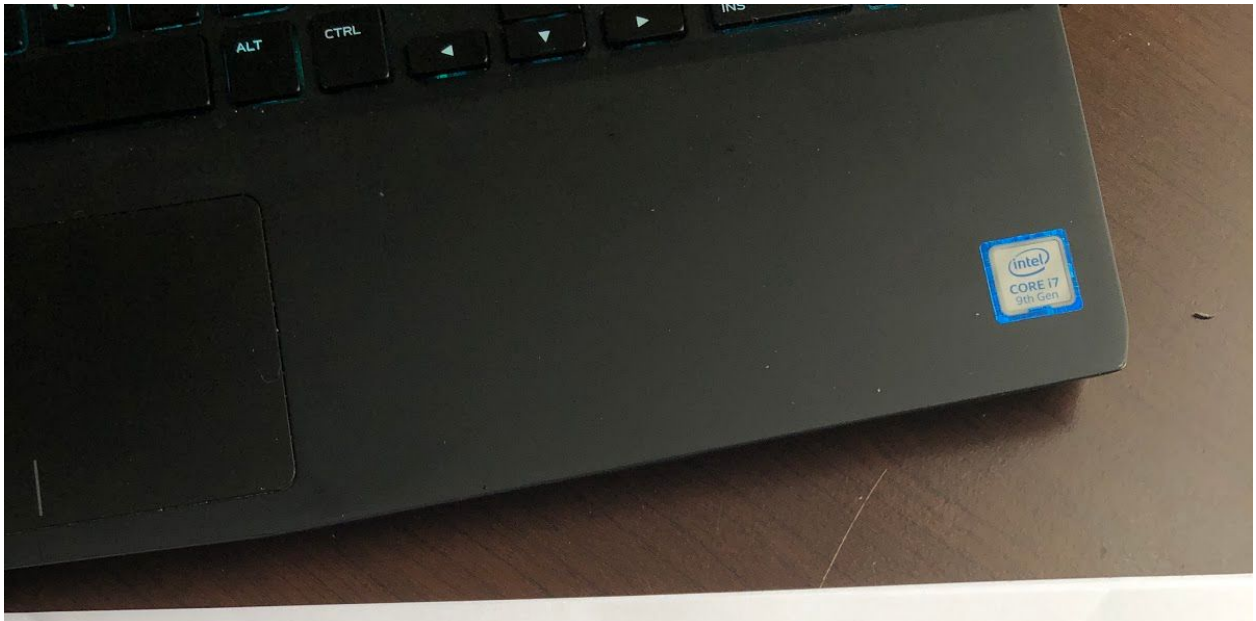


d) Draw the circuit diagram for an implementation of product of sum logic expression without hazard using NOR gates ONLY. (15 pts)

$$\overline{\overline{F}} = \overline{(W+Y+Z).(X'+Y'+Z').(Y'+W'+X).(Y'+Z'+W')}$$

$$\overline{\overline{F}} = \overline{\overline{(W+Y+Z)} + \overline{(X'+Y'+Z')} + \overline{(Y'+W'+X)} + \overline{(Y'+Z'+W')}}$$





SOP

$F = Y'W + Y'Z + ZW'X' + YW'X' + YW' + YX + Z'WX$

Problem 4 – 15 points total
Draw the timing waveform for any of the hazard-free expression (SOP/POS) from problem 3.

Initial State: W=Z=0; X=Y=1

Z changes from 0 to 1,

assume delay for
inverter to be 15ns,
and gate to be 18ns,
or gate to be 15ns

timing wave form completed using logic diagram not logic diagram from part 3b (using NAND gates)