

ECE 2029 Introduction to Digital Circuit Design

HOMEWORK # 4

Due: 2pm on Friday, 04/24

Student Name: _____ Date: _____

ECE Box#: _____

Problems	Score	Instructor/TA's Comments
1)	/10	
2)	/25	
3)	/50	
4)	/15	
Total	/100	

TA's/Instructor's Signature: _____ Date: _____

Important (TIPS)

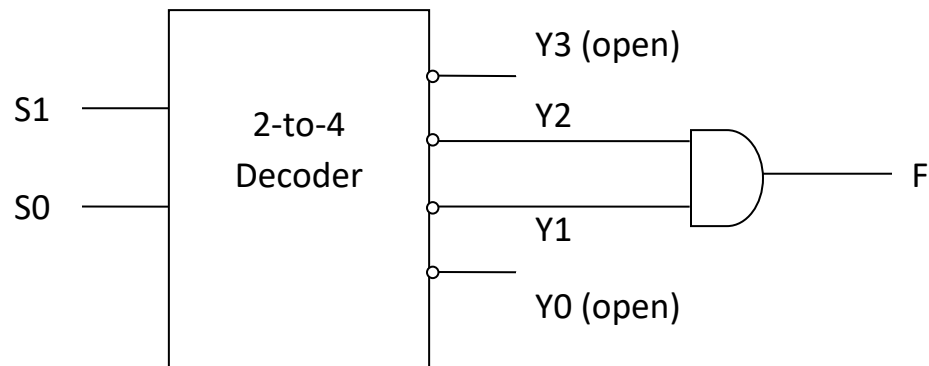
1. **Show all the process work neatly, don't just jump to answer.** Partial credit may be given.
Box/highlight your answer.
2. Read the problem carefully, don't assume. Look for the simple, straightforward way to solve the problem. Don't overdo yourself.
3. To make the grading easier, please return your homework on this problem sheet.
4. If you need to use an extra piece of paper, please staple it on and number your solutions just like below!

Please turn it into the ECE2029 box located at the ECE department office AK202 above the shelf just when you walk-in.

Problem 1 – 10 points total

The following truth table describes the logic function of **low-active** 2-to-4 decoder. Using the decoder and a 2-input AND gate, we can build a logic circuit function F. Note that Y₀ and Y₃ are not connected. Complete the truth table below and derive the logic expression of F (with S₀ and S₁ as input and F as output); then indicate clearly what type of logic gate this circuit functions.

S ₁	S ₀	Y ₃	Y ₂	Y ₁	Y ₀	F
0	0	1	1	1	0	
0	1					
1	0					
1	1					



Problem 2 – 25 points total

Design a 2-bit comparator using a 16-to-1 multiplexer. Given two standard unsigned binary numbers $A[1:0]$ and $B[1:0]$, if $A \leq B$, then $\{C = 0\}$, else $\{C = 1\}$. Write the truth table of the comparator. Then draw a circuit block diagram by implementing it with a 16-to-1 multiplexer. Write a Verilog code also to implement the comparator.

A1	A0	B1	B0	C
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Problem 3 - 50 points total

For the function F described by the truth table:

(10 pts)

W	X	Y	Z	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

With hazards: F =

Without hazards: F =

a) Use a Karnaugh map (above) to produce simplified sum of products (SOP) expressions of F, one with and one without hazards?

What type of hazard is associated with sum of products expressions? _____

- b)** Draw the combinational logic circuit diagram for an implementation of sum of product logic expression without hazard using NAND gates ONLY. (15 pts)

- c) Using Karnaugh map (below) to produce simplified product of sums (POS) expressions of F, one with hazards and one without hazards. (10 pts)

What type of hazard is associated with product of sums expressions? _____

With hazards: F =

Without hazards: F=

d) Draw the circuit diagram for an implementation of product of sum logic expression without hazard using NOR gates ONLY.

(15 pts)

Problem 4 – 15 points total

Draw the timing waveform for any of the hazard-free expression (SOP/POS) from problem 3.

Initial State: $W=Z=0$; $X=Y=1$

Z changes from 0 to 1,

