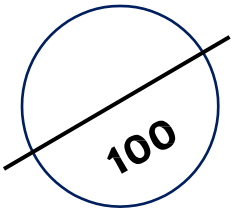
ECE 2029 Introduction to Digital Circuit Design

HOMEWORK # 3

Due: 2 pm on Friday, 04/17



Student Name: _____ Date:_____

ECE Box#:_____

Problems	Score	Instructor/TA's Comments
1)	/35	
2)	/20	
3)	/45	
Total	/100	

TA's/Instructor's Signature: _____ Date: _____

Important (TIPS)

1. **Show all the process work neatly, don't just jump to answer**. Partial credit may be given. **Box/highlight your answer**.
2. Read the problem carefully, don't assume. Look for the simple, straightforward way to solve the problem. Don't overdo yourself.
3. To make the grading easier, please return your homework on this problem sheet.
4. If you need to use an extra piece of paper, please staple it on and number your solutions just like below!

Problem 1 – 35 points total

We will design part of a set of logic circuits that tests numbers for divisibility for certain prime numbers as part of an information encryption system. The binary number A is represented by a four bit unsigned number: A = (a_3; a_2; a_1; a_0) where a_0 is the least significant bit, etc. The circuit you must design will have a single **output, F**, which must take on the value of **1** if A is divisible by 3 or 7 and zero otherwise, except when A = 0 (which is "technically" divisible by any number) for which case we want **F = 0**.

(a) Give the truth table for F as a function of a_3; a_2; a_1; a_0. (5 pts)

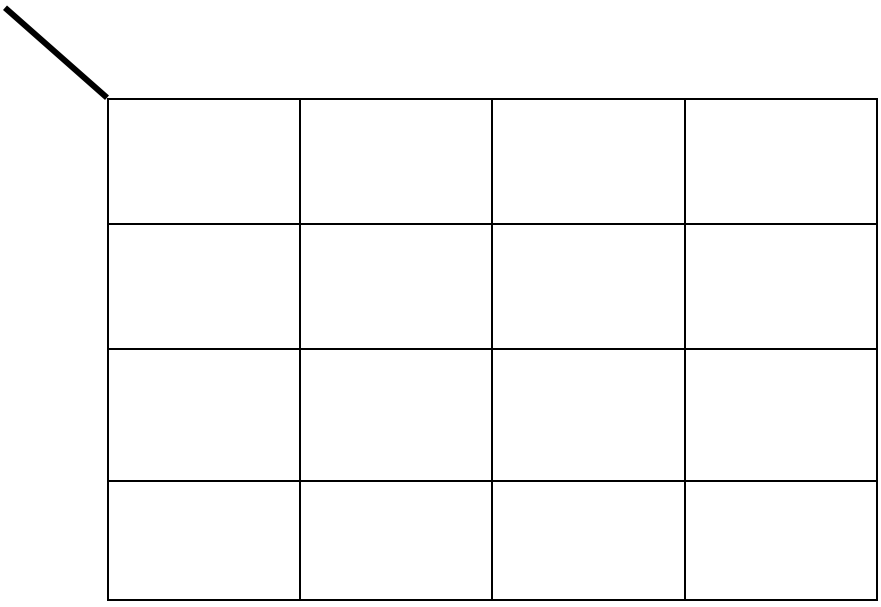
					F
0					
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

(b) Write out the canonical sum of Minterms expression for F. (5 pts)

F =

(c) Obtain a simplified expression for F using a Karnaugh Map. (5 pts)

Label essential prime implicants (EPI) with asterisk sign on the K-Map!



F =

(d) Draw the combinational logic circuit diagram that implements F. (5 pts)

(e) Write the Verilog code for the combinational logic circuit diagram that implements F. (5 pts)

(f) Draw the combinational logic circuit diagram that implements F using NAND Gates only. (10 pts)

Problem 2 - 20 points total

For each of the following truth tables, use a Karnaugh map to produce a **simplified sum of products expression.**

The X's in the tables indicate "don't cares". Be sure to show your Karnaugh map with clearly circled groups that correspond to your sum of products solution. Please draw your final Karnaugh maps, clearly labeled and the resulting simplified logic expressions next to them.

(a) Three Variable Map **(5 pts)**

X	Y	Z	A
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(b) Four Variable Map **(5 pts)**

W	X	Y	Z	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

F =

(c) Three Variable Map **(5 pts)**

X	Y	Z	C
0	0	0	0
0	0	1	1
0	1	0	X
0	1	1	1
1	0	0	0
1	0	1	X
1	1	0	0
1	**1**	**1**	**X**

C =

(d) Four Variable Map **(5 pts)**

W	X	Y	Z	D
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	X
0	1	1	0	1
0	1	1	1	X
1	0	0	0	1
1	0	0	1	X
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	X
1	1	1	1	0

D =

Problem 3 - 45 points total

For the function given:

$$F = (A + B + C) \cdot (A + B' + C) \cdot (A + B' + C') \cdot (A' + B' + C')$$

(a) Produce a truth table that expresses F as a function of A, B, and C. (5 pts)

Note: You can do this on Logisim also.

(b) Use a Karnaugh map to produce a simplified sum of products form. (Show both the Karnaugh map and Sum of Product expression.) (5 pts)

(c) Draw the circuit diagram of a NAND gate only implementation from your simplified sum of products (SOP) expression. (15 pts)

(d) Use a Karnaugh map to produce a simplified product of sums (POS) form.
(Show both the K- map and simplified expression.)

(5 pts)

(e) Draw the circuit diagram of a NOR gate only implementation from your simplified product of sums (POS) expression. **(15 pts)**