SRMIST

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

DELHI NCR CAMPUS, MODINAGAR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II YEAR / III SEMESTER

ANALOG AND DIGITAL ELECTRONICS LABORATORY

(18CSS201J)

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Register Number : RA1911003030265

Branch-Section :CSE-I

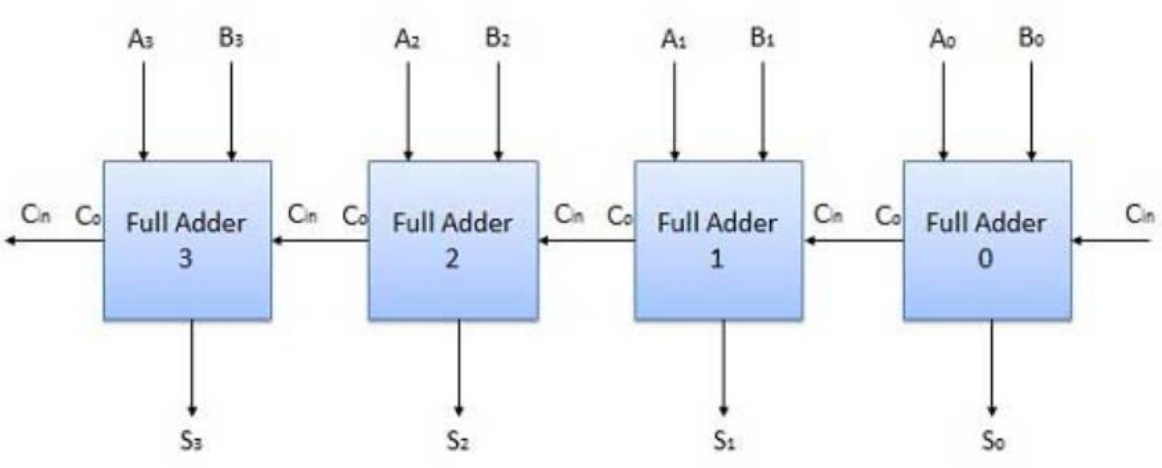
Year/Semester :2ND / 3RD

S. No.	EXPERIMENT NAME	EXPERIMENT DATE	SUBMISSION DATE
7	A)- Ripple Carry Adder by Full Adder by Half Adder by Exor Gate, B)- Full Subtractor by Half Subtractor by Exor Gate, C)- 8:1 MUX from gate level modeling . with bottom to top methodology.	23/09/2020	05/10/2020
8	Carry Look Ahead Adder by Data Flow Modeling. (a) - 4 BITS & b) - 6 BITS)	23/09/2020	05/10/2020

Experiment 7-

A)- Ripple Carry Adder by Full Adder by Half Adder by Exor Gate,
B)- Full Subtractor by Half Subtractor by Exor Gate,
C)- 8:1 MUX from gate level modeling .
with bottom to top methodology.

A) - AIM- Ripple Carry Adder by Full Adder by Half Adder by Exor Gate.
SOFTWARE USED: MODELSIM (by verilog)
LOGIC DIAGRAM:



CODE:

```
module exor_1 (a, b, y);
    input a,b;
    output y;

    wire w1,w2,w3,w4;

    not n_1 (w1,a);
    not n_2 (w2,b);

    and a_1 (w3,a,w2);
    and a_2 (w4,b,w1);

    or o_1 (y, w3,w4);

  endmodule
```

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```
module ripple_adder_4bit(output [3:0] Sum,output Cout,input [3:0] A,B,input Cin);
 wire c1,c2,c3;
 full_adder FA1(Sum[0],c1,A[0],B[0],Cin),
    FA2(Sum[1],c2,A[1],B[1],c1),
    FA3(Sum[2],c3,A[2],B[2],c2),
    FA4(Sum[3],Cout,A[3],B[3],c3);
endmodule

module full_adder( output S,Cout,input A,B,Cin);
 wire s1,c1,c2;
 half_adder HA1(s1,c1,A,B);
 half_adder HA2(S,c2,s1,Cin);
 or OG1(Cout,c1,c2);

endmodule


module half_adder(
    output S,C,
  input A,B
    );
 xor(S,A,B);
 and(C,A,B);

endmodule
```

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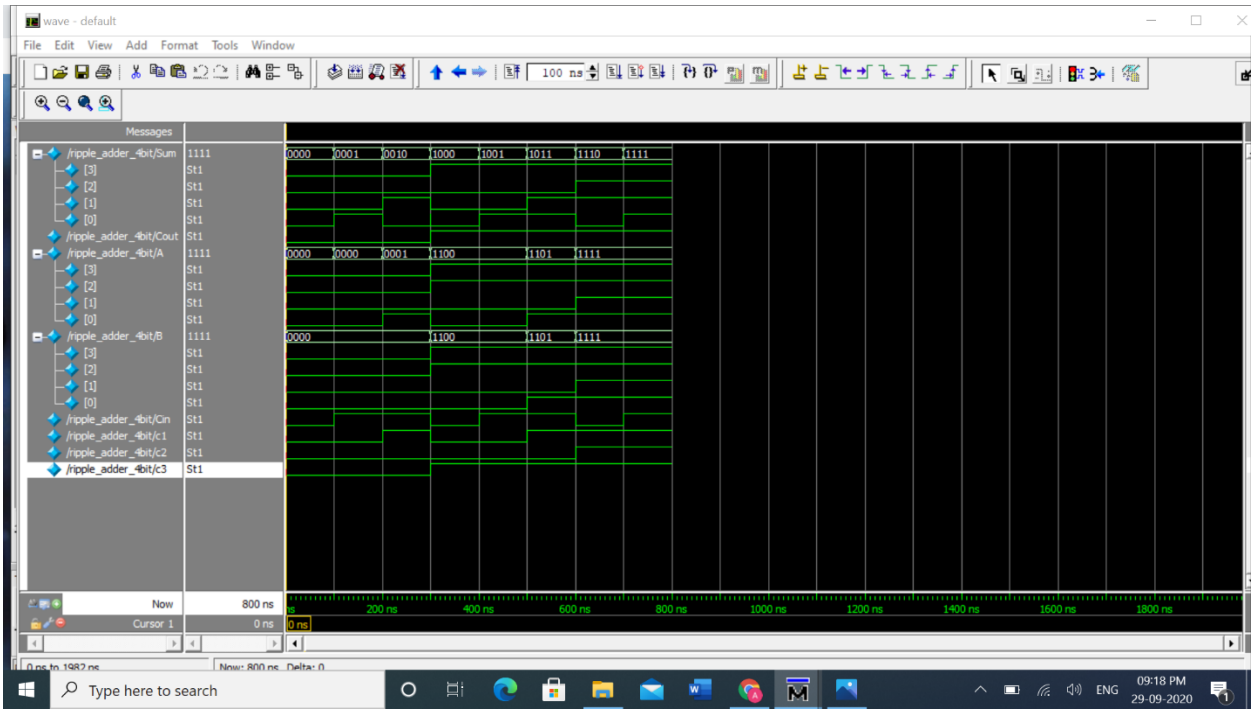
WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/ripple_adder_4bit/Sum
/ripple_adder_4bit/Cout
/ripple_adder_4bit/A
/ripple_adder_4bit/B
/ripple_adder_4bit/Cin
/ripple_adder_4bit/c1
/ripple_adder_4bit/c2
/ripple_adder_4bit/c3
Now
800 ns
Cursor 1
0 ns
200 ns
400 ns
600 ns
800 ns
1000 ns
1200 ns
1400 ns
1600 ns
1800 ns
Type here to search
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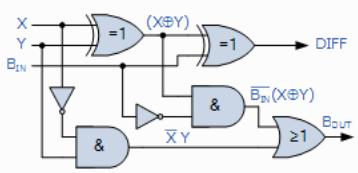
29-09-2020

B) - AIM: Full Subtractor by Half Subtractor by Exor Gate.

SOFTWARE USED: MODELSIM (by verilog).

LOGIC DIAGRAM:

Symbol



Truth Table

B-in	Y	X	Diff.	B-out
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

CODE:

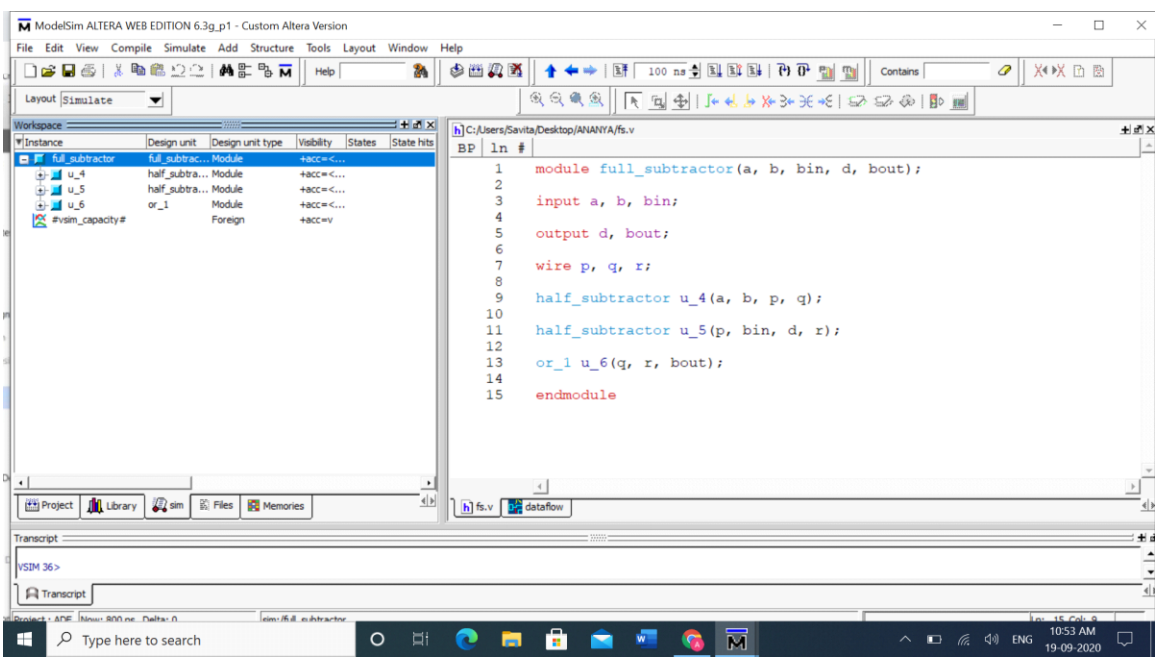
a) EXOR GATE:

```
BP | ln #
module exor_1 (a, b, y);
    input a,b;
    output y;

    wire w1,w2,w3,w4;

    not n_1 (w1,a);
    not n_2 (w2,b);

    and a_1 (w3,a,w2);
    and a_2 (w4,b,w1);

    or o_1 (y, w3,w4);

 endmodule
```

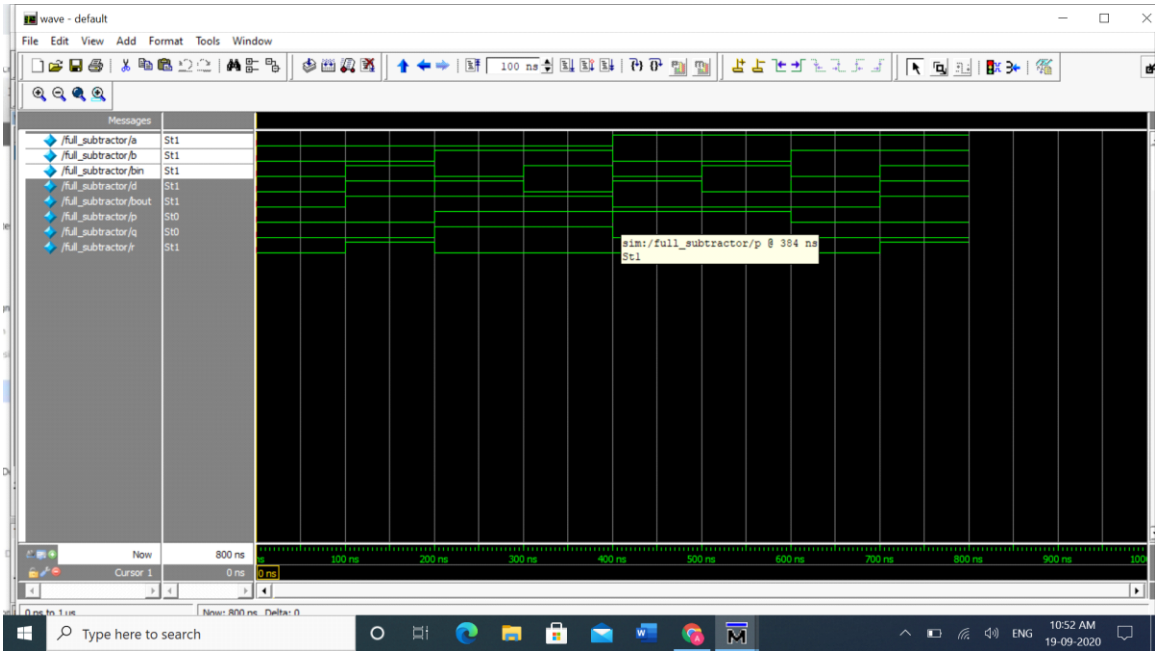
b) HALF SUBTRACTOR:

```
module half_subtractor(a, b, difference, borrow);

input a, b;

output difference, borrow;

wire x;

exor_1 u_1(a, b, difference);

and_1 u_2(x, b, borrow);

not_1 u_3(a, x);

endmodule
```

FULL SUBTRACTOR:



WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/full_subtractor/a St1
/full_subtractor/b St1
/full_subtractor/bin St1
/full_subtractor/d St1
/full_subtractor/bout St1
/full_subtractor/p St0
/full_subtractor/q St0
/full_subtractor/r St1
sim:/full_subtractor/p @ 384 ns
St1
Now 800 ns
Cursor 1 0 ns
100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns
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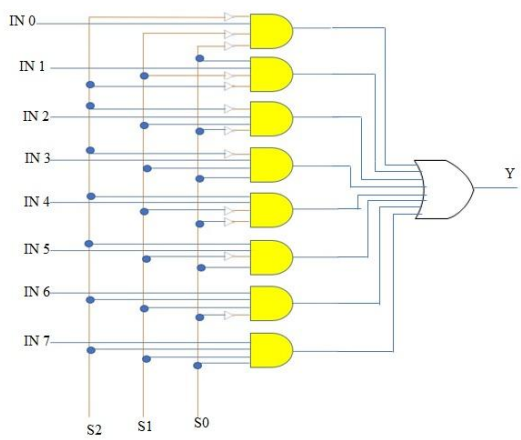
C)- AIM: Design 8:1 MUX from gate level modeling.

SOFTWARE USED: MODELSIM (by verilog).

LOGIC DIAGRAM:



CODE:

C:/Users/Savita/Desktop/ANANYA/8-1 mul.v

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```
module mux_8_1 (in, s, y);

    input [0:7] in;
    input [0:2] s;
    output y;

    wire [0:10] w;

    not n_0 (w[0], s[0]);
    not n_1 (w[1], s[1]);
    not n_2 (w[2], s[2]);

    and a_0 (w[3], in[0], w[0], w[1], w[2]);
    and a_1 (w[4], in[1], s[0], w[1], w[2]);
    and a_2 (w[5], in[2], s[1], w[0], w[2]);
    and a_3 (w[6], in[3], s[0], s[1], w[2]);
    and a_4 (w[7], in[4], s[2], w[0], w[1]);
    and a_5 (w[8], in[5], s[0], s[2], w[1]);
    and a_6 (w[9], in[6], s[1], s[2], w[0]);
    and a_7 (w[10], in[7], s[0], s[1], s[2]);

    or o_1 (y, w[3], w[4], w[5], w[6], w[7], w[8], w[9], w[10]);

endmodule
```

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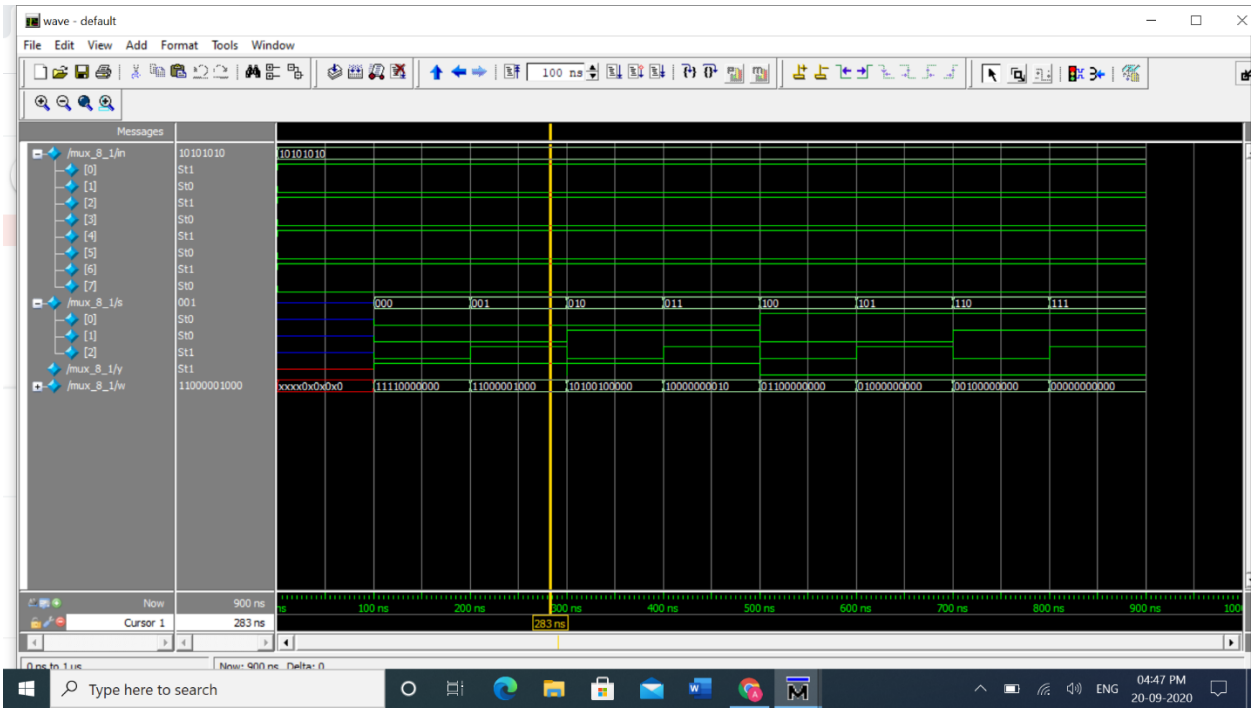
WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/mux_8_1/in
/mux_8_1/s
/mux_8_1/y
/mux_8_1/w
Now
Cursor 1
900 ns
283 ns
Type here to search
ENG
04:47 PM
20-09-2020

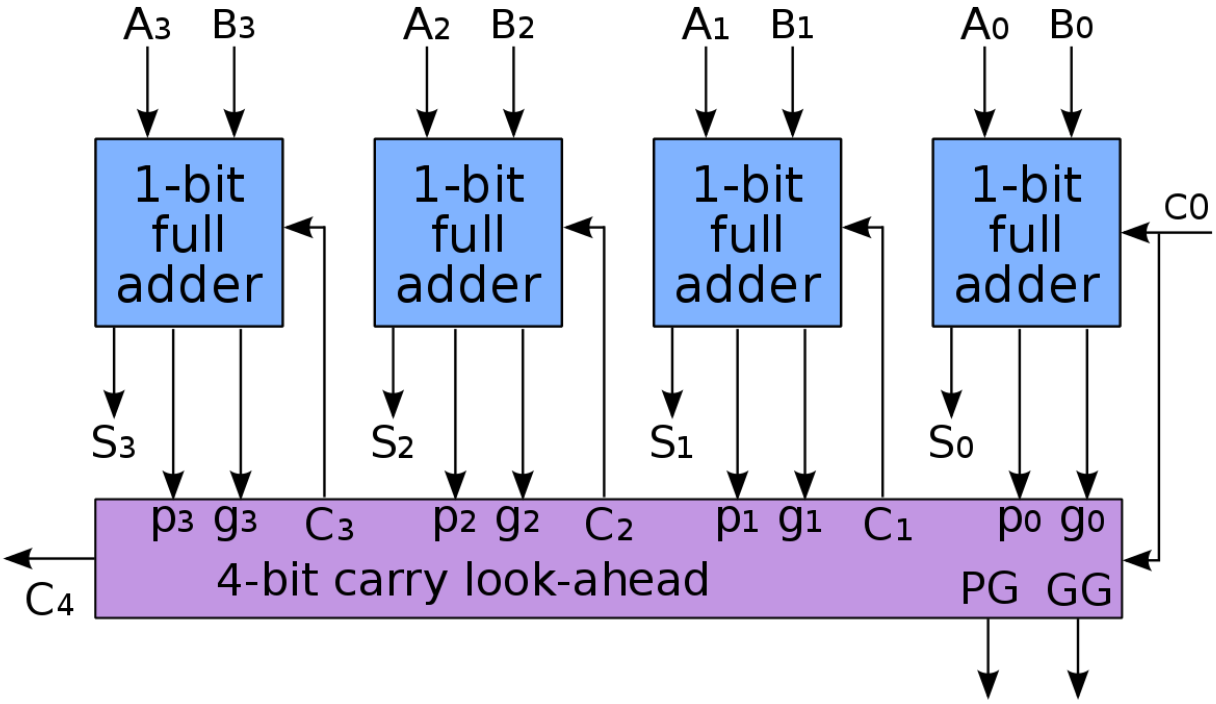
EXPERIMENT 8-

Carry Look Ahead Adder (a)-4 bits & b)-6 bits) by Data Flow Modeling.

a)- AIM: Design 4-BIT Carry Look Ahead Adder by Data Flow Modeling.

SOFTWARE USED: MODELSIM (by verilog).

LOGIC DIAGRAM:



CODE:

C:/Users/Savita/Desktop/ANANYA/cla-4bit.v

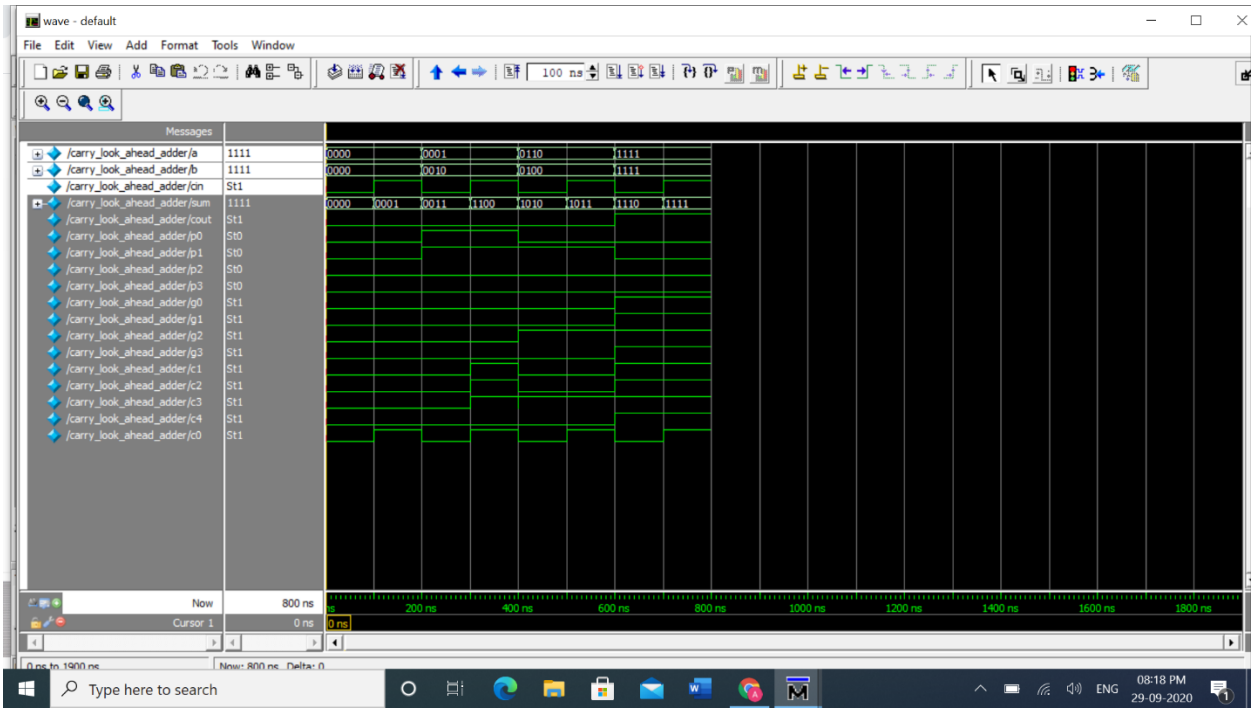
```
module carry_look_ahead_adder (a,b,cin,sum,cout);

input[3:0] a,b;
input cin;
output [3:0] sum;
output cout;

wire p0,p1,p2,p3,g0,g1,g2,g3,c1,c2,c3,c4;

assign p0=(a[0]^b[0]),
p1=(a[1]^b[1]),
p2=(a[2]^b[2]),
p3=(a[3]^b[3]);
assign g0=(a[0]&b[0]),
g1=(a[1]&b[1]),
g2=(a[2]&b[2]),
g3=(a[3]&b[3]);
assign c0=cin,
c1=g0|(p0&cin),
c2=g1|(p1&g0)|(p1&p0&cin),
c3=g2|(p2&g1)|(p2&p1&g0)|(p1&p1&p0&cin),
c4=g3|(p3&g2)|(p3&p2&g1)|(p3&p2&p1&g0)|(p3&p2&p1&p0&cin);
assign sum[0]=p0^c0,
sum[1]=p1^c1,
sum[2]=p2^c2,
sum[3]=p3^c3;
assign cout=c4;
endmodule
```

WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/carry_look_ahead_adder/a 1111
/carry_look_ahead_adder/b 1111
/carry_look_ahead_adder/cin St1
/carry_look_ahead_adder/sum 1111
/carry_look_ahead_adder/cout St1
/carry_look_ahead_adder/p0 St0
/carry_look_ahead_adder/p1 St0
/carry_look_ahead_adder/p2 St0
/carry_look_ahead_adder/p3 St0
/carry_look_ahead_adder/g0 St1
/carry_look_ahead_adder/g1 St1
/carry_look_ahead_adder/g2 St1
/carry_look_ahead_adder/g3 St1
/carry_look_ahead_adder/c1 St1
/carry_look_ahead_adder/c2 St1
/carry_look_ahead_adder/c3 St1
/carry_look_ahead_adder/c4 St1
/carry_look_ahead_adder/c0 St1
Now 800 ns
Cursor 1 0 ns
Type here to search
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29-09-2020

b)- AIM: Design 6-BITS Carry Look Ahead Adder by Data Flow Modeling.

SOFTWARE USED: MODELSIM (by verilog).

CODE:

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```
module carry_look_ahead_adder_6bit (a,b,cin,s,cout);

input[5:0] a,b;
input cin;

output [5:0] s;
output cout;

wire [5:1] c;
wire [5:0] g,p;

assign g[0]=(a[0]&&b[0]);
assign g[1]=(a[1]&&b[1]);
assign g[2]=(a[2]&&b[2]);
assign g[3]=(a[3]&&b[3]);
assign g[4]=(a[4]&&b[4]);
assign g[5]=(a[5]&&b[5]);

assign p[0]=(a[0]^b[0]);
assign p[1]=(a[1]^b[1]);
assign p[2]=(a[2]^b[2]);
assign p[3]=(a[3]^b[3]);
assign p[4]=(a[4]^b[4]);
assign p[5]=(a[5]^b[5]);

assign c[1]=g[0]||(p[0]&&cin);
assign c[2]=g[1]||(p[1]&&g[0])||(p[1]&&p[0]&&cin);
assign c[3]=g[2]||(p[2]&&g[1])||(p[2]&&p[1]&&g[0])||(p[2]&&p[1]&&p[0]&&cin);
assign c[4]=g[3]||(p[3]&&g[2])||(p[3]&&p[2]&&g[1])||(p[3]&&p[2]&&p[1]&&g[0])||(p[3]&&p[2]&&p[1]&&p[0]&&cin);
assign c[5]=g[4]||(p[4]&&g[3])||(p[4]&&p[3]&&g[2])||(p[4]&&p[3]&&p[2]&&g[1])||(p[4]&&p[3]&&p[2]&&p[1]&&g[0])
```

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C:/Users/Savita/Desktop/ANANYA/cla-6bit 1.v *

```
assign g[3]=(a[3]&&b[3]);
assign g[4]=(a[4]&&b[4]);
assign g[5]=(a[5]&&b[5]);

assign p[0]=(a[0]^b[0]);
assign p[1]=(a[1]^b[1]);
assign p[2]=(a[2]^b[2]);
assign p[3]=(a[3]^b[3]);
assign p[4]=(a[4]^b[4]);
assign p[5]=(a[5]^b[5]);

assign c[1]=g[0]||(p[0]&&cin);
assign c[2]=g[1]||(p[1]&&g[0])||(p[1]&&p[0]&&cin);
assign c[3]=g[2]||(p[2]&&g[1])||(p[2]&&p[1]&&g[0])||(p[2]&&p[1]&&p[0]&&cin);
assign c[4]=g[3]||(p[3]&&g[2])||(p[3]&&p[2]&&g[1])||(p[3]&&p[2]&&p[1]&&g[0])||(p[3]&&p[2]&&p[1]&&p[0]&&cin);
assign c[5]=g[4]||(p[4]&&g[3])||(p[4]&&p[3]&&g[2])||(p[4]&&p[3]&&p[2]&&g[1])||(p[4]&&p[3]&&p[2]&&p[1]&&g[0])
||(p[4]&&p[3]&&p[2]&&p[1]&&p[0]&&cin) ;
assign cout=g[5]||(p[5]&&g[4])||(p[5]&&p[4]&&g[3])||(p[5]&&p[4]&&p[3]&&g[2])||(p[5]&&p[4]&&p[3]&&p[2]&&g[1])
||(p[5]&&p[4]&&p[3]&&p[2]&&p[1]&&g[0])||(p[5]&&p[4]&&p[3]&&p[2]&&p[1]&&p[0]&&cin);

assign s[0]=p[0]^cin;
assign s[1]=p[1]^c[1];
assign s[2]=p[2]^c[2];
assign s[3]=p[3]^c[3];
assign s[4]=p[4]^c[4];
assign s[5]=p[5]^c[5];

endmodule
```

WAVEFORM: