SRMIST

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

DELHI NCR CAMPUS, MODINAGAR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II YEAR / III SEMESTER

ANALOG AND DIGITAL ELECTRONICS LABORATORY

(18CSS201J)

Name of the candidate : ANANYA GUPTA

Register Number : RA1911003030265

Branch-Section :CSE-I

Year/Semester :2ND / 3RD

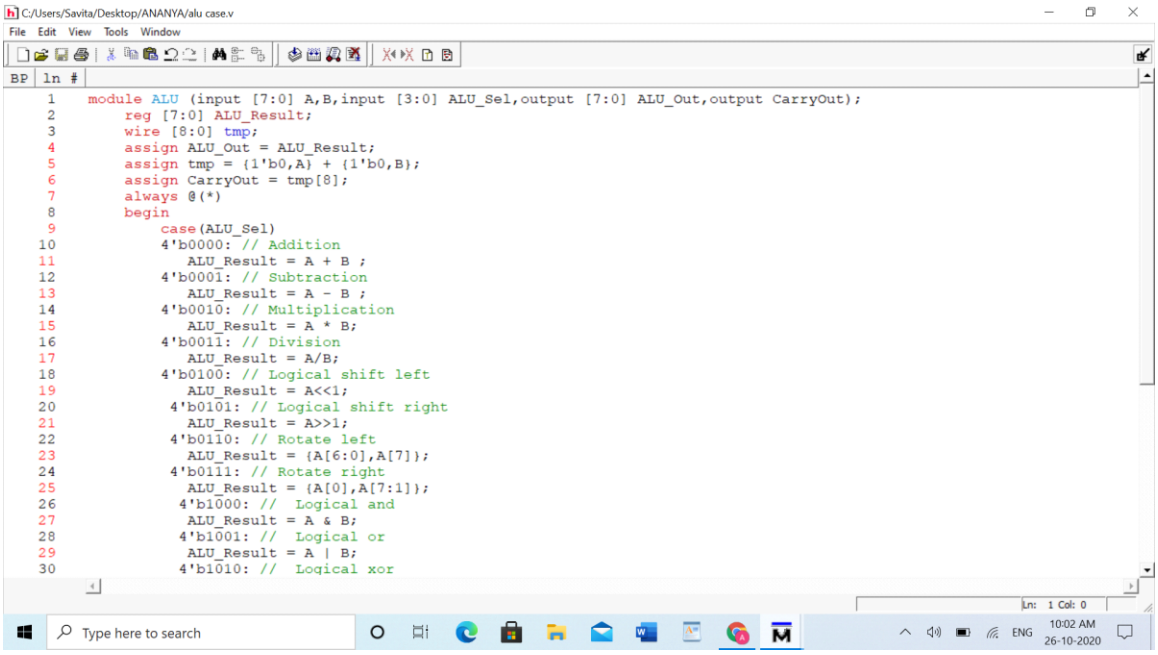
S. No.	TITLE OF EXPERIMENT	Date of Experiment	Date of Submission
EXPERIMENT - 11	Design ALU for operations by CASE STATEMENT (Behavioral Modeling).	06-10-2020	27-10-2020

EXPERIMENT : 11

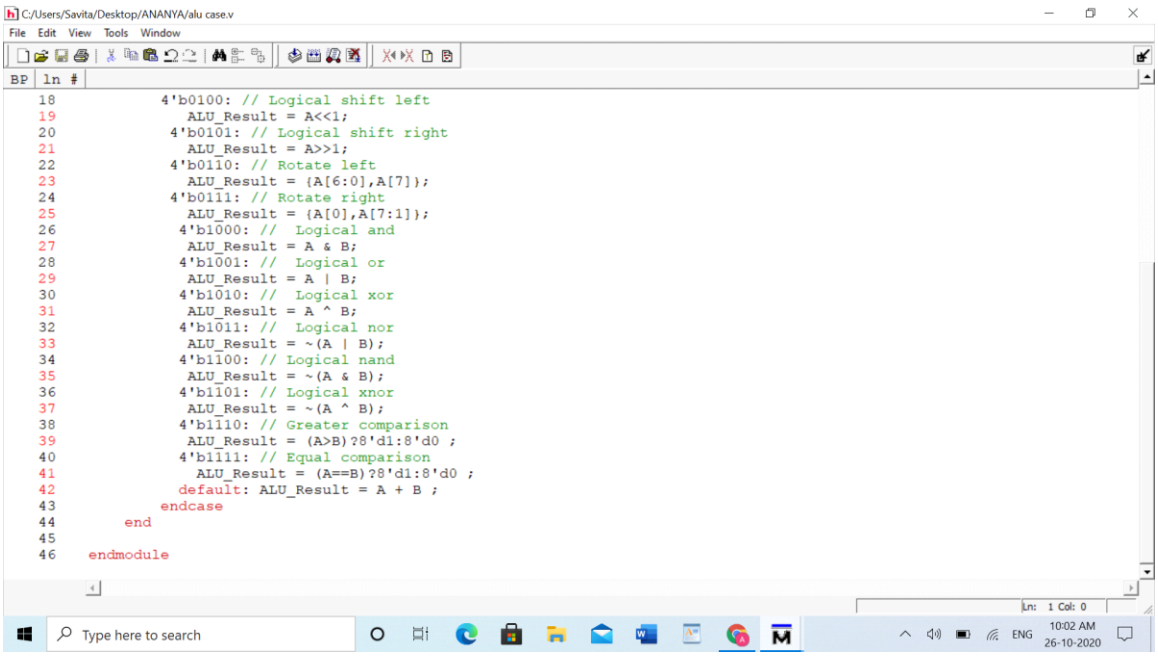
AIM: Design ALU for operations by CASE STATEMENT (Behavioral Modeling).

SOFTWARE REQUIRED: MODELSIM (Verilog).

CODE:



```
C:/Users/Savita/Desktop/ANANYA/alu case.v
File  Edit  View  Tools  Window
BP | ln #
 1  module ALU (input [7:0] A,B,input [3:0] ALU_Sel,output [7:0] ALU_Out,output CarryOut);
 2      reg [7:0] ALU_Result;
 3      wire [8:0] tmp;
 4      assign ALU_Out = ALU_Result;
 5      assign tmp = {1'b0,A} + {1'b0,B};
 6      assign CarryOut = tmp[8];
 7      always @(*)
 8      begin
 9          case(ALU_Sel)
10          4'b0000: // Addition
11             ALU_Result = A + B ;
12          4'b0001: // Subtraction
13             ALU_Result = A - B ;
14          4'b0010: // Multiplication
15             ALU_Result = A * B;
16          4'b0011: // Division
17             ALU_Result = A/B;
18          4'b0100: // Logical shift left
19             ALU_Result = A<<1;
20           4'b0101: // Logical shift right
21             ALU_Result = A>>1;
22           4'b0110: // Rotate left
23             ALU_Result = {A[6:0],A[7]};
24           4'b0111: // Rotate right
25             ALU_Result = {A[0],A[7:1]};
26            4'b1000: //  Logical and
27             ALU_Result = A & B;
28            4'b1001: //  Logical or
29             ALU_Result = A | B;
30            4'b1010: //  Logical xor
```



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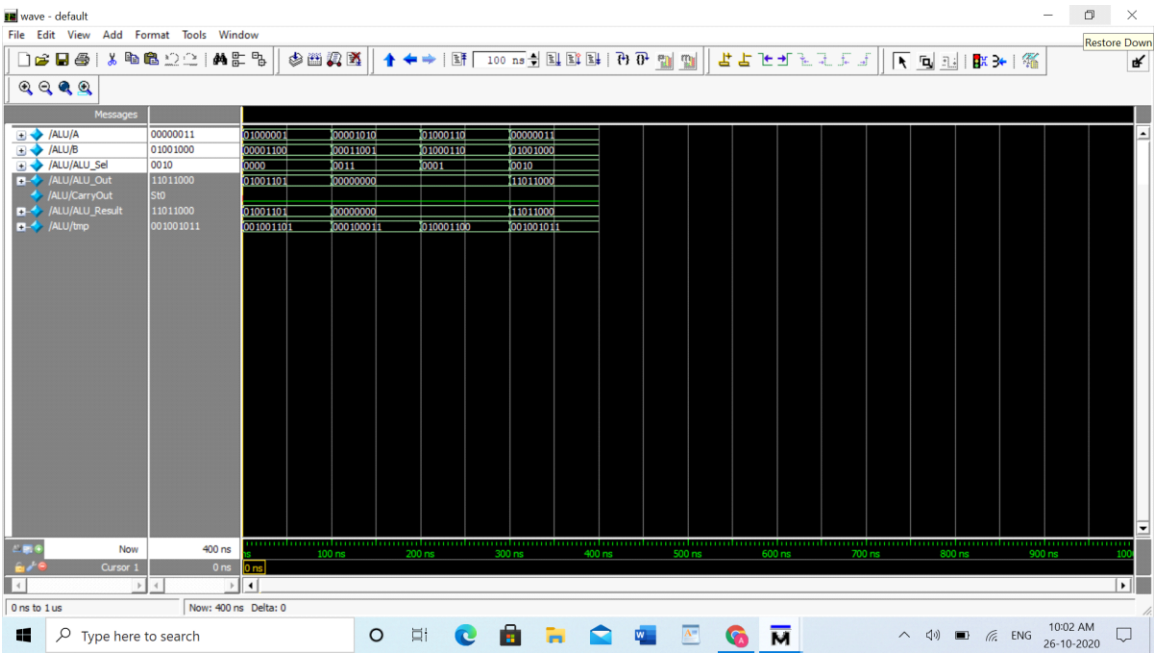
24           4'b0111: // Rotate right
25             ALU_Result = {A[0],A[7:1]};
26            4'b1000: //  Logical and
27             ALU_Result = A & B;
28            4'b1001: //  Logical or
29             ALU_Result = A | B;
30            4'b1010: //  Logical xor
31             ALU_Result = A ^ B;
32            4'b1011: //  Logical nor
33             ALU_Result = ~(A | B);
34            4'b1100: // Logical nand
35             ALU_Result = ~(A & B);
36            4'b1101: // Logical xnor
37             ALU_Result = ~(A ^ B);
38            4'b1110: // Greater comparison
39             ALU_Result = (A>B)?8'd1:8'd0 ;
40            4'b1111: // Equal comparison
41              ALU_Result = (A==B)?8'd1:8'd0 ;
42           default: ALU_Result = A + B ;
43          endcase
44      end
45
46  endmodule
```

WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Restore Down
Messages
/ALU/A
/ALU/B
/ALU/ALU_Sel
/ALU/ALU_Out
/ALU/CarryOut
/ALU/ALU_Result
/ALU/tmp
00000011
01001000
0010
11011000
St0
11011000
001001011
01000001
00001100
0000
01001101
01001101
001001101
00001010
00011001
0011
00000000
00000000
001001011
01000110
01000110
0001
010001100
00000011
01001000
0010
11011000
11011000
001001011
Now
400 ns
Cursor 1
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
0 ns to 1 us
Now: 400 ns Delta: 0
Type here to search
ENG
10:02 AM
26-10-2020