SRMIST

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

DELHI NCR CAMPUS, MODINAGAR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II YEAR / III SEMESTER

ANALOG AND DIGITAL ELECTRONICS LABORATORY

(18CSS201J)

Name of the candidate : ANANYA GUPTA

Register Number : RA1911003030265

Branch-Section :CSE-I

Year/Semester :2ND / 3RD

S. No.	TITLE OF EXPERIMENT
EXPERIMENT	**BEHAVIORAL MODELING BY VERILOG (MODEL SIMULATOR)**
A	**Design UNIVERSAL GATES a-) NAND, b-)NOR using behavioral modeling .**
B	**Design XOR GATE using behavioral modeling.**
C	**Design FULL ADDER using behavioral modeling .**
D	**Design FULL SUBTRACTOR using behavioral modeling .**
E	**Design 4-1 MULTIPLEXER using behavioral modelling .**
F	**Design 3-8 DECODER using behavioral modeling.**

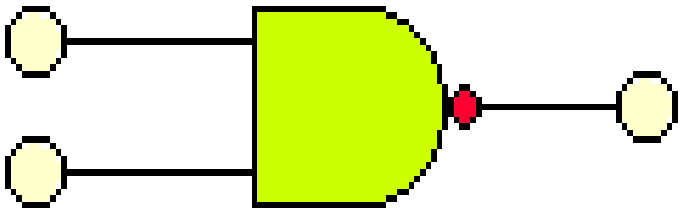
EXPERIMENT:10 A

AIM: Design UNIVERSAL GATES using behavioral modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

A) – NAND GATE:

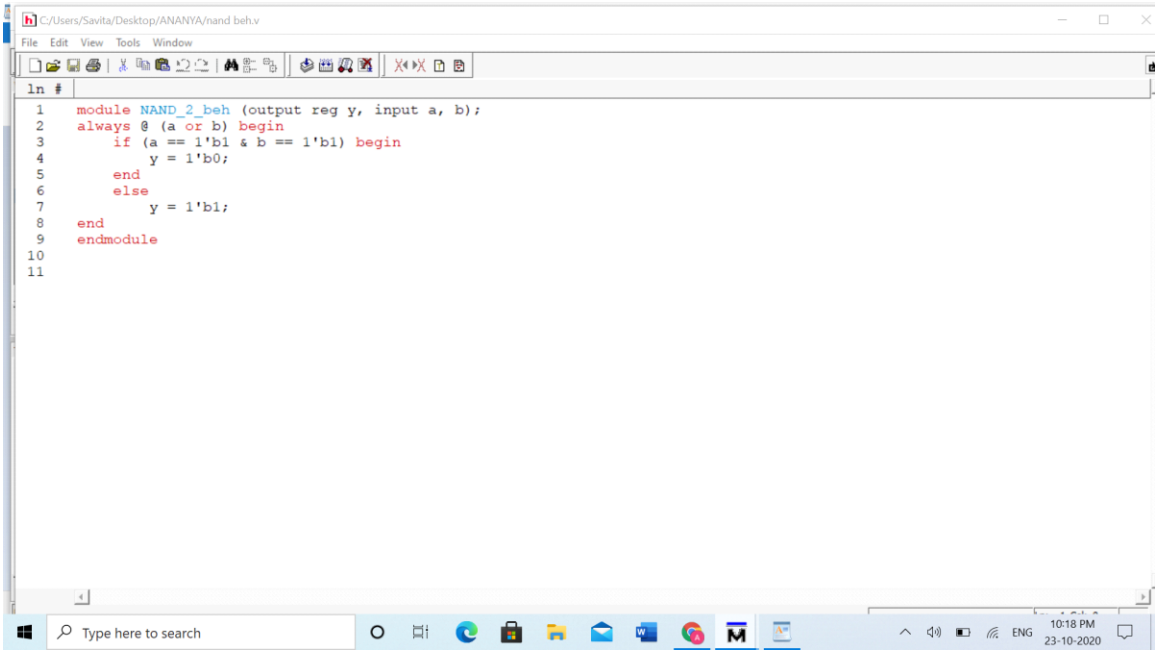
LOGIC DIAGARM:



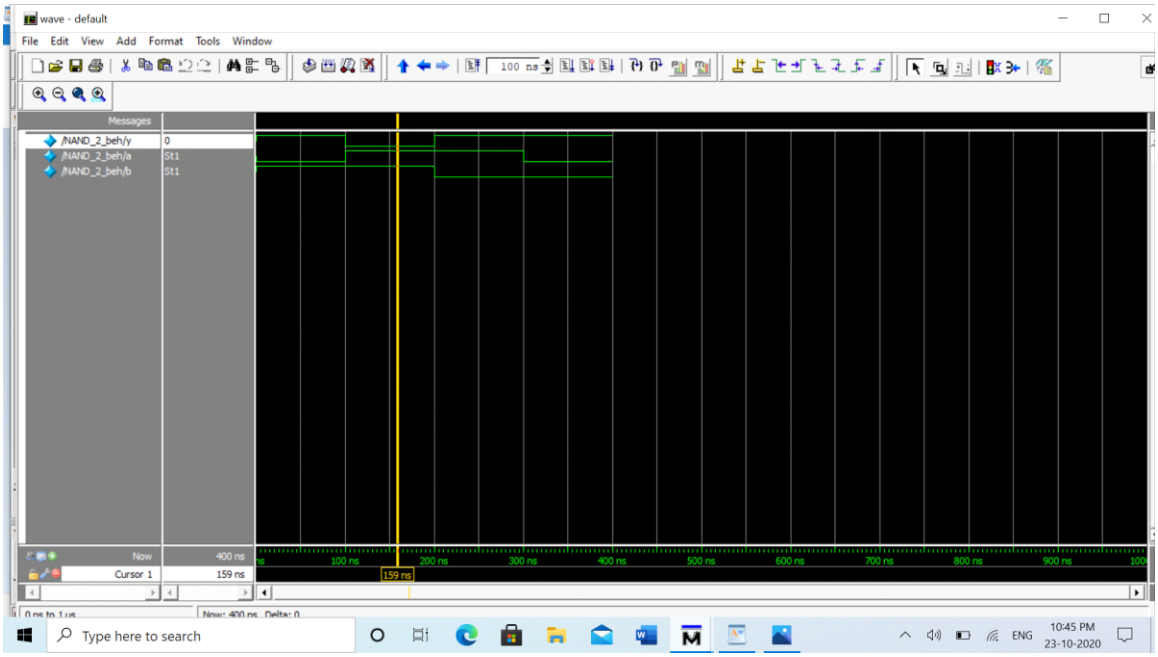
TRUTH TABLE:

Input		Output
A	B	Y= $\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

CODE:

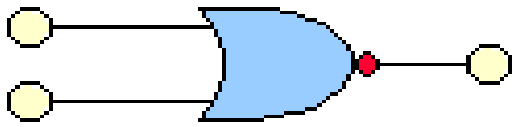

C:/Users/Savita/Desktop/ANANYA/nand beh.v
File Edit View Tools Window
ln #
1 module NAND_2_beh (output reg y, input a, b);
2 always @ (a or b) begin
3 if (a == 1'b1 & b == 1'b1) begin
4 y = 1'b0;
5 end
6 else
7 y = 1'b1;
8 end
9 endmodule
10
11
Type here to search
ENG
10:18 PM
23-10-2020

WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/NAND_2_beh/y
/NAND_2_beh/a
/NAND_2_beh/b
Now
Cursor 1
159 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
Type here to search
ENG
10:45 PM
23-10-2020

B) NOR GATE:

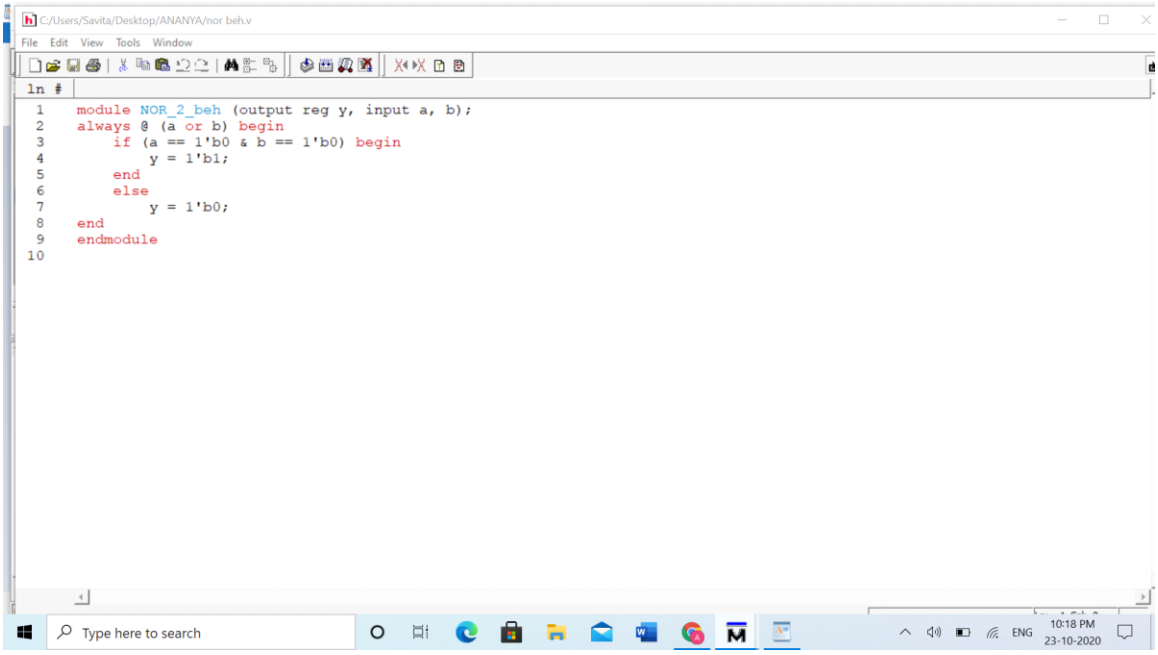
LOGIC DIAGRAM:



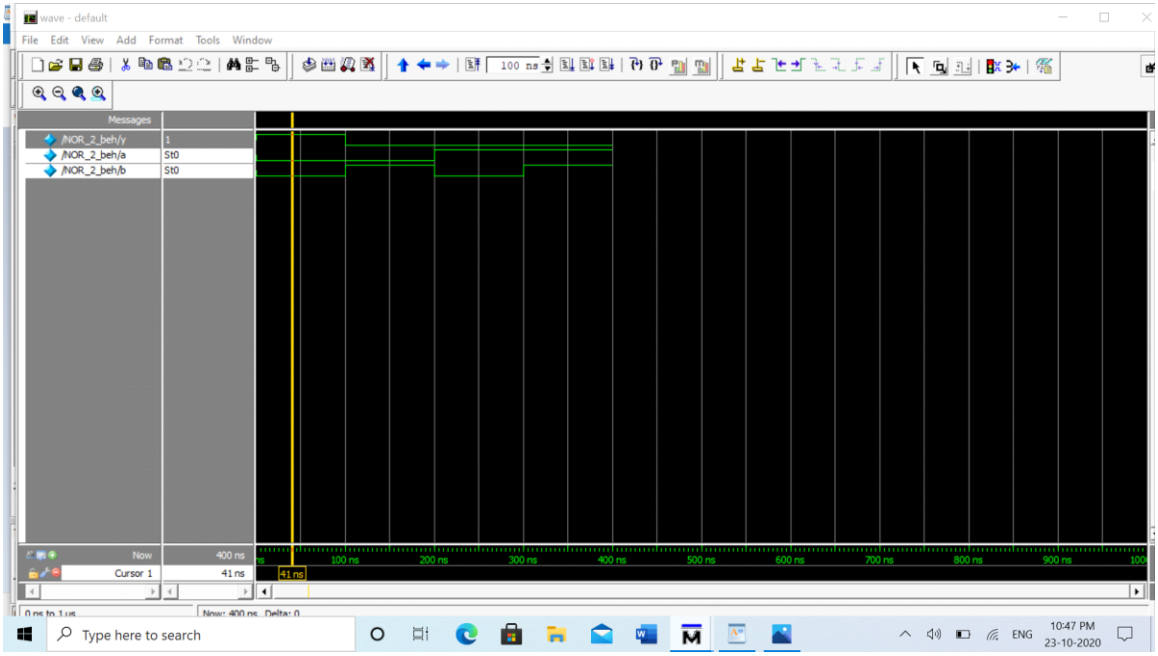
TRUTH TABLE:

Input		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

CODE:


C:/Users/Savita/Desktop/ANANYA/nor beh.v
File Edit View Tools Window
ln #
1 module NOR_2_beh (output reg y, input a, b);
2 always @ (a or b) begin
3 if (a == 1'b0 & b == 1'b0) begin
4 y = 1'b1;
5 end
6 else
7 y = 1'b0;
8 end
9 endmodule
10
Type here to search
ENG
10:18 PM
23-10-2020

WAVEFORM:

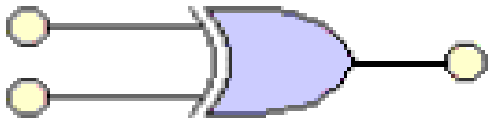

wave - default
File Edit View Add Format Tools Window
Messages
/NOR_2_beh/y
/NOR_2_beh/a
/NOR_2_beh/b
Now
Cursor 1
41 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
Type here to search
ENG
10:47 PM
23-10-2020

EXPERIMENT:10 B

AIM: Design XOR GATE using behavioral modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

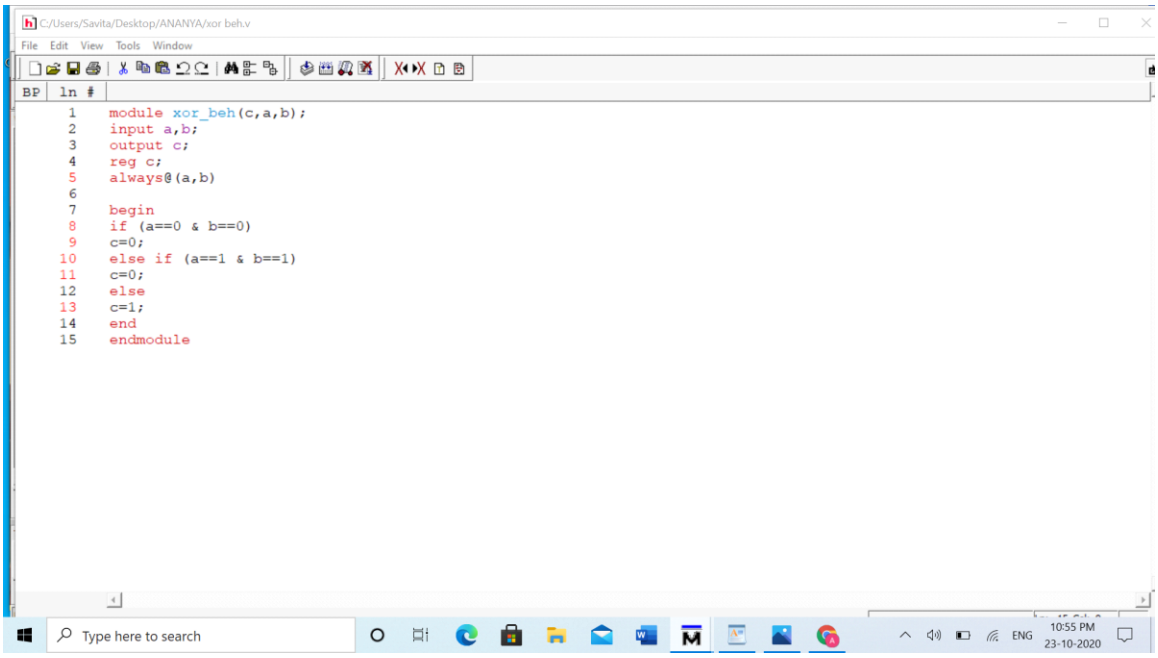
LOGIC DIAGRAM:



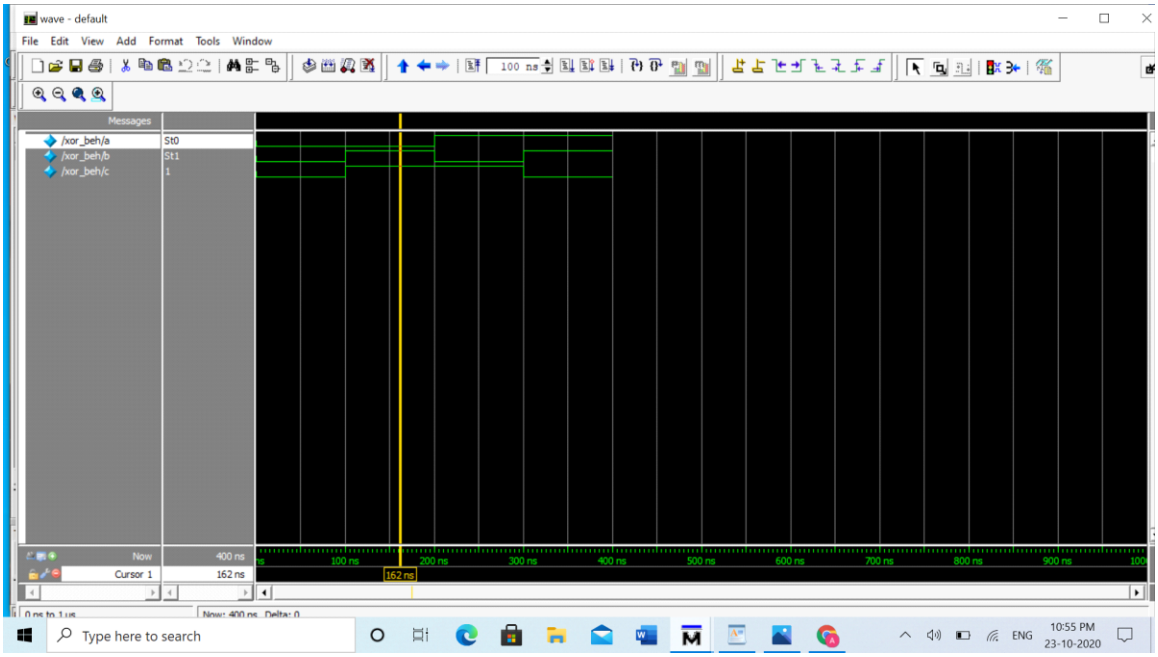
TRUTH TABLE:

XOR Truth Table		
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

CODE:


C:/Users/Savita/Desktop/ANANYA/xor beh.v
File Edit View Tools Window
BP ln #
1 module xor_beh(c,a,b);
2 input a,b;
3 output c;
4 reg c;
5 always@(a,b)
6
7 begin
8 if (a==0 & b==0)
9 c=0;
10 else if (a==1 & b==1)
11 c=0;
12 else
13 c=1;
14 end
15 endmodule
Type here to search
ENG
10:55 PM
23-10-2020

WAVEFORM:

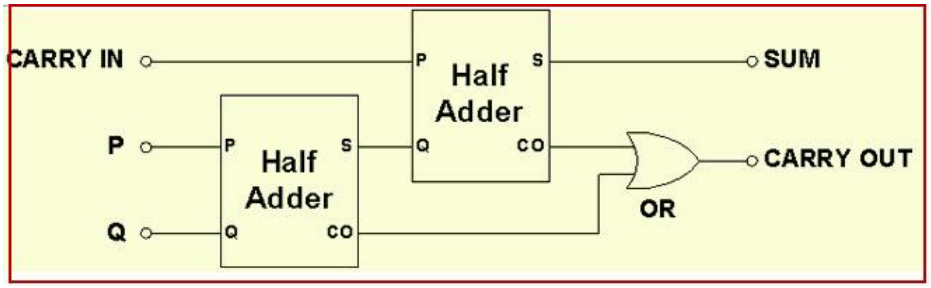

wave - default
File Edit View Add Format Tools Window
Messages
/xor_beh/a
/xor_beh/b
/xor_beh/c
St0
St1
1
Now
400 ns
Cursor 1
162 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
Type here to search
ENG
10:55 PM
23-10-2020

EXPERIMENT:10 C

AIM: Design FULL ADDER using behavioral modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

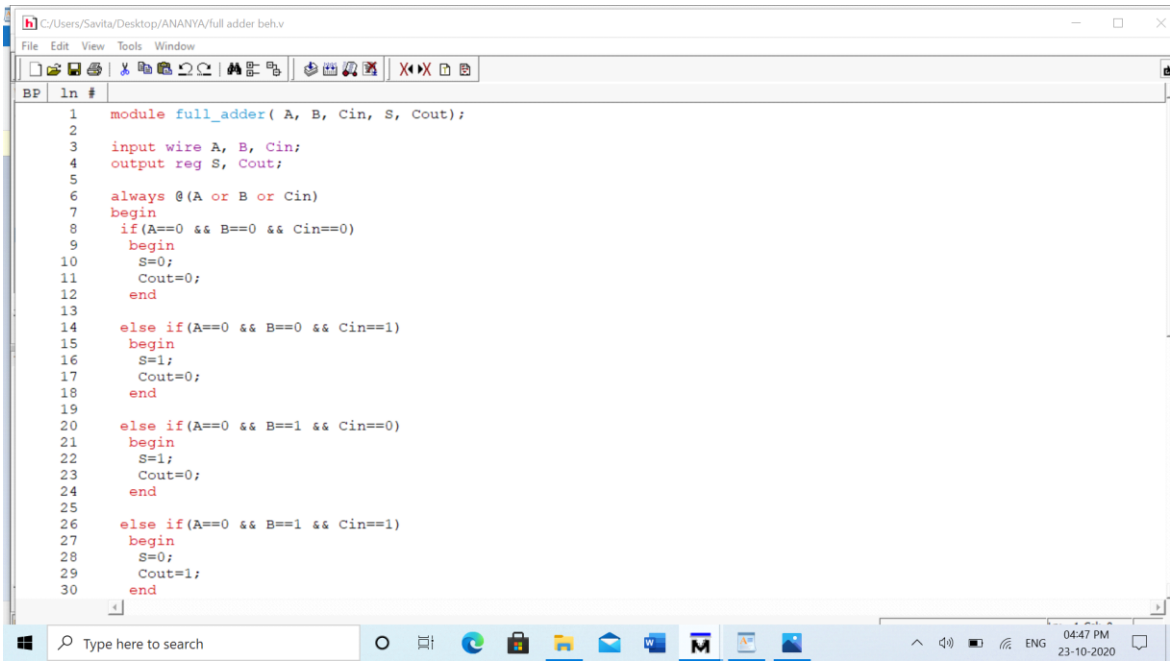
LOGIC DIAGRAM:

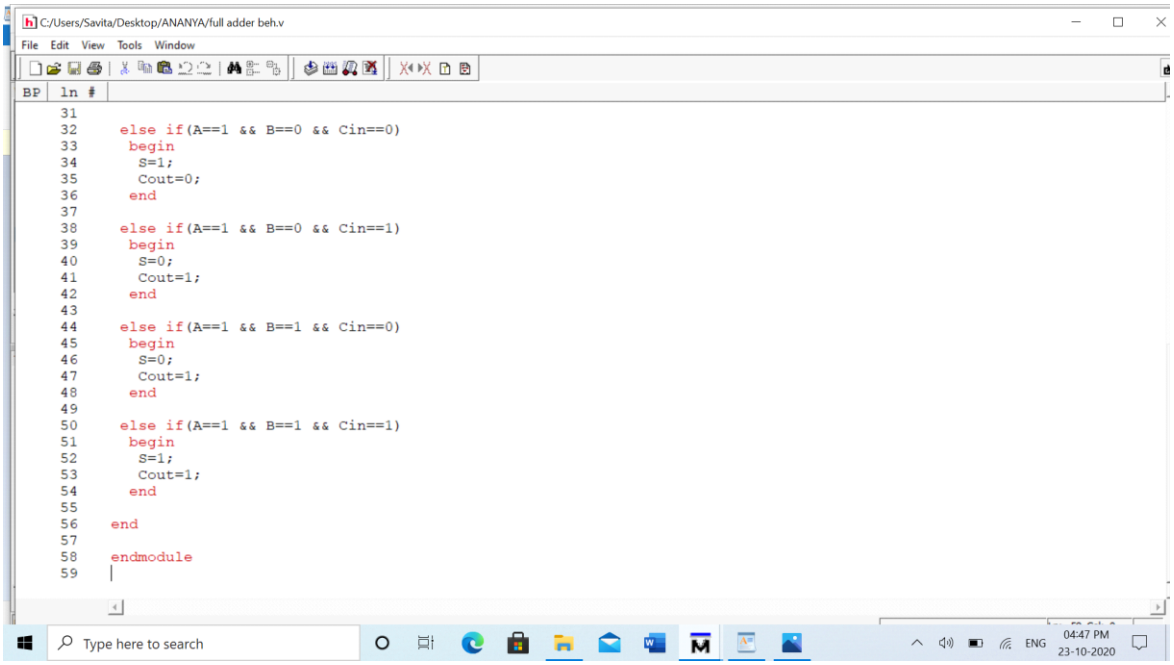


TRUTH TABLE:

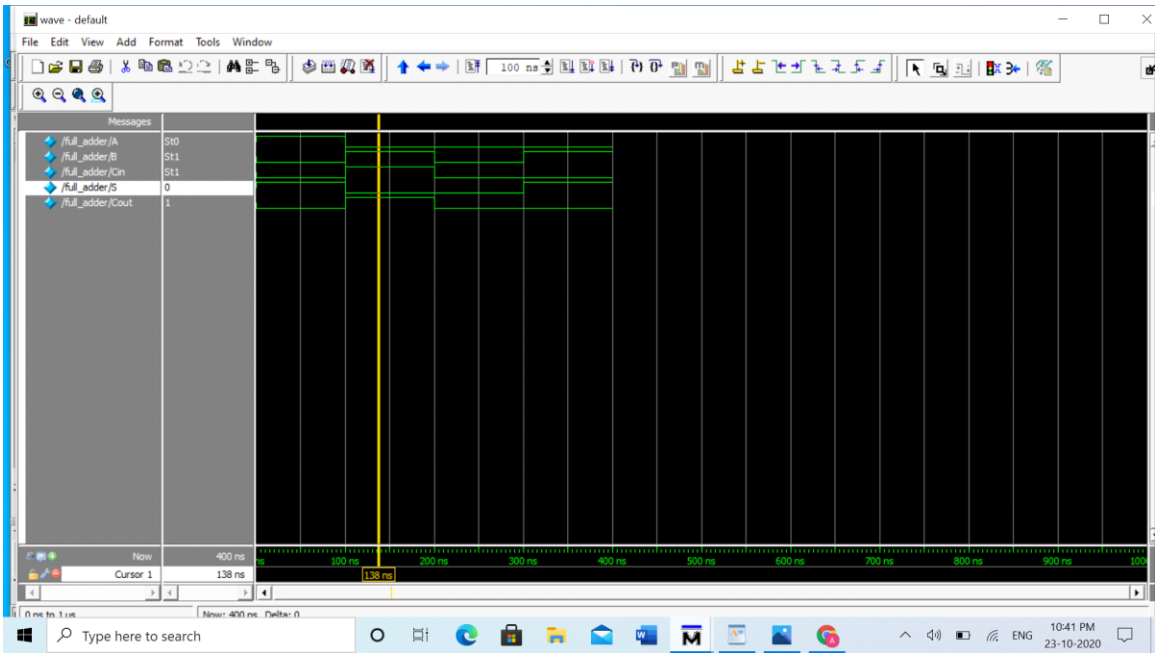
Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

CODE:


C:/Users/Savita/Desktop/ANANYA/full adder beh.v
File Edit View Tools Window
BP ln #
1 module full_adder(A, B, Cin, S, Cout);
2
3 input wire A, B, Cin;
4 output reg S, Cout;
5
6 always @(A or B or Cin)
7 begin
8 if(A==0 && B==0 && Cin==0)
9 begin
10 S=0;
11 Cout=0;
12 end
13
14 else if(A==0 && B==0 && Cin==1)
15 begin
16 S=1;
17 Cout=0;
18 end
19
20 else if(A==0 && B==1 && Cin==0)
21 begin
22 S=1;
23 Cout=0;
24 end
25
26 else if(A==0 && B==1 && Cin==1)
27 begin
28 S=0;
29 Cout=1;
30 end
Type here to search
ENG
04:47 PM
23-10-2020


C:/Users/Savita/Desktop/ANANYA/full adder beh.v
File Edit View Tools Window
BP ln #
31
32 else if(A==1 && B==0 && Cin==0)
33 begin
34 S=1;
35 Cout=0;
36 end
37
38 else if(A==1 && B==0 && Cin==1)
39 begin
40 S=0;
41 Cout=1;
42 end
43
44 else if(A==1 && B==1 && Cin==0)
45 begin
46 S=0;
47 Cout=1;
48 end
49
50 else if(A==1 && B==1 && Cin==1)
51 begin
52 S=1;
53 Cout=1;
54 end
55
56 end
57
58 endmodule
59
Type here to search
ENG
04:47 PM
23-10-2020

WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/full_adder/A
/full_adder/B
/full_adder/Cin
/full_adder/S
/full_adder/Cout
St0
St1
St1
0
1
Now
400 ns
Cursor 1
138 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
Type here to search
ENG
10:41 PM
23-10-2020

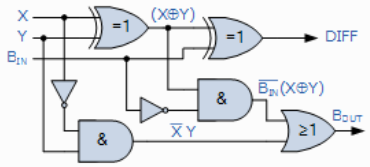
EXPERIMENT:10 D

AIM: Design FULL SUBTRACTOR using behavioral modeling .

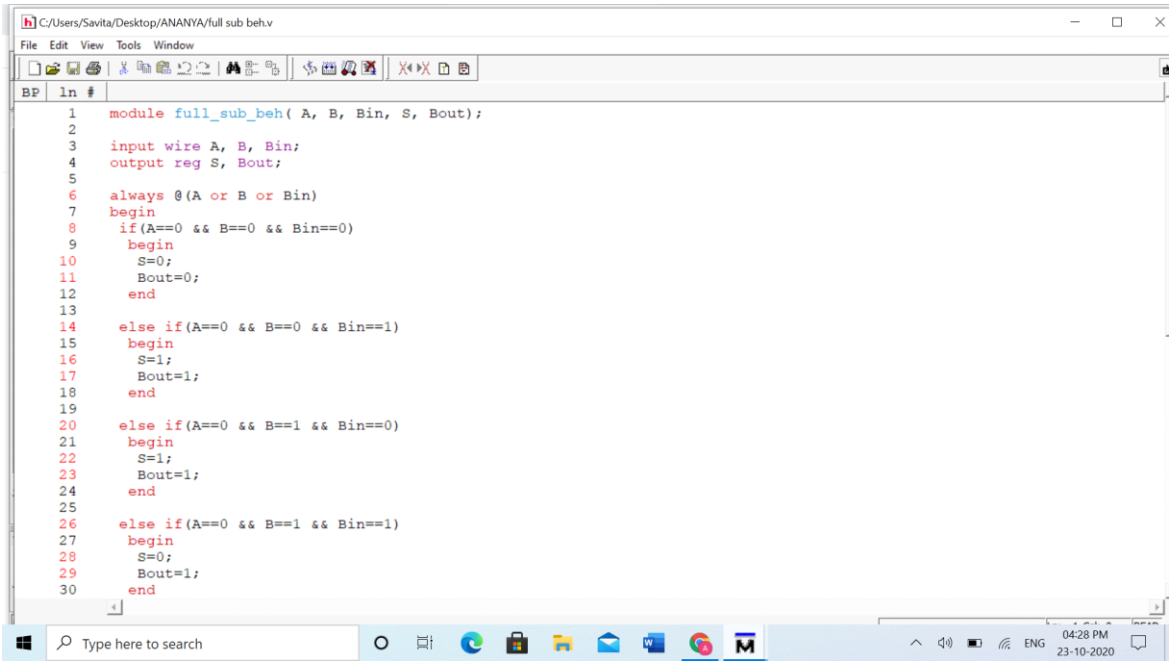
SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

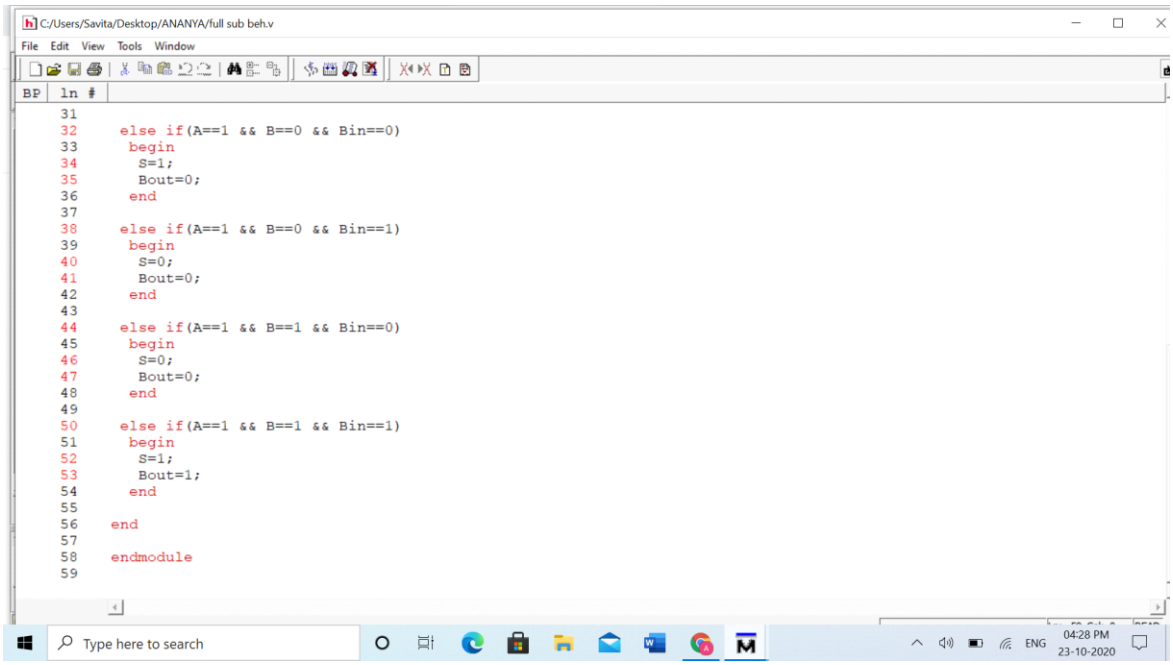
LOGIC DIAGRAM:

Symbol	Truth Table				
	B-in	Y	X	Diff.	B-out
	0	0	0	0	0
	0	0	1	1	1
	0	1	0	1	1
	0	1	1	0	1
	1	0	0	1	0
	1	0	1	0	0
	1	1	0	0	0
	1	1	1	1	1

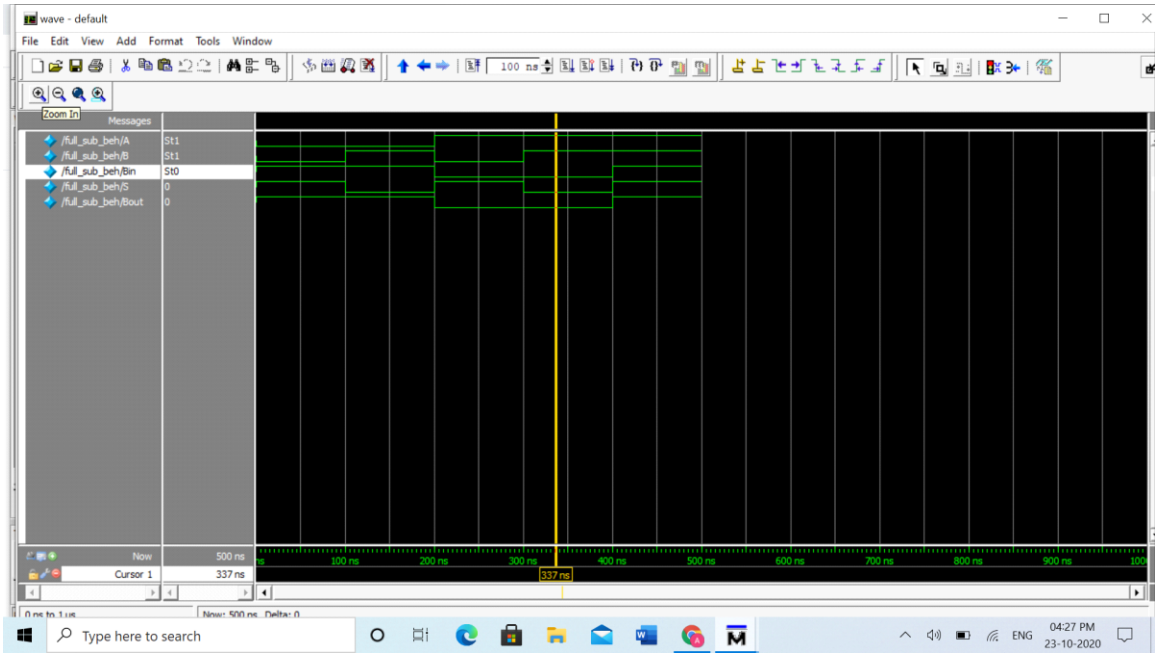


CODE:




C:/Users/Savita/Desktop/ANANYA/full sub beh.v
File Edit View Tools Window
BP ln #
31
32 else if(A==1 && B==0 && Bin==0)
33 begin
34 S=1;
35 Bout=0;
36 end
37
38 else if(A==1 && B==0 && Bin==1)
39 begin
40 S=0;
41 Bout=0;
42 end
43
44 else if(A==1 && B==1 && Bin==0)
45 begin
46 S=0;
47 Bout=0;
48 end
49
50 else if(A==1 && B==1 && Bin==1)
51 begin
52 S=1;
53 Bout=1;
54 end
55
56 end
57
58 endmodule
59
Type here to search
ENG
04:28 PM
23-10-2020

WAVEFORM:

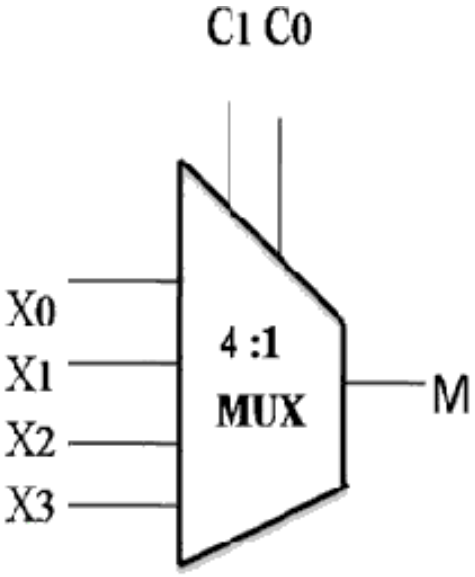

wave - default
File Edit View Add Format Tools Window
Zoom In
Messages
/full_sub_beh/A
/full_sub_beh/B
/full_sub_beh/Bin
/full_sub_beh/S
/full_sub_beh/Bout
St1
St1
St0
0
0
Now
500 ns
Cursor 1
337 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
337 ns
Type here to search
ENG
04:27 PM
23-10-2020

EXPERIMENT:10 E

AIM: Design 4-1 MULTIPLEXER using behavioral modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

LOGIC DIAGRAM:



(a)

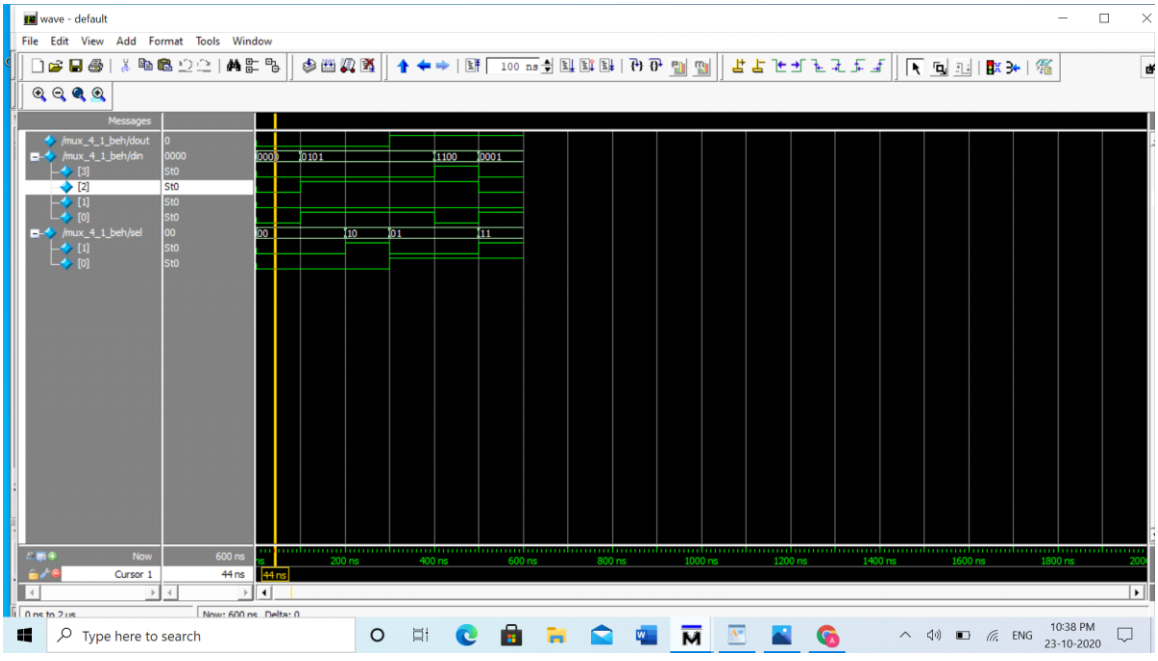
C1	C0	M
0	0	X0
0	1	X1
1	0	X2
1	1	X3

(b)

CODE:

```
module mux_4_1_beh( din ,sel ,dout );

output dout ;
reg dout ;

input [3:0] din ;
wire [3:0] din ;
input [1:0] sel ;
wire [1:0] sel ;

always @ (din or sel) begin
 if (sel==0)
  dout = din[3];
 else if (sel==1)
  dout = din[2];
 else if (sel==2)
  dout = din[1];
 else
  dout = din[0];
end

endmodule
```

WAVEFORM:

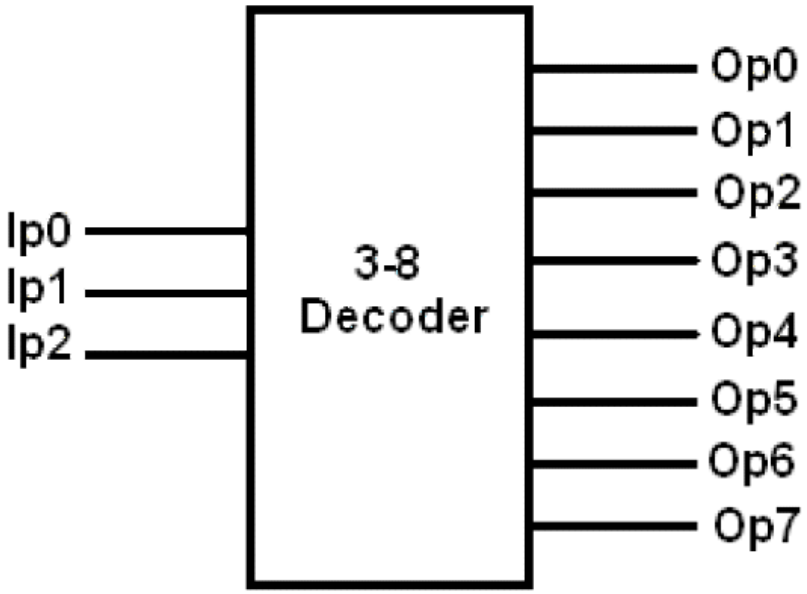


EXPERIMENT:10 F

AIM: Design 3-8 DECODER using behavioral modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

LOGIC DIAGRAM:

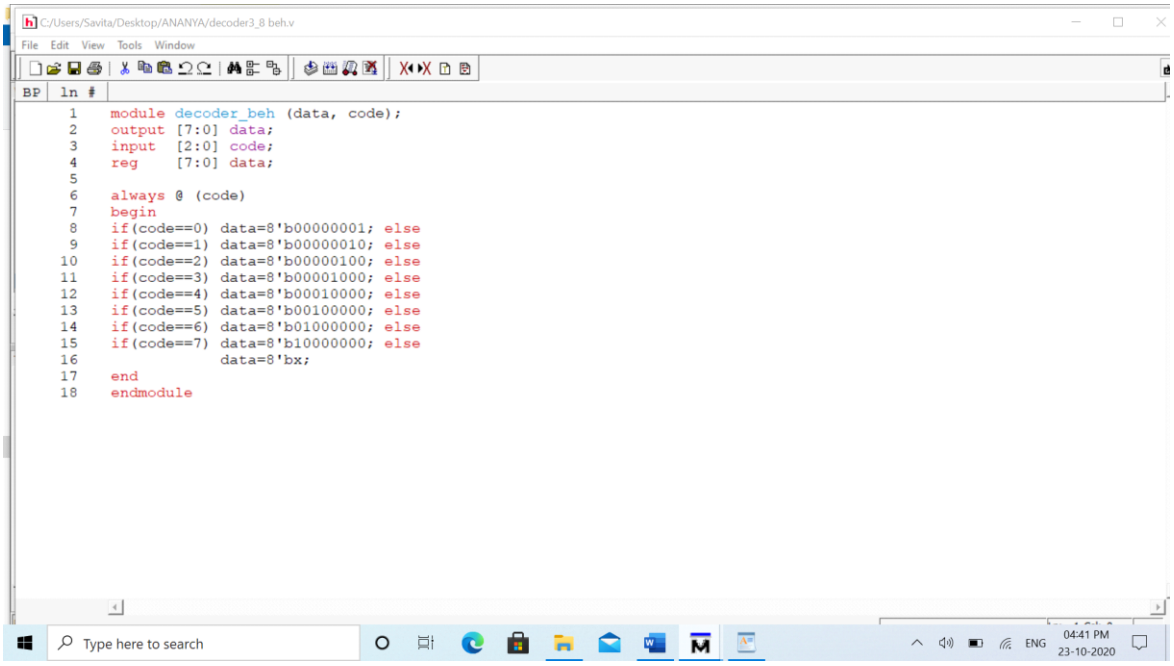


3 to 8 Line Decoder

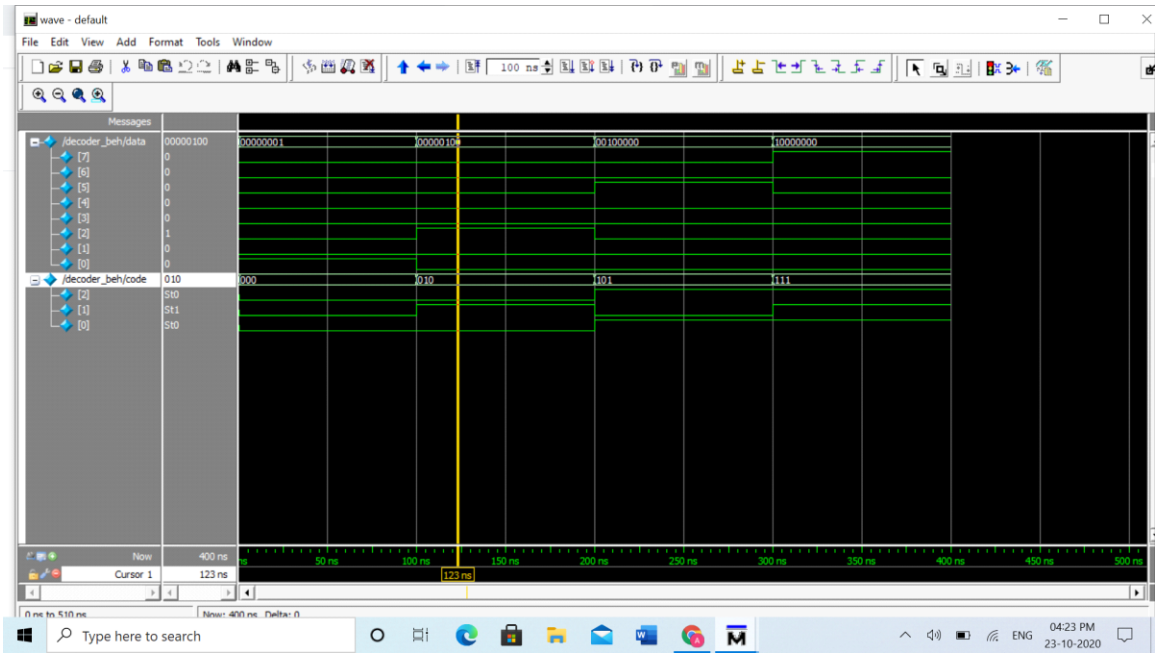
Inputs			Outputs							
x	y	z	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

electroniclinic.com

CODE:



WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/decoder_beh/data
00000100
[7]
[6]
[5]
[4]
[3]
[2]
[1]
[0]
/decoder_beh/code
010
[2]
[1]
[0]
St0
St1
St0
00000001
00000100
00100000
10000000
000
010
101
111
Now
400 ns
Cursor 1
123 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns
400 ns
450 ns
500 ns
Type here to search
ENG
04:23 PM
23-10-2020