SRMIST

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY

DELHI NCR CAMPUS, MODINAGAR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

II YEAR / III SEMESTER

ANALOG AND DIGITAL ELECTRONICS LABORATORY

(18CSS201J)

Name of the candidate : ANANYA GUPTA

Register Number : RA1911003030265

Branch-Section :CSE-I

Year/Semester :2ND / 3RD

S. No.	TITLE OF EXPERIMENT
EXPERIMENT - 11	Design a)-BINARY TO GRAY Converter b)- GRAY TO BINARY Converter using gate level modeling.

EXPERIMENT : 11

AIM: Design

a)-BINARY TO GRAY Converter

b)- GRAY TO BINARY Converter

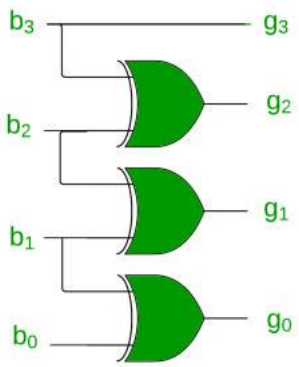
using gate level modeling.

SOFTWARE REQUIRED: MODEL SIMULATOR (verilog).

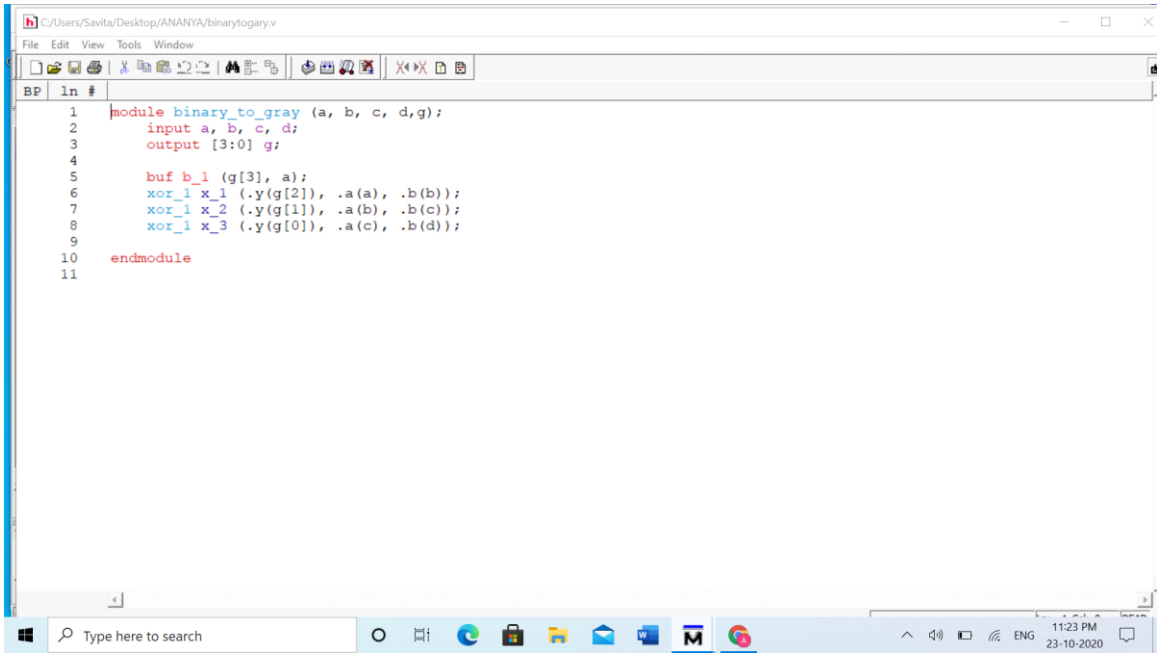
a)- BINARY TO GRAY Converter.

LOGIC DIAGRAM:

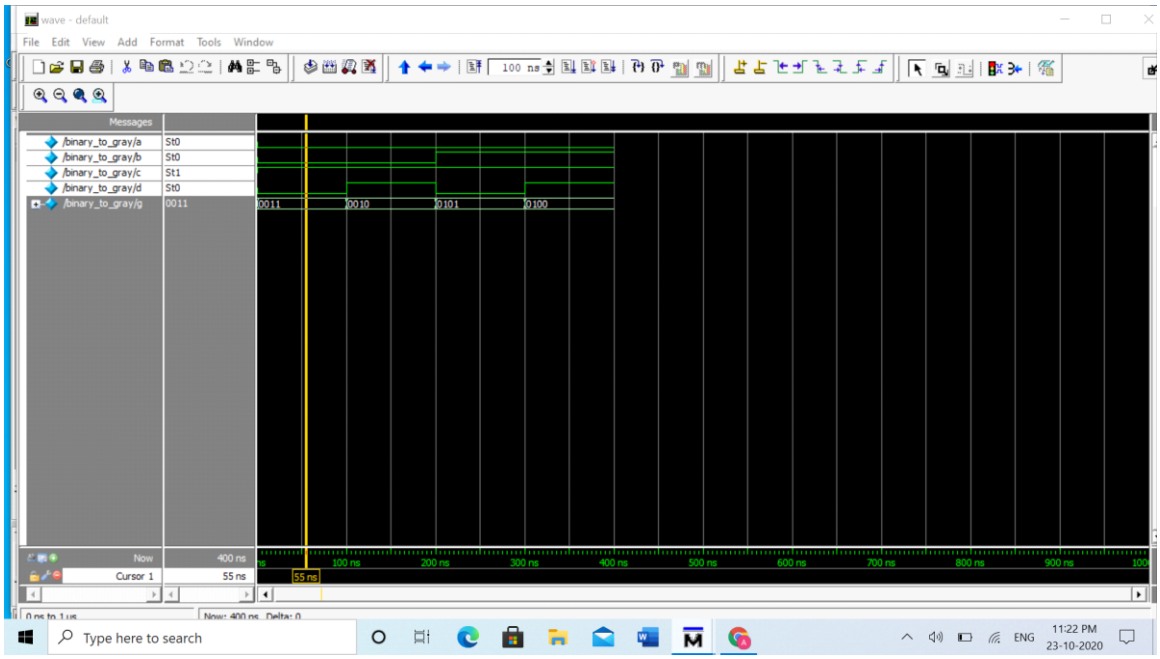
Decimal Number	4 bit Binary Number ABCD	4 bit Gray Code $G_1G_2G_3G_4$
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1
10	1 0 1 0	1 1 1 1
11	1 0 1 1	1 1 1 0
12	1 1 0 0	1 0 1 0
13	1 1 0 1	1 0 1 1
14	1 1 1 0	1 0 0 1
15	1 1 1 1	1 0 0 0



CODE:



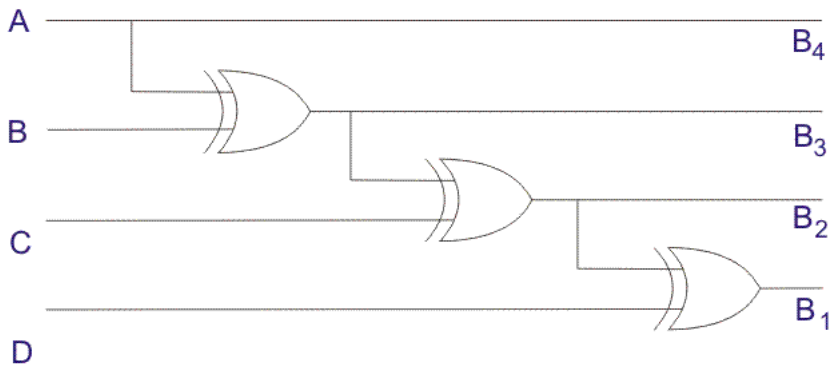
WAVEFORM:



b)- GRAY TO BINARY Converter.

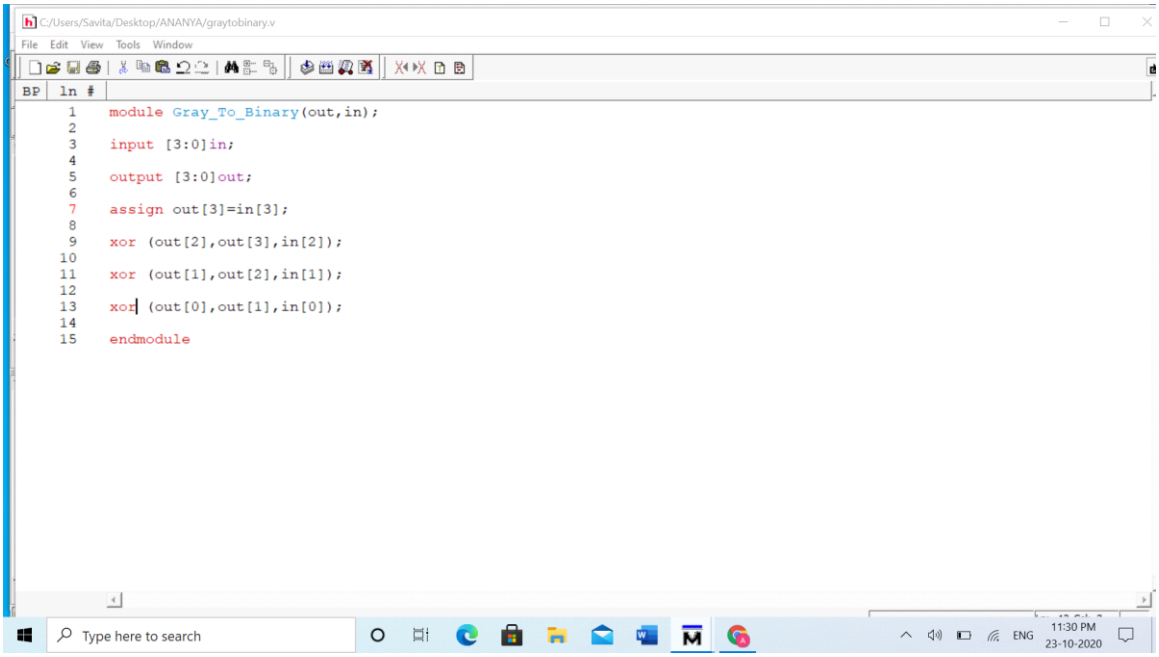
LOGIC DIAGRAM:

4 bit Gray Code	4 bit Binary Code
A B C D	B_4 B_3 B_2 B_1
0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1
0 0 1 1	0 0 1 0
0 0 1 0	0 0 1 1
0 1 1 0	0 1 0 0
0 1 1 1	0 1 0 1
0 1 0 1	0 1 1 0
0 1 0 0	0 1 1 1
1 1 0 0	1 0 0 0
1 1 0 1	1 0 0 1
1 1 1 1	1 0 1 0
1 1 1 0	1 0 1 1
1 0 1 0	1 1 0 0
1 0 1 1	1 1 0 1
1 0 0 1	1 1 1 0
1 0 0 0	1 1 1 1



Logic Circuit for Gray to Binary Code Converter

CODE:



WAVEFORM: