# SRMIST

**SRM INSTITUTE OF SCIENCE AND TECHNOLOGY**

**DELHI NCR CAMPUS, MODINAGAR**

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**II YEAR / III SEMESTER**

**ANALOG AND DIGITAL ELECTRONICS LABORATORY**

**(18CSS201J)**

**Name of the candidate : ANANYA GUPTA**

**Register Number : RA1911003030265**

**Branch-Section :CSE-I**

**Year/Semester :2$^{ND}$ / 3$^{RD}$**

| S. No. | TITLE OF EXPERIMENT |
|---|---|
| EXPERIMENT | GATE LEVEL MODELING BY VERILOG (MODEL SIMULATOR) |
| A | **Design AND GATE using gate level modeling .** |
| B | **Design NOT GATE using gate level modeling .** |
| C | **Design OR GATE using gate level modeling .** |
| D | **Design UNIVERSAL GATES**<br>**a-) NAND,**<br>**b-)NOR,**<br>**c-)EX-OR,**<br>**d-)EX-NOR**<br>**using gate level modeling .** |
| E | **Design EX-OR GATE with WIRE SYNTAX using gate level modeling .** |
| F | **Design HALF ADDER using gate level modeling .** |
| G | **Design FULL ADDER using gate level modeling .** |
| H | **Design HALF SUBTRACTOR using gate level modeling .** |
| I | **Design FULL SUBTRACTOR using gate level modeling .** |
| J | **Design 4-1 MULTIPLEXER using gate level modelling .** |
| K | **Design 3-8 DECODER using** |

| | gate level modeling |
|---|---|

# EXPERIMENT:  6 : GATE LEVEL MODELING BY VERILOG

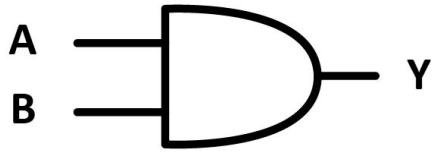
## EXPERIMENT:A

**AIM:  Design AND GATE using gate level modeling .**

**SOFTWARE REQUIRED: MODEL SIMULATOR(VERILOG).**

**LOGIC DIAGARM:**

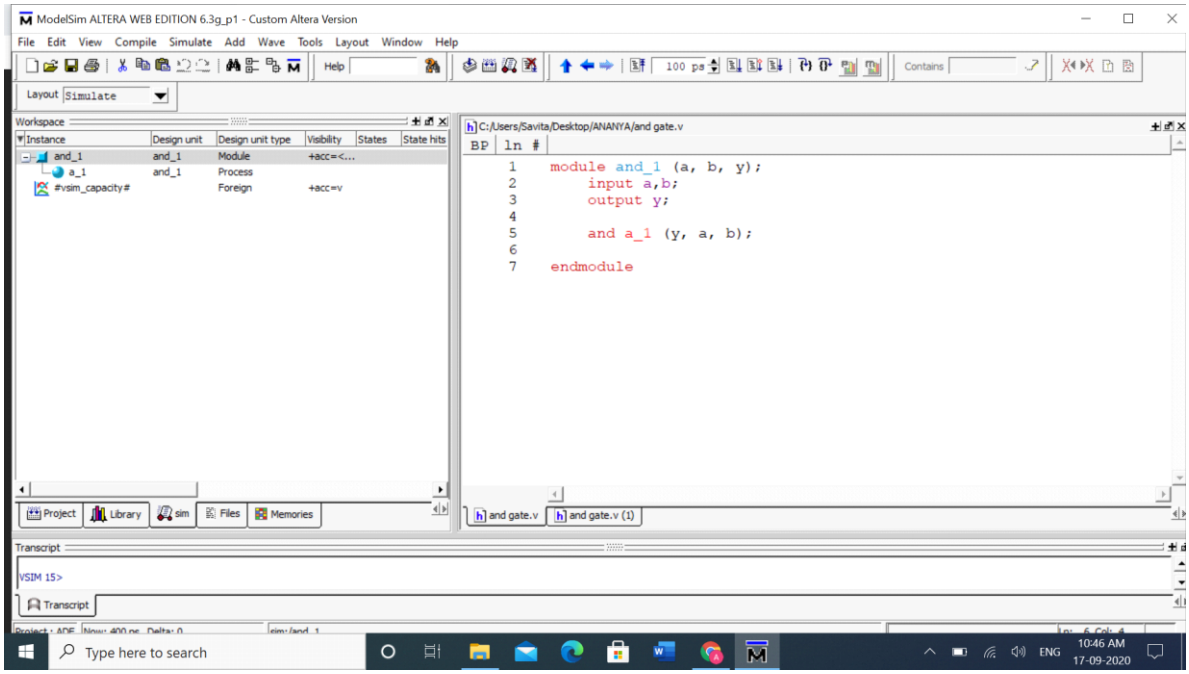
| Inputs | | Output |
|---|---|---|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



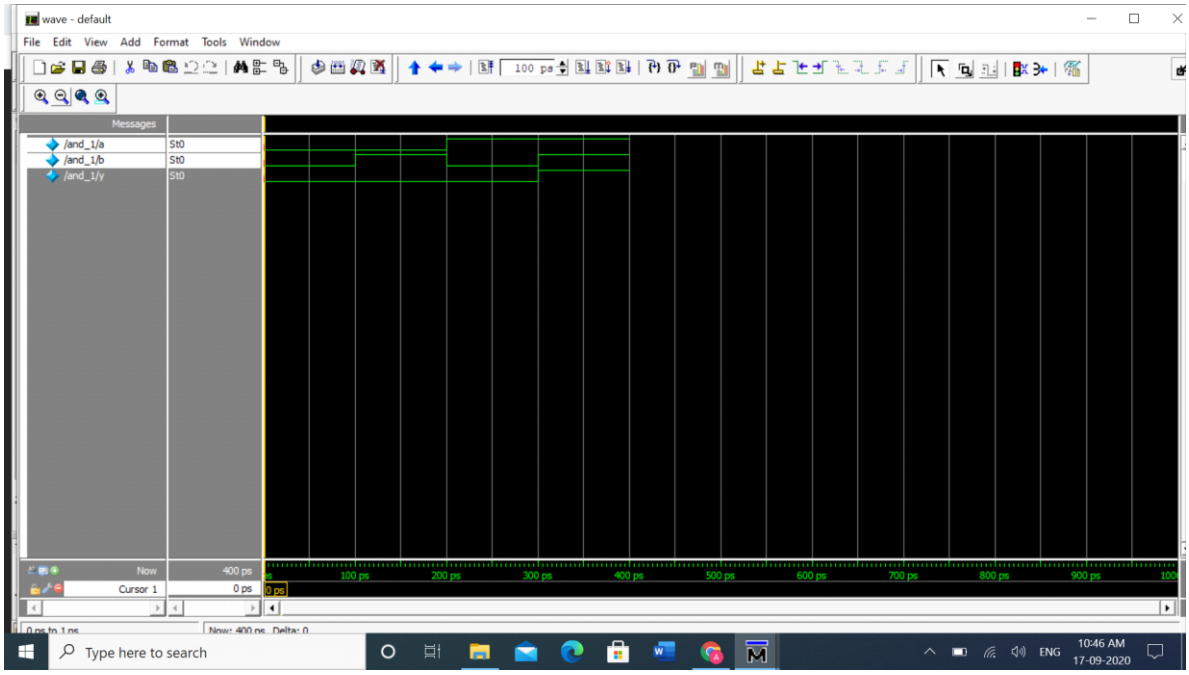

AND

## Truth Table

**CODE:**


ModelSim ALTERA WEB EDITION 6.3g_p1 - Custom Altera Version
File Edit View Compile Simulate Add Wave Tools Layout Window Help
Workspace
Instance Design unit Design unit type Visibility States State hits
and_1 and_1 Module +acc=<...
a_1 and_1 Process
#vsim_capacity# Foreign +acc=v
C:/Users/Savita/Desktop/ANANYA/and gate.v
BP ln #
1 module and_1 (a, b, y);
2 input a,b;
3 output y;
4
5 and a_1 (y, a, b);
6
7 endmodule
Project Library sim Files Memories
and gate.v and gate.v (1)
Transcript
VSIM 15>
Transcript
Type here to search
ENG
10:46 AM
17-09-2020

WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/and_1/a
/and_1/b
/and_1/y
St0
Now
400 ps
Cursor 1
0 ps
100 ps 200 ps 300 ps 400 ps 500 ps 600 ps 700 ps 800 ps 900 ps
Type here to search
ENG
10:46 AM
17-09-2020

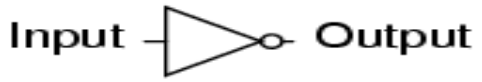
# EXPERIMENT:B

**AIM: Design NOT GATE using gate level modeling .**

**SOFTWARE REQUIRED: MODEL SIMULATOR(VERILOG).**

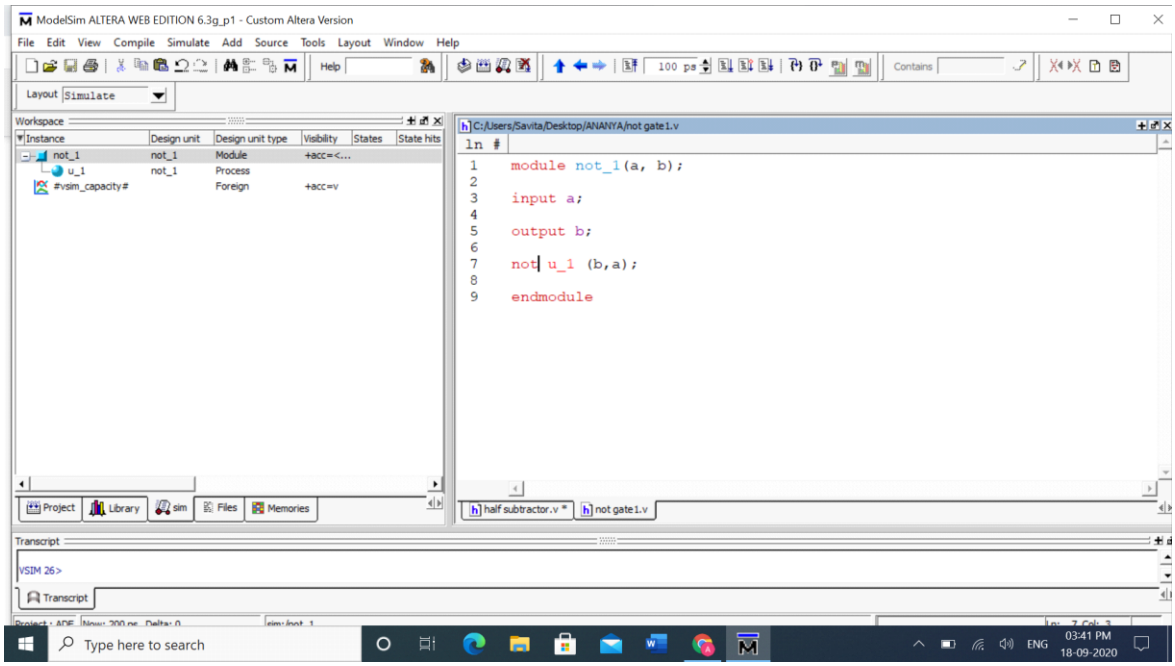
**LOGIC DIAGARM**:

*NOT gate truth table*

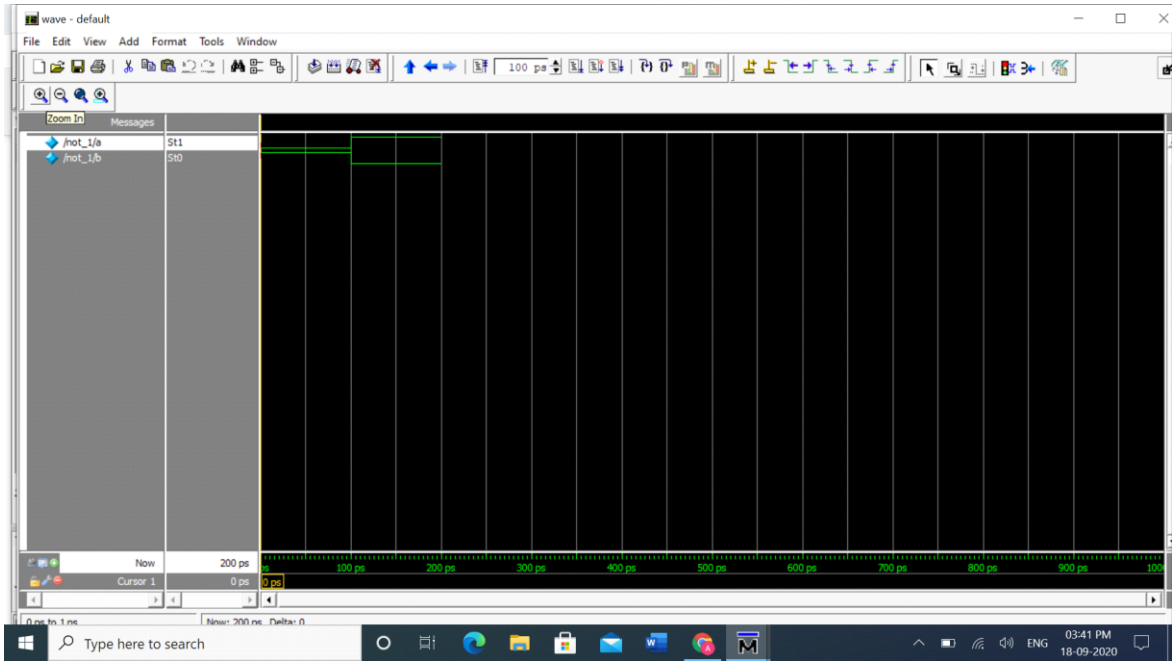



| Input | Output |
|---|---|
| 0 | 1 |
| 1 | 0 |

CODE:



WAVEFORM:

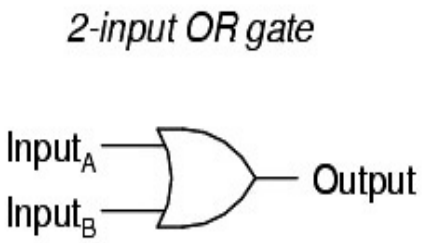

wave - default
File Edit View Add Format Tools Window
Zoom In
Messages
/not_1/a
/not_1/b
St1
St0
Now
200 ps
Cursor 1
0 ps
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
Type here to search
ENG
03:41 PM
18-09-2020

# EXPERIMENT:C

**AIM: Design OR GATE using gate level modeling .**

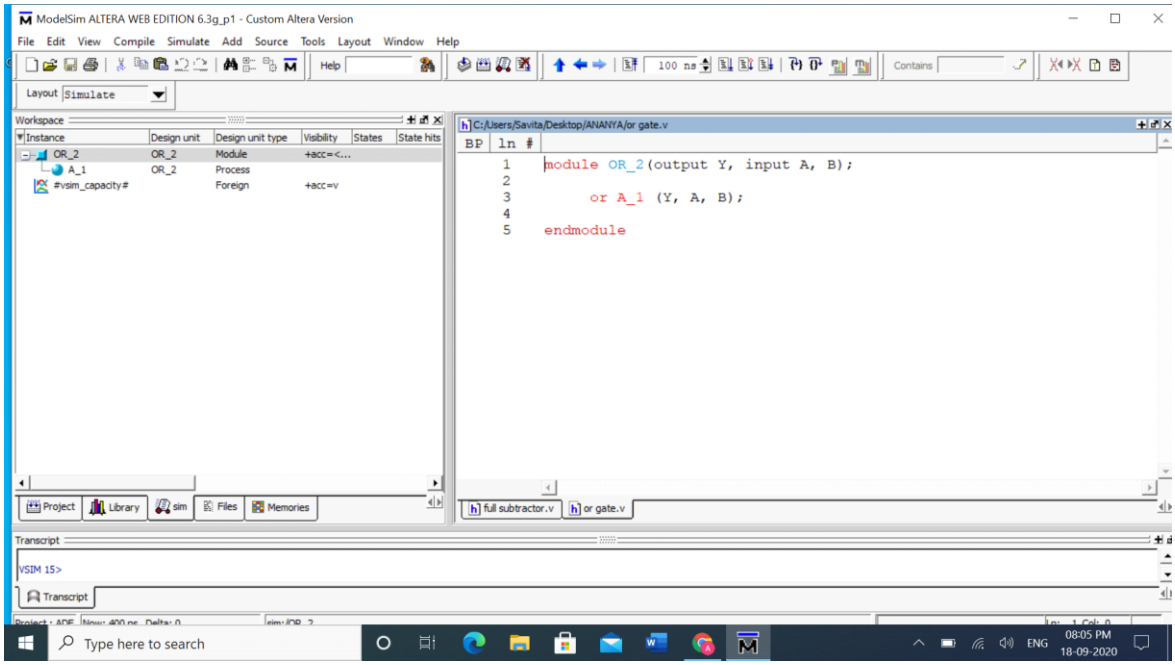
**SOFTWARE REQUIRED: MODEL SIMULATOR(VERILOG).**

**LOGIC DIAGARM:**

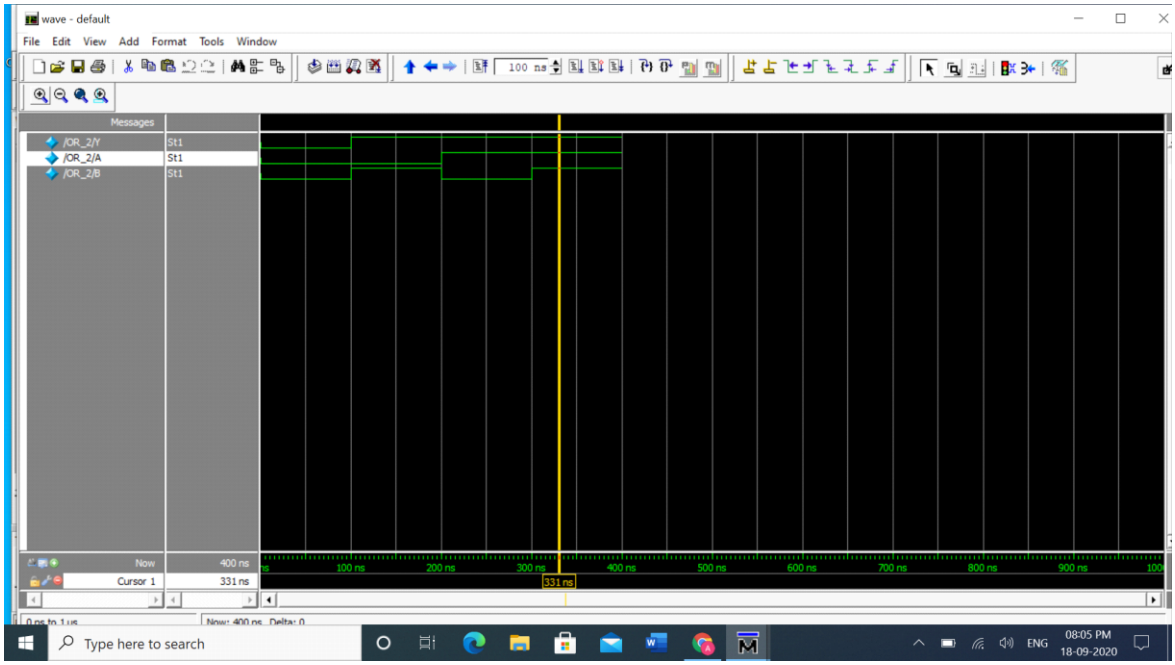



| A | B | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

CODE:




WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/OR_2/Y
/OR_2/A
/OR_2/B
St1
St1
St1
Now
400 ns
Cursor 1
331 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
Type here to search
ENG
08:05 PM
18-09-2020

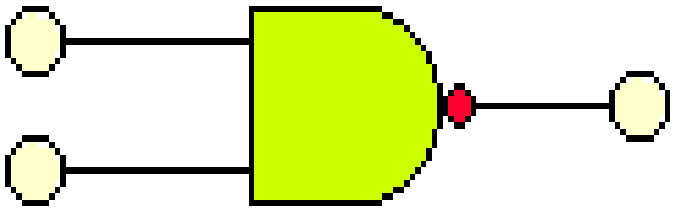
# EXPERIMENT:D

**AIM: Design UNIVERSAL GATES using gate level modeling .**

**SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).**

**A) – NAND GATE:**

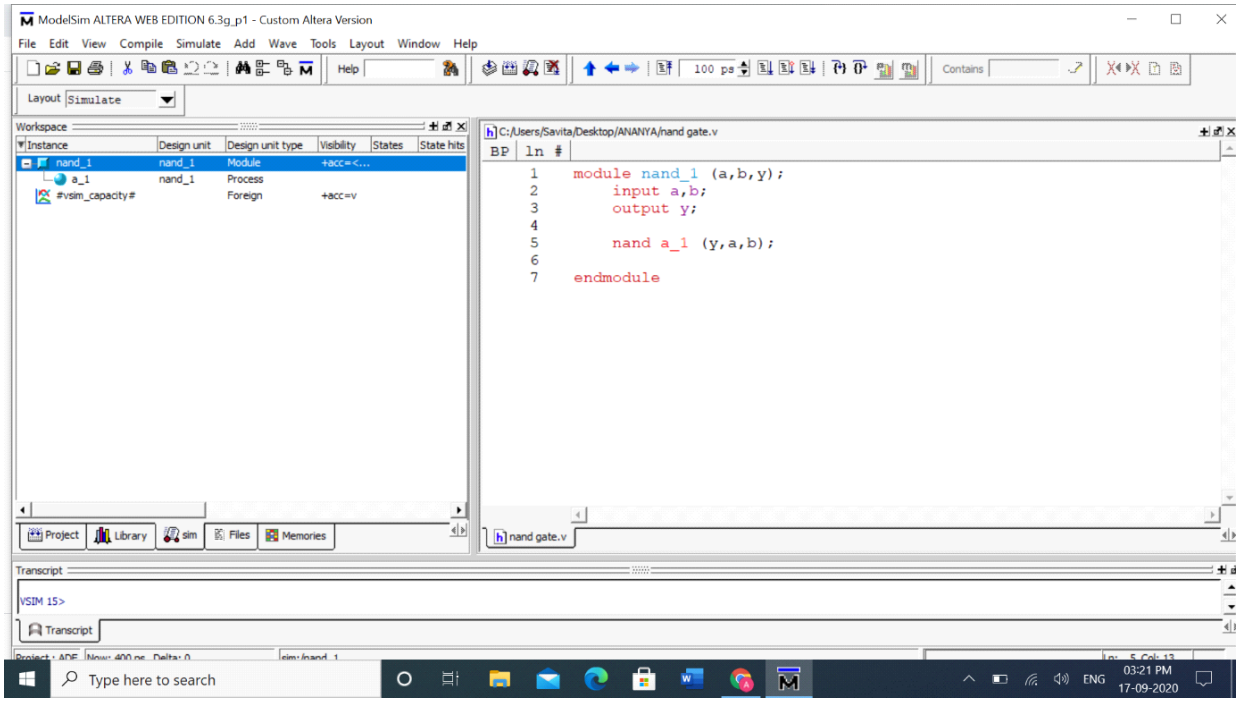
**LOGIC DIAGARM:**



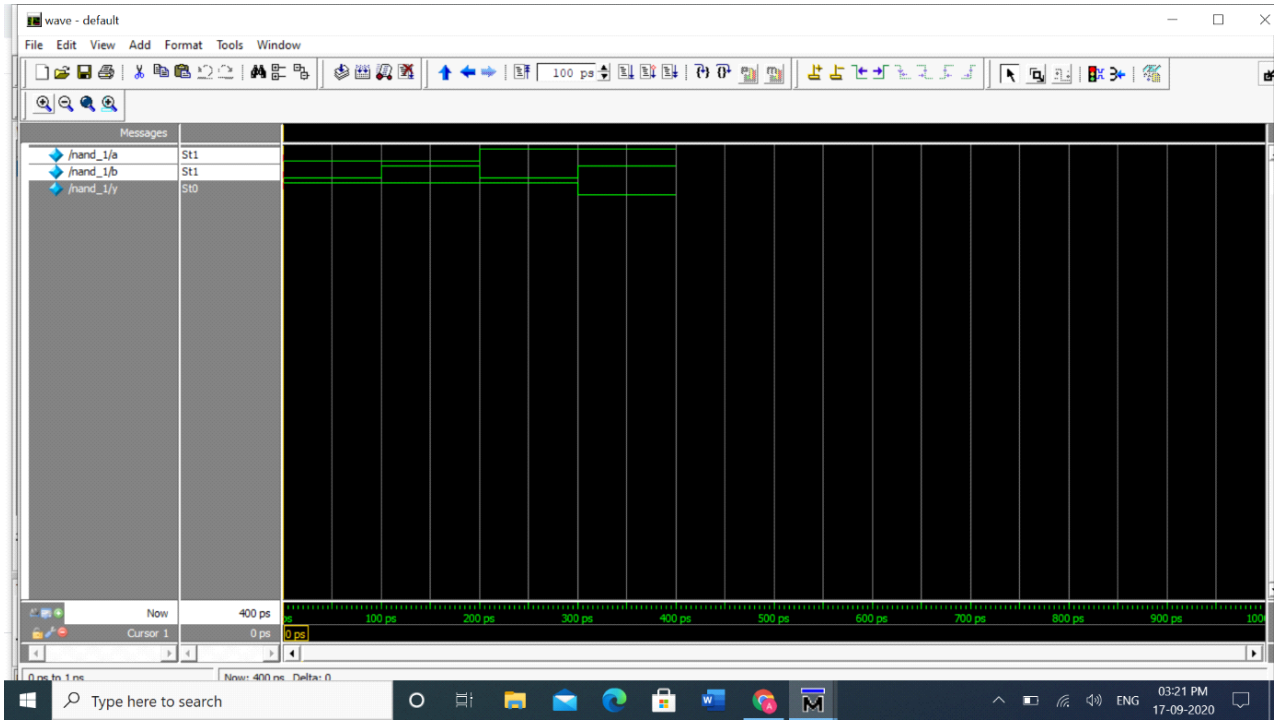
**TRUTH TABLE:**

| Input | | Output |
|---|---|---|
| A | B | Y= $\overline{A.B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**CODE:**

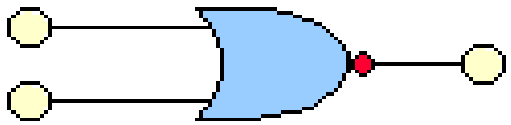

ModelSim ALTERA WEB EDITION 6.3g_p1 - Custom Altera Version
File Edit View Compile Simulate Add Wave Tools Layout Window Help
Workspace
Instance Design unit Design unit type Visibility States State hits
nand_1 nand_1 Module +acc=<...
a_1 nand_1 Process
#vsim_capacity# Foreign +acc=v
C:/Users/Savita/Desktop/ANANYA/nand gate.v
BP ln #
1 module nand_1 (a,b,y);
2 input a,b;
3 output y;
4
5 nand a_1 (y,a,b);
6
7 endmodule
Project Library sim Files Memories
nand gate.v
Transcript
VSIM 15>
Transcript
Type here to search
ENG
03:21 PM
17-09-2020

## WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/nand_1/a St1
/nand_1/b St1
/nand_1/y St0
Now 400 ps
Cursor 1 0 ps
100 ps 200 ps 300 ps 400 ps 500 ps 600 ps 700 ps 800 ps 900 ps
Type here to search
ENG
03:21 PM
17-09-2020

**B) NOR:**

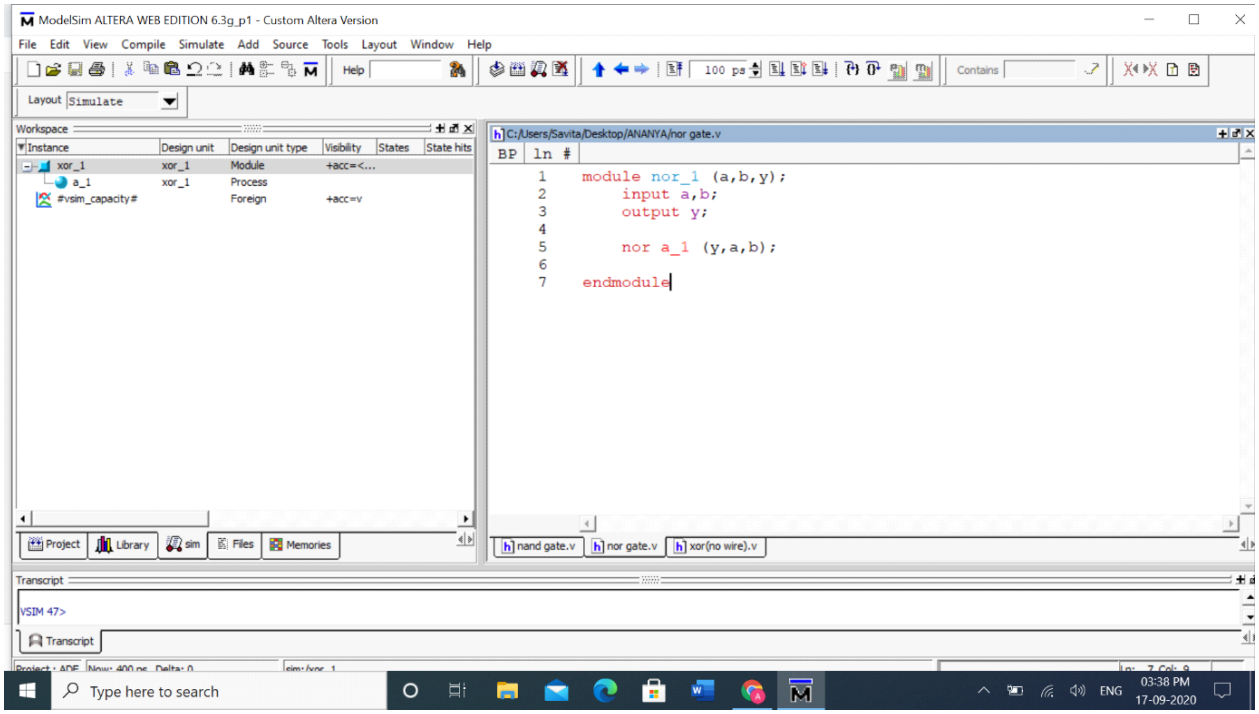
**LOGIC DIAGRAM:**



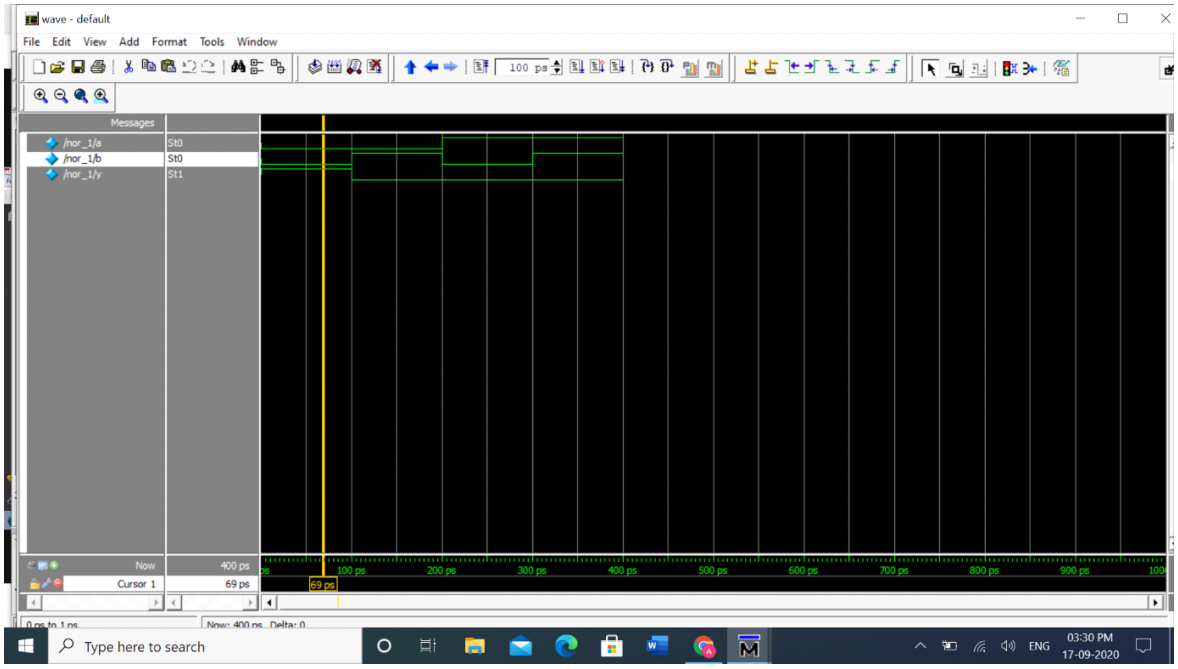
**TRUTH TABLE:**

| Input | | Output |
|---|---|---|
| A | B | $\overline{A+B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**CODE:**

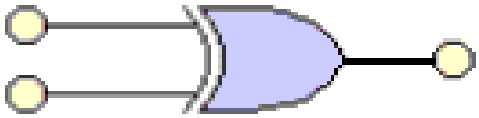

ModelSim ALTERA WEB EDITION 6.3g_p1 - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Window Help
Workspace
Instance Design unit Design unit type Visibility States State hits
xor_1 xor_1 Module +acc=<...
a_1 xor_1 Process
#vsim_capacity# Foreign +acc=v
C:/Users/Savita/Desktop/ANANYA/nor gate.v
BP ln #
1 module nor_1 (a,b,y);
2 input a,b;
3 output y;
4
5 nor a_1 (y,a,b);
6
7 endmodule
Project Library sim Files Memories
nand gate.v nor gate.v xor(no wire).v
Transcript
VSIM 47>
Transcript
Type here to search
ENG
03:38 PM
17-09-2020

## WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/nor_1/a St0
/nor_1/b St0
/nor_1/y St1
Now 400 ps
Cursor 1 69 ps
100 ps 200 ps 300 ps 400 ps 500 ps 600 ps 700 ps 800 ps 900 ps
Type here to search
ENG
03:30 PM
17-09-2020

**C) -EX_OR GATE:**

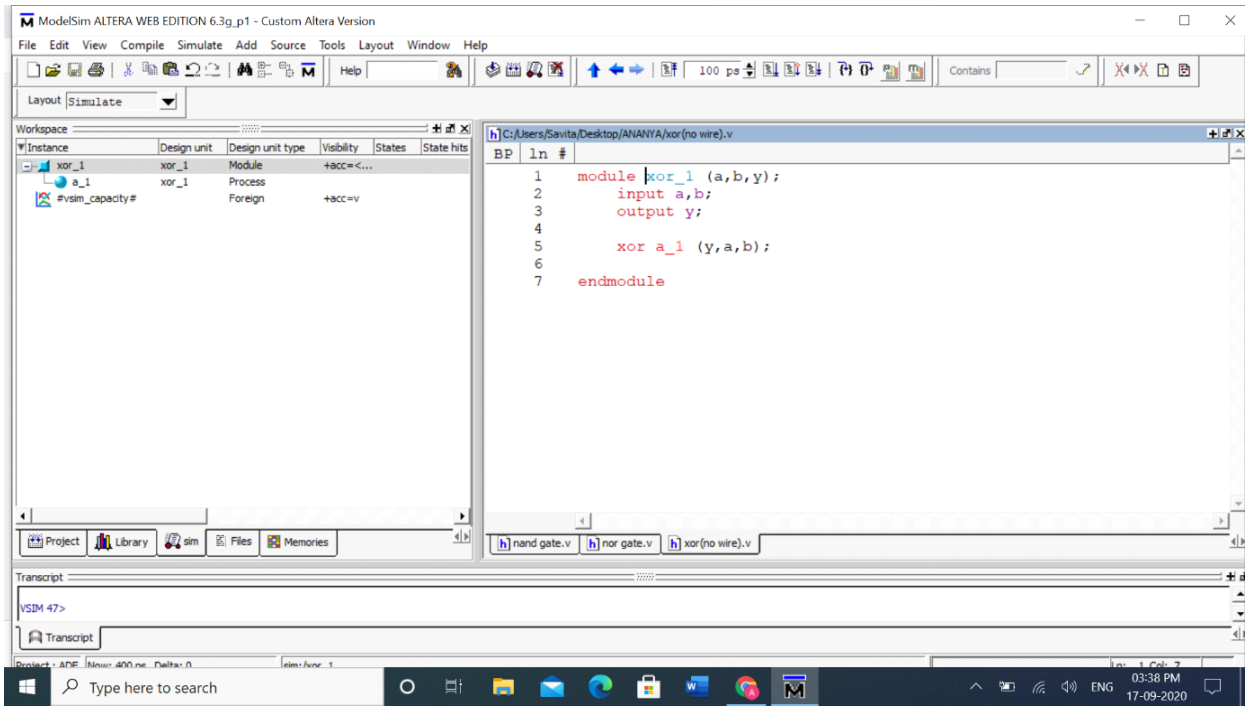
**LOGIC DIAGRAM:**



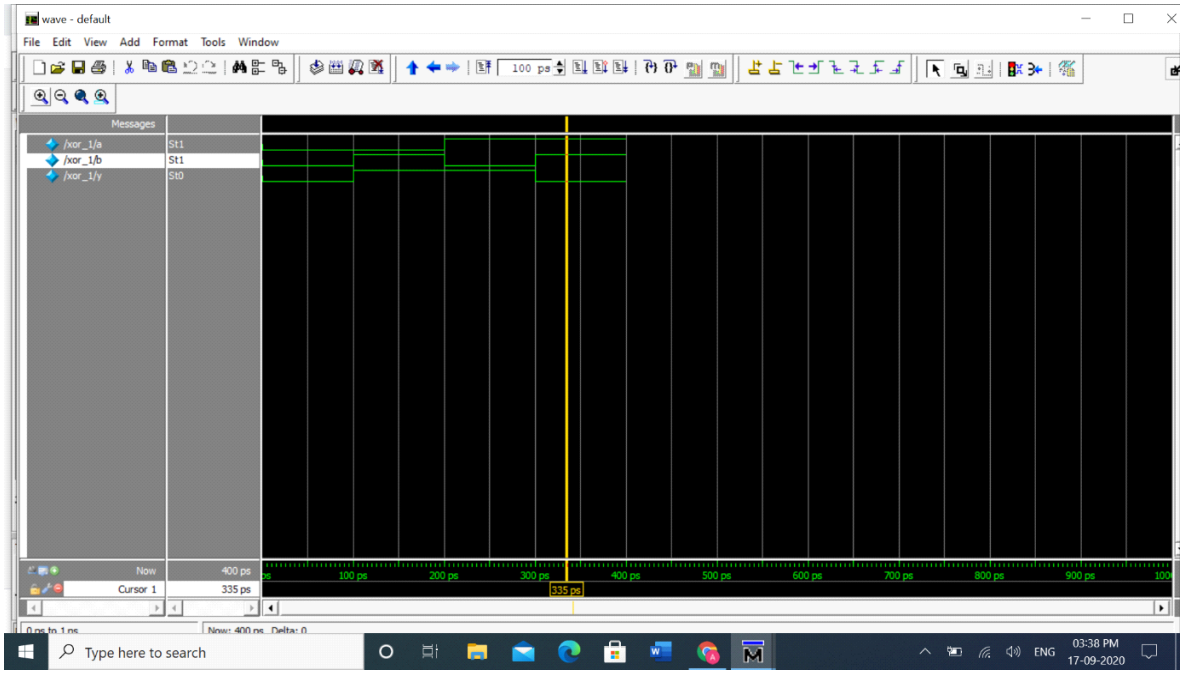
**TRUTH TABLE:**

| XOR Truth Table | | |
|---|---|---|
| **A** | **B** | **Q** |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**CODE:**

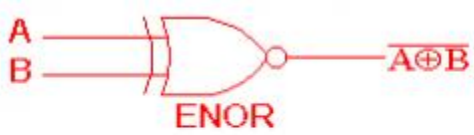


**WAVEFORM:**



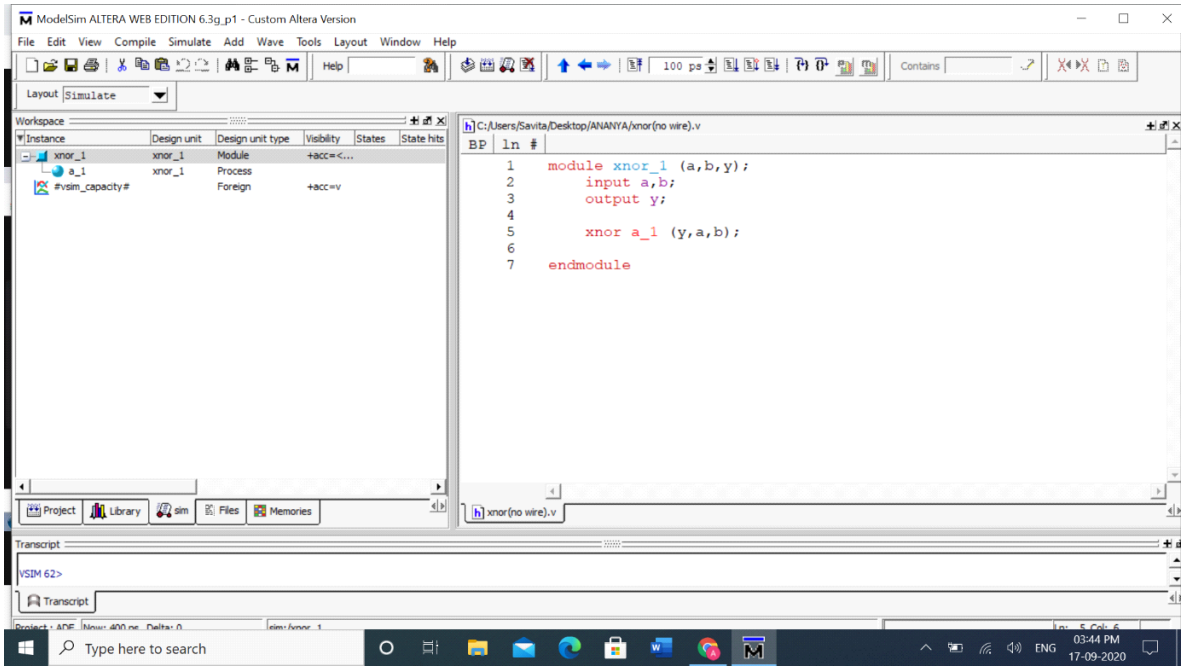

**D) – EX_NOR GATE:**

**LOGIC DIAGRAM:**

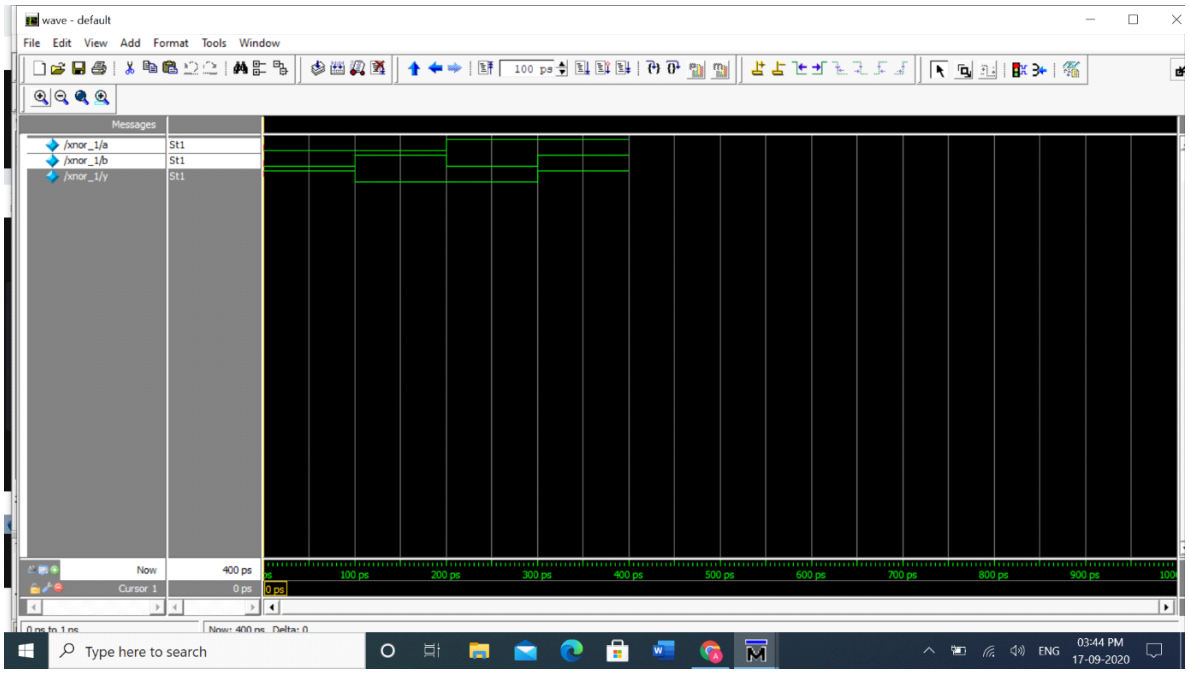



| 2 Input EXNOR gate | | |
|---|---|---|
| A | B | $\overline{A \oplus B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

## CODE:




## WAVEFORM:



# EXPERIMENT:E

**AIM: Design EX_OR GATE using gate level modeling with wire syntax .**

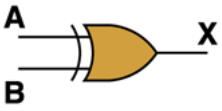
**SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).**

**LOGIC DIAGRAM:**

**Boolean Expression**

$$X = A \oplus B$$

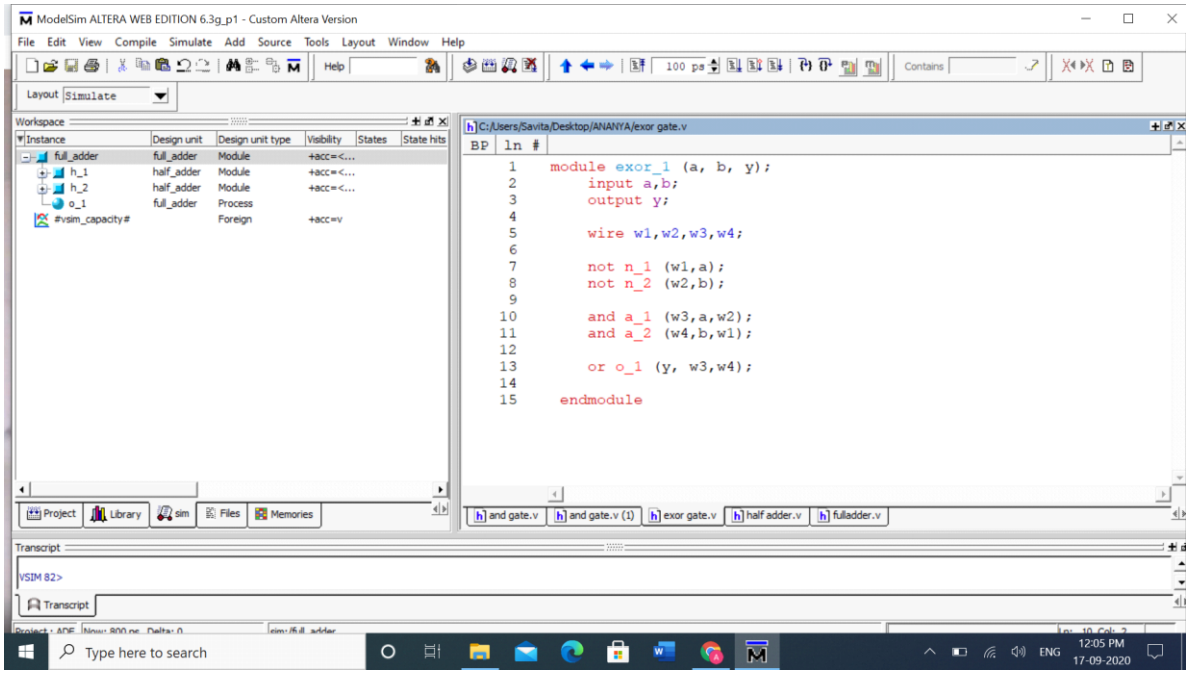
**Logic Diagram Symbol**



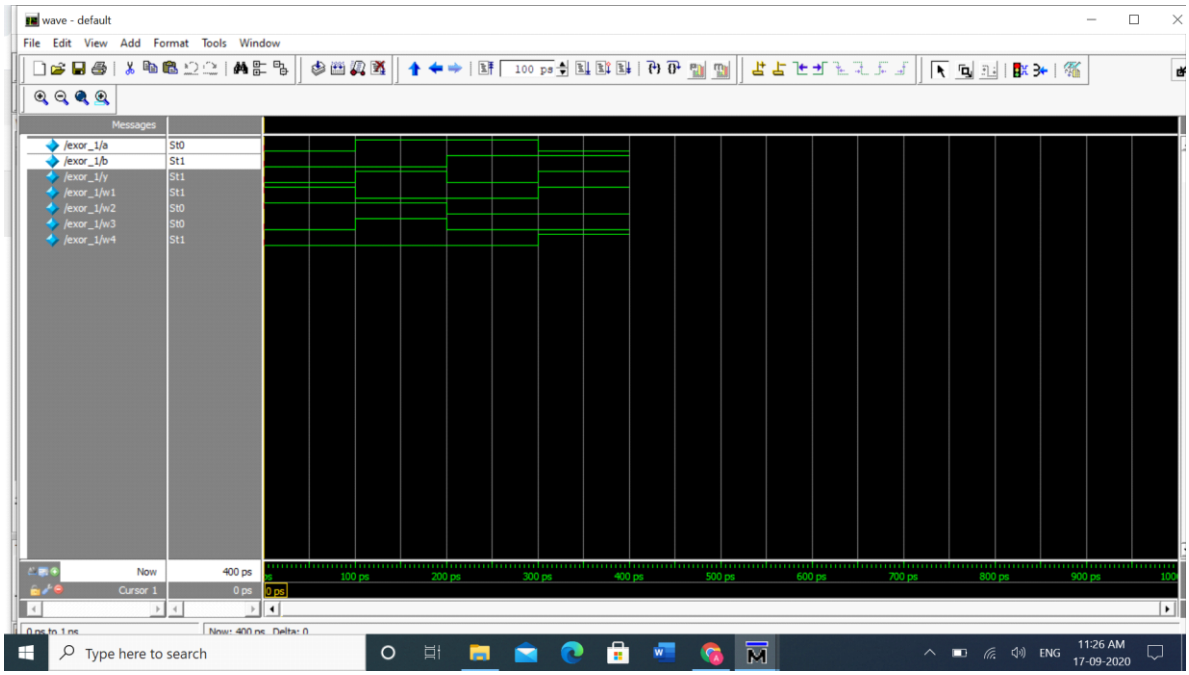

**Truth Table**

| A | B | X |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**CODE:**



**WAVEFORM:**

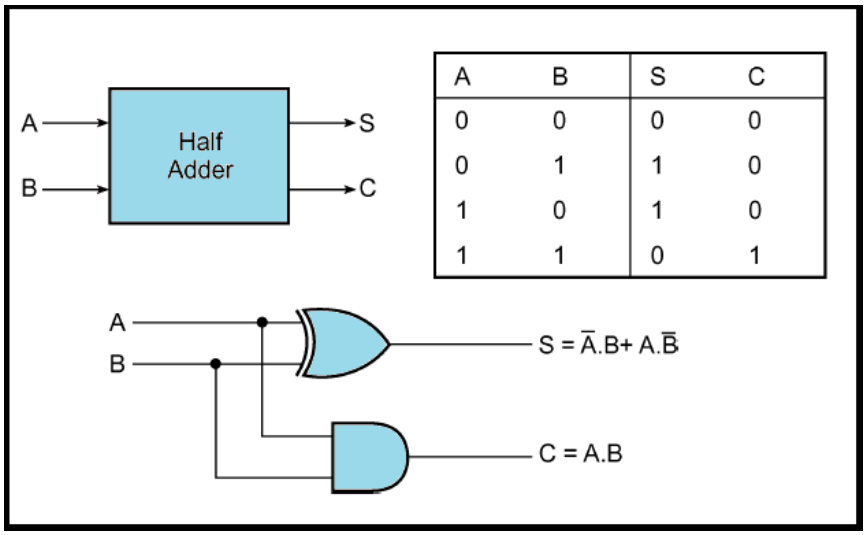

wave - default
File Edit View Add Format Tools Window
Messages
/exor_1/a
/exor_1/b
/exor_1/y
/exor_1/w1
/exor_1/w2
/exor_1/w3
/exor_1/w4
St0
St1
St1
St1
St0
St0
St1
Now
400 ps
Cursor 1
0 ps
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
Type here to search
ENG
11:26 AM
17-09-2020

# EXPERIMENT:F

**AIM: Design HALF ADDER using gate level modeling .**

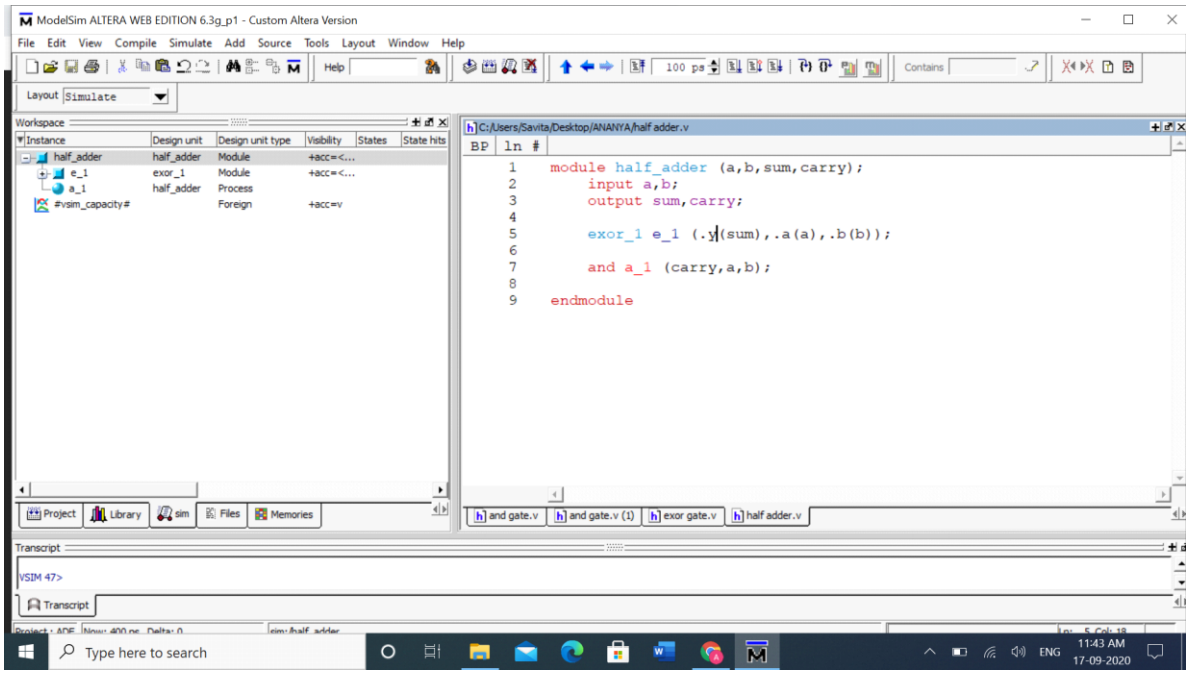
**SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).**

**LOGIC DIAGRAM:**

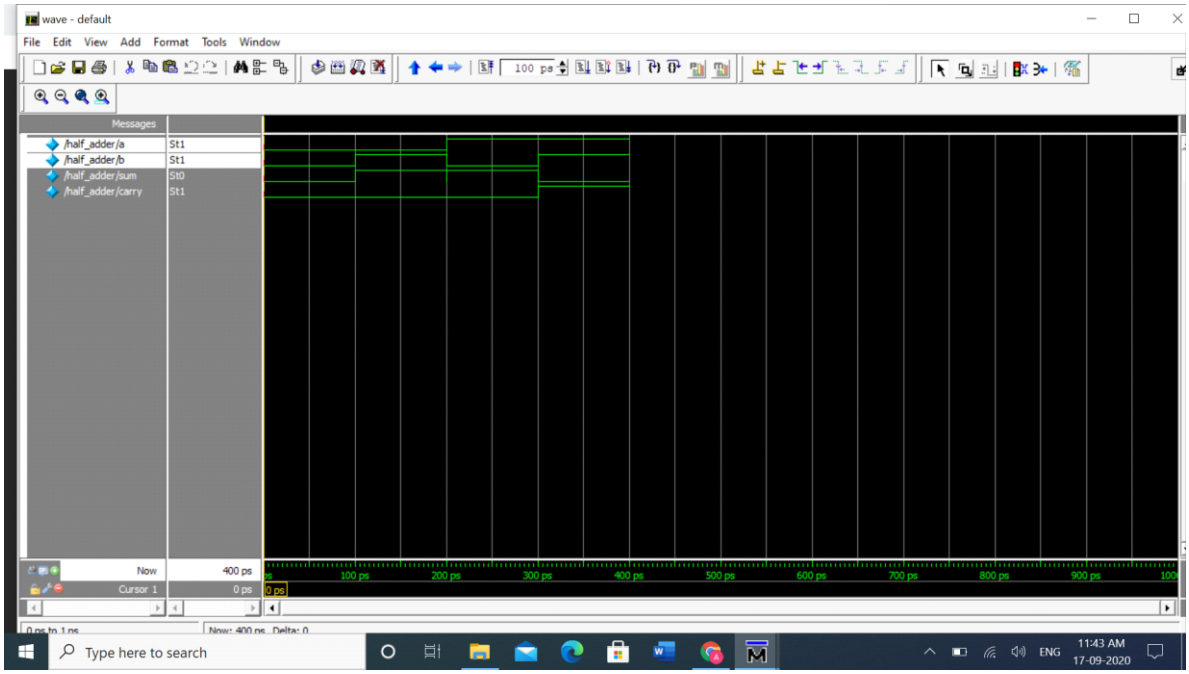



| A | B | S | C |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**CODE:**




**WAVEFORM:**

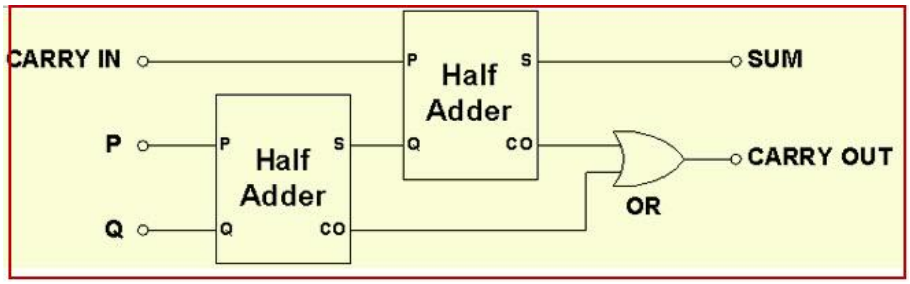

wave - default
File Edit View Add Format Tools Window
Messages
/half_adder/a
/half_adder/b
/half_adder/sum
/half_adder/carry
St1
St1
St0
St1
Now
400 ps
Cursor 1
0 ps
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
Type here to search
ENG
11:43 AM
17-09-2020

# EXPERIMENT:G

**AIM: Design FULL ADDER using gate level modeling .**

**SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).**

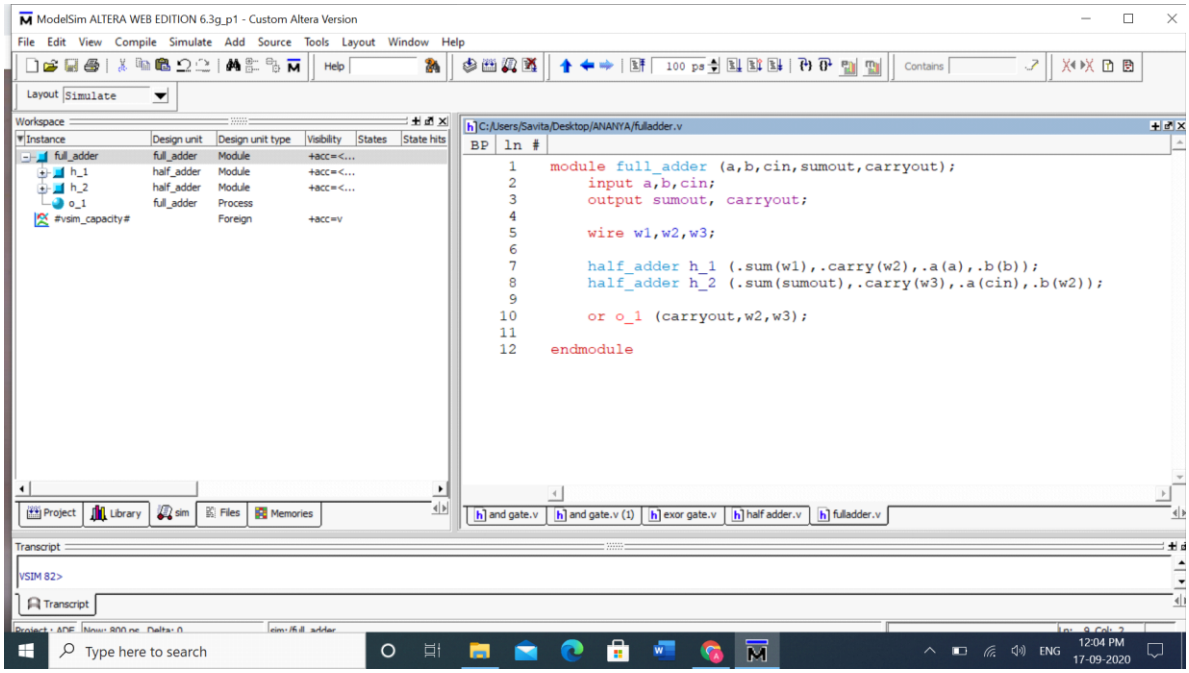
**LOGIC DIAGRAM:**



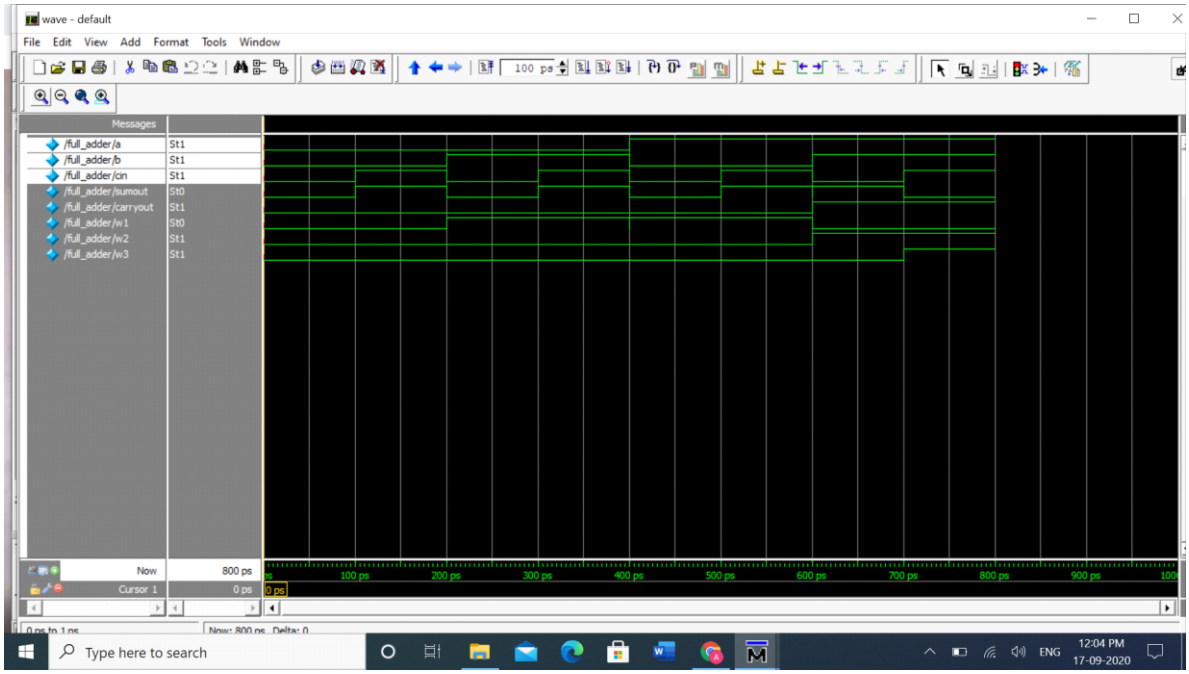

**TRUTH TABLE:**

| Input | | | Output | |
|---|---|---|---|---|
| A | B | Cin | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**CODE:**



**WAVEFORM:**

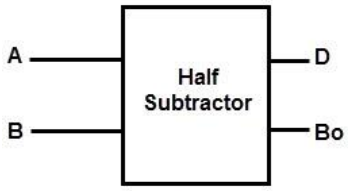



# EXPERIMENT:H

**AIM: Design HALF SUBTRACTOR using gate level modeling .**

**SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).**

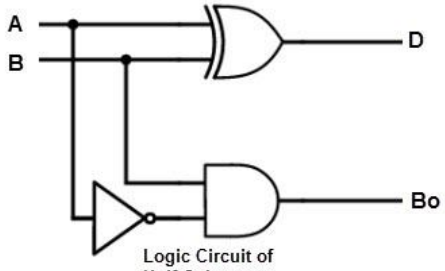
**LOGIC DIAGRAM:**




Block Diagram

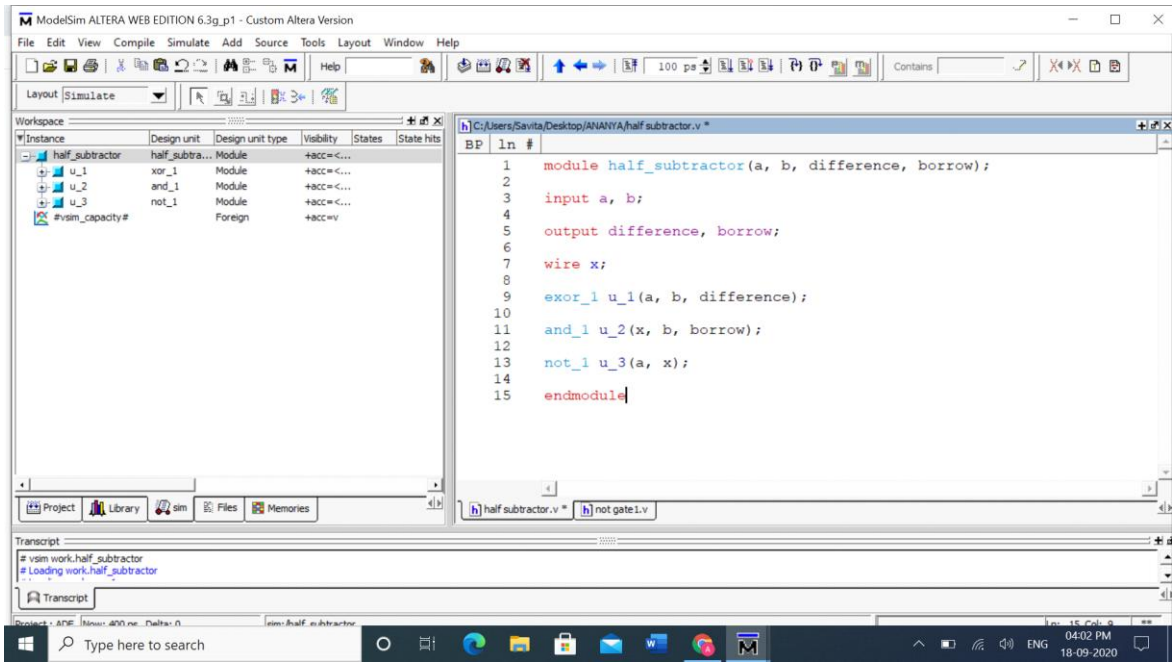
| A | B | D | $B_0$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

Truth Table

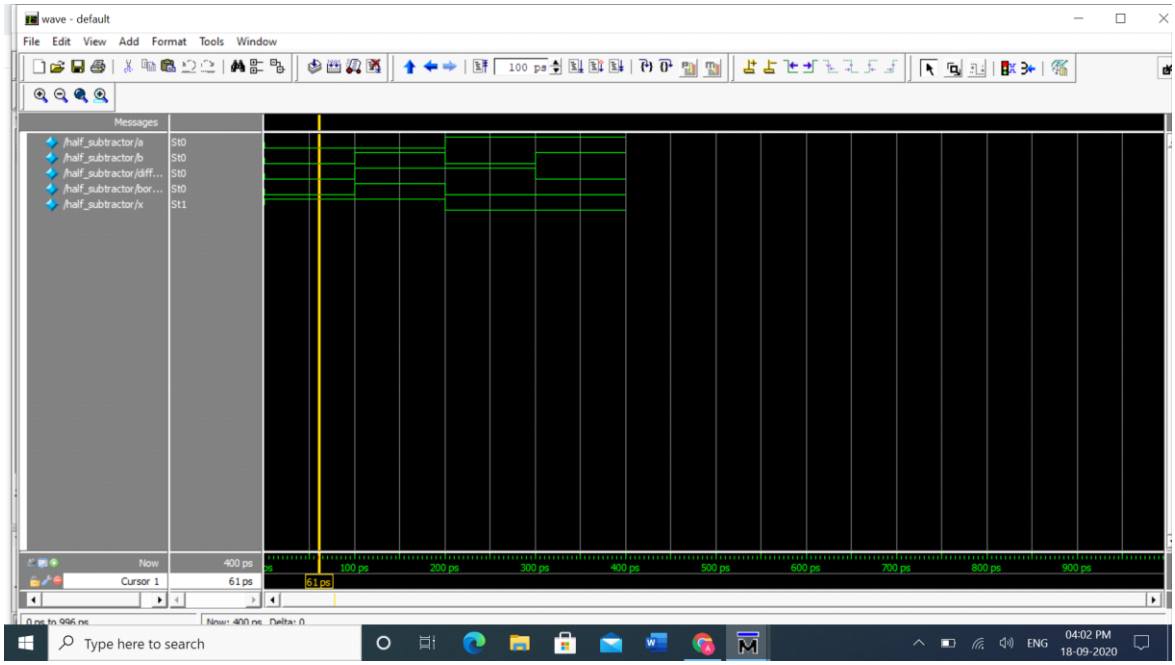



Logic Circuit of
Half Subtractor

**CODE:**




**WAVEFORM:**



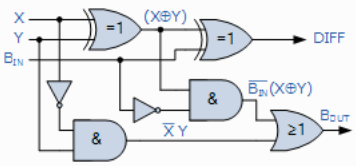

# EXPERIMENT:I

**AIM: Design FULL SUBTRACTOR using gate level modeling .**

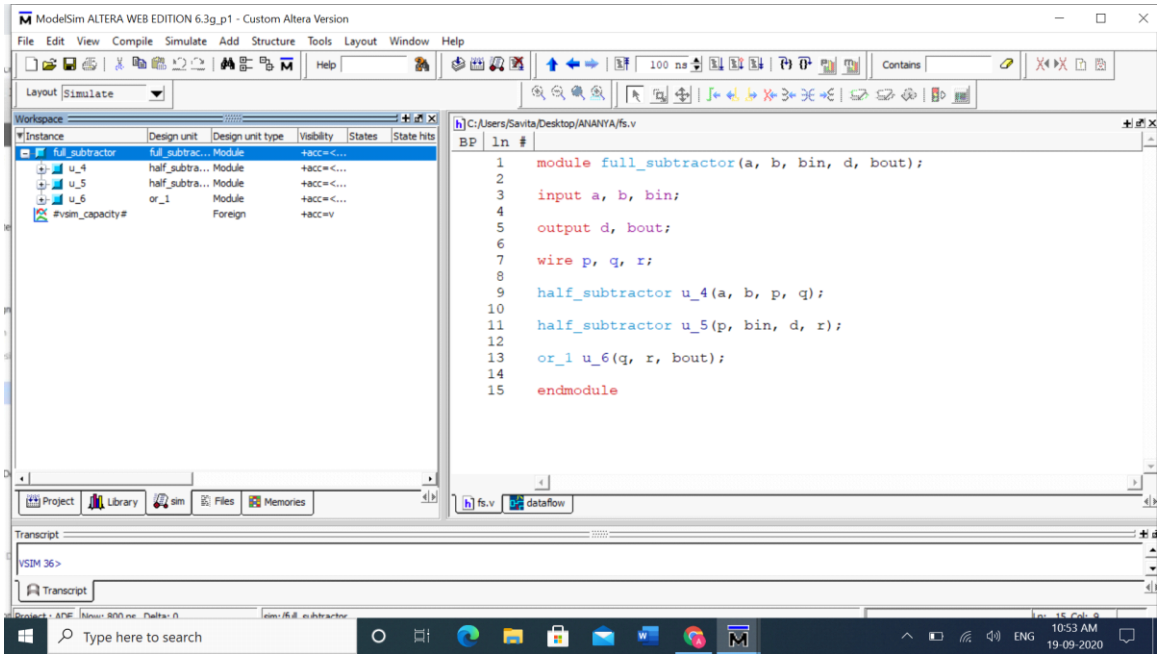
**SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).**

**LOGIC DIAGRAM:**

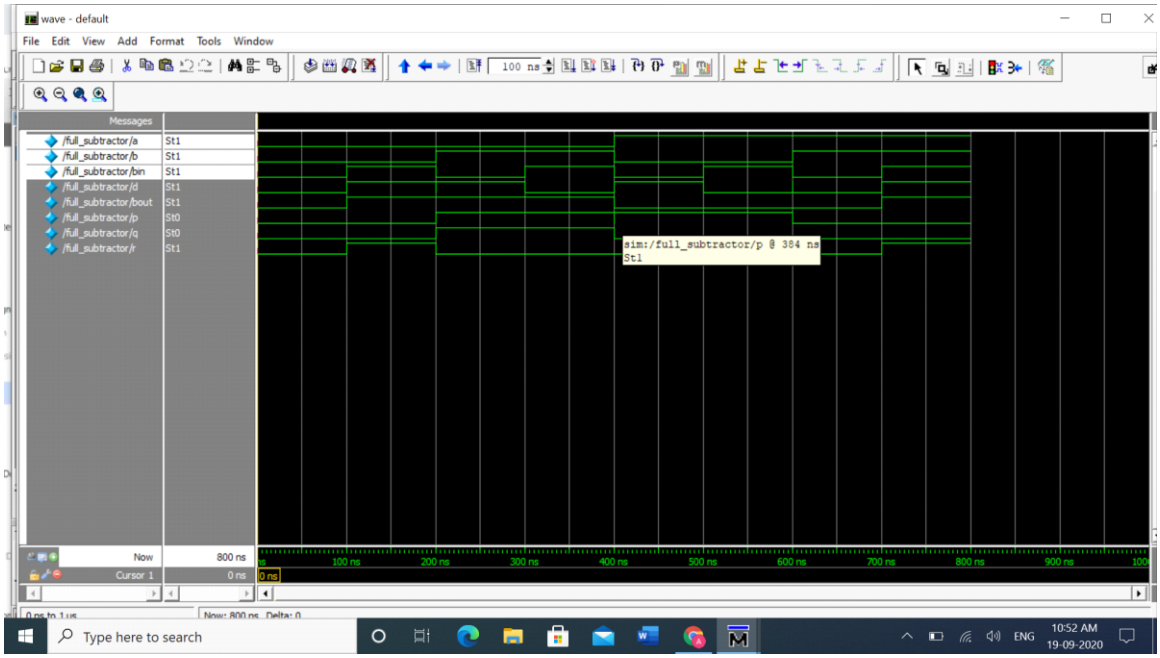
| Symbol | Truth Table | | | | |
|---|---|---|---|---|---|
| | B-in | Y | X | Diff. | B-out |
| | 0 | 0 | 0 | 0 | 0 |
| | 0 | 0 | 1 | 1 | 1 |
| | 0 | 1 | 0 | 1 | 1 |
| | 0 | 1 | 1 | 0 | 1 |
| | 1 | 0 | 0 | 1 | 0 |
| | 1 | 0 | 1 | 0 | 0 |
| | 1 | 1 | 0 | 0 | 0 |
| | 1 | 1 | 1 | 1 | 1 |




**CODE:**


ModelSim ALTERA WEB EDITION 6.3g_p1 - Custom Altera Version
File Edit View Compile Simulate Add Structure Tools Layout Window Help
Workspace
Instance Design unit Design unit type Visibility States State hits
full_subtractor full_subtrac... Module +acc=<...
u_4 half_subtra... Module +acc=<...
u_5 half_subtra... Module +acc=<...
u_6 or_1 Module +acc=<...
#vsim_capacity# Foreign +acc=v
C:/Users/Savita/Desktop/ANANYA/fs.v
1 module full_subtractor(a, b, bin, d, bout);
2
3 input a, b, bin;
4
5 output d, bout;
6
7 wire p, q, r;
8
9 half_subtractor u_4(a, b, p, q);
10
11 half_subtractor u_5(p, bin, d, r);
12
13 or_1 u_6(q, r, bout);
14
15 endmodule
Project Library sim Files Memories
fs.v dataflow
Transcript
VSIM 36>
Transcript
Type here to search
ENG
10:53 AM
19-09-2020

**WAVEFORM:**

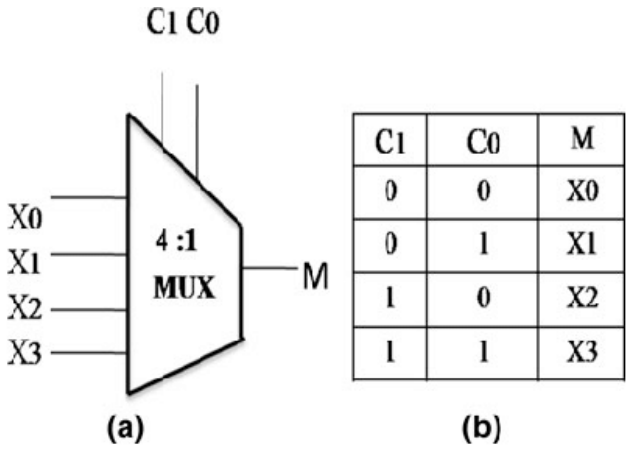

wave - default
File Edit View Add Format Tools Window
Messages
/full_subtractor/a St1
/full_subtractor/b St1
/full_subtractor/bin St1
/full_subtractor/d St1
/full_subtractor/bout St1
/full_subtractor/p St0
/full_subtractor/q St0
/full_subtractor/r St1
sim:/full_subtractor/p @ 384 ns
St1
Now 800 ns
Cursor 1 0 ns
0 ns 100 ns 200 ns 300 ns 400 ns 500 ns 600 ns 700 ns 800 ns 900 ns
Type here to search
ENG
10:52 AM
19-09-2020

# EXPERIMENT:J

**AIM: Design 4-1 MULTIPLEXER using gate level modeling .**

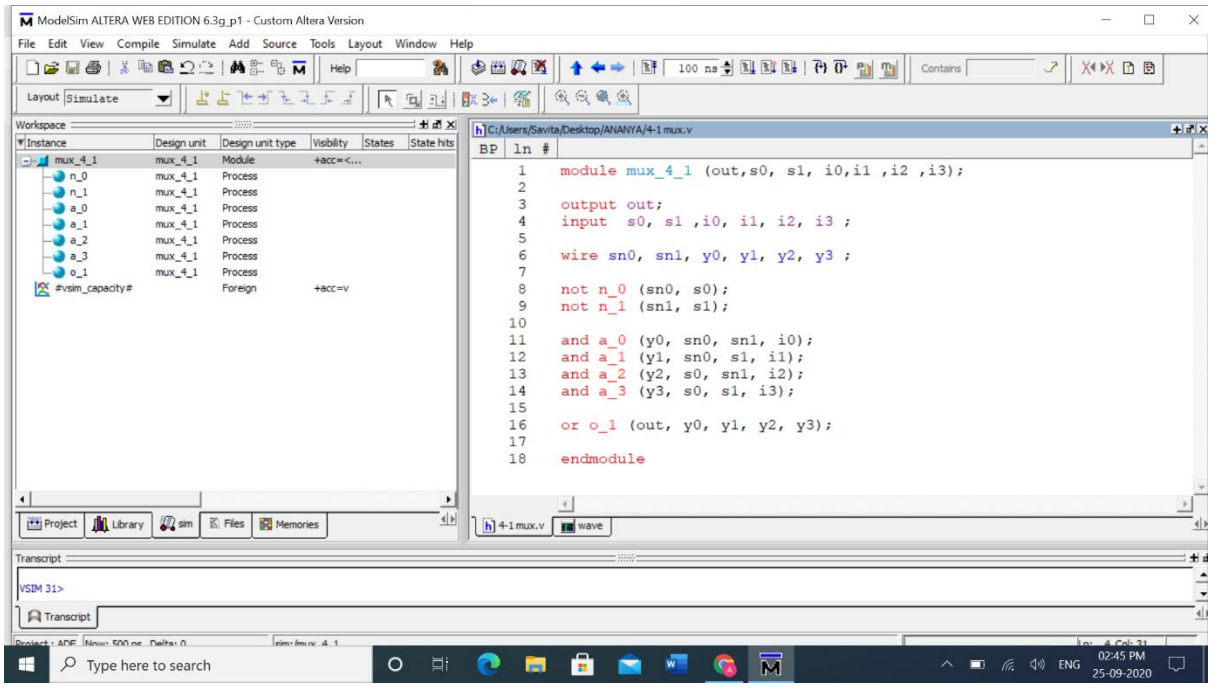
**SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).**

**LOGIC DIAGRAM:**

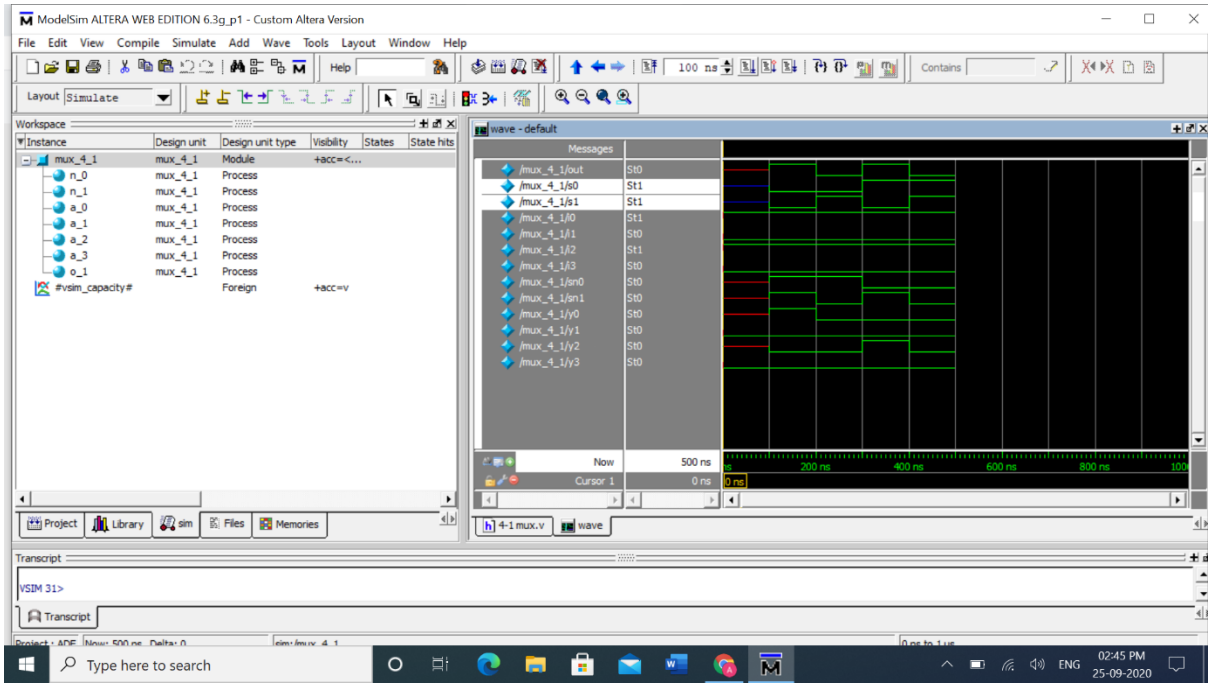



| C1 | C0 | M |
|---|---|---|
| 0 | 0 | X0 |
| 0 | 1 | X1 |
| 1 | 0 | X2 |
| 1 | 1 | X3 |

**CODE:**



## WAVEFORM:

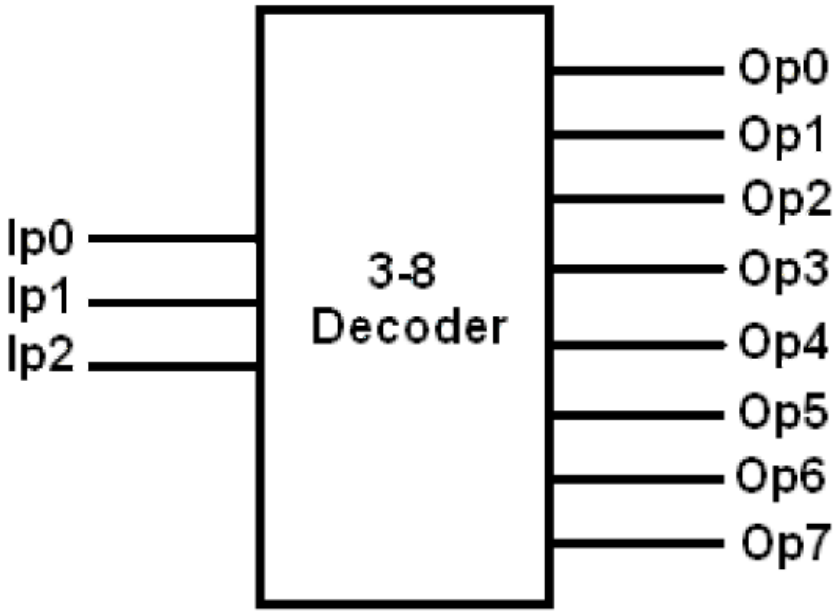

ModelSim ALTERA WEB EDITION 6.3g_p1 - Custom Altera Version
File Edit View Compile Simulate Add Wave Tools Layout Window Help
Workspace
Instance Design unit Design unit type Visibility States State hits
mux_4_1 mux_4_1 Module +acc=<...
n_0 mux_4_1 Process
n_1 mux_4_1 Process
a_0 mux_4_1 Process
a_1 mux_4_1 Process
a_2 mux_4_1 Process
a_3 mux_4_1 Process
o_1 mux_4_1 Process
#vsim_capacity# Foreign +acc=v
wave - default
Messages
/mux_4_1/out St0
/mux_4_1/s0 St1
/mux_4_1/s1 St1
/mux_4_1/i0 St1
/mux_4_1/i1 St0
/mux_4_1/i2 St1
/mux_4_1/i3 St0
/mux_4_1/sn0 St0
/mux_4_1/sn1 St0
/mux_4_1/y0 St0
/mux_4_1/y1 St0
/mux_4_1/y2 St0
/mux_4_1/y3 St0
Now 500 ns
Cursor 1 0 ns
200 ns 400 ns 600 ns 800 ns
Project Library sim Files Memories
4-1mux.v wave
Transcript
VSIM 31>
Transcript
Type here to search
ENG
02:45 PM
25-09-2020

# EXPERIMENT:k

**AIM: Design 3-8 DECODER using gate level modeling .**

**SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).**

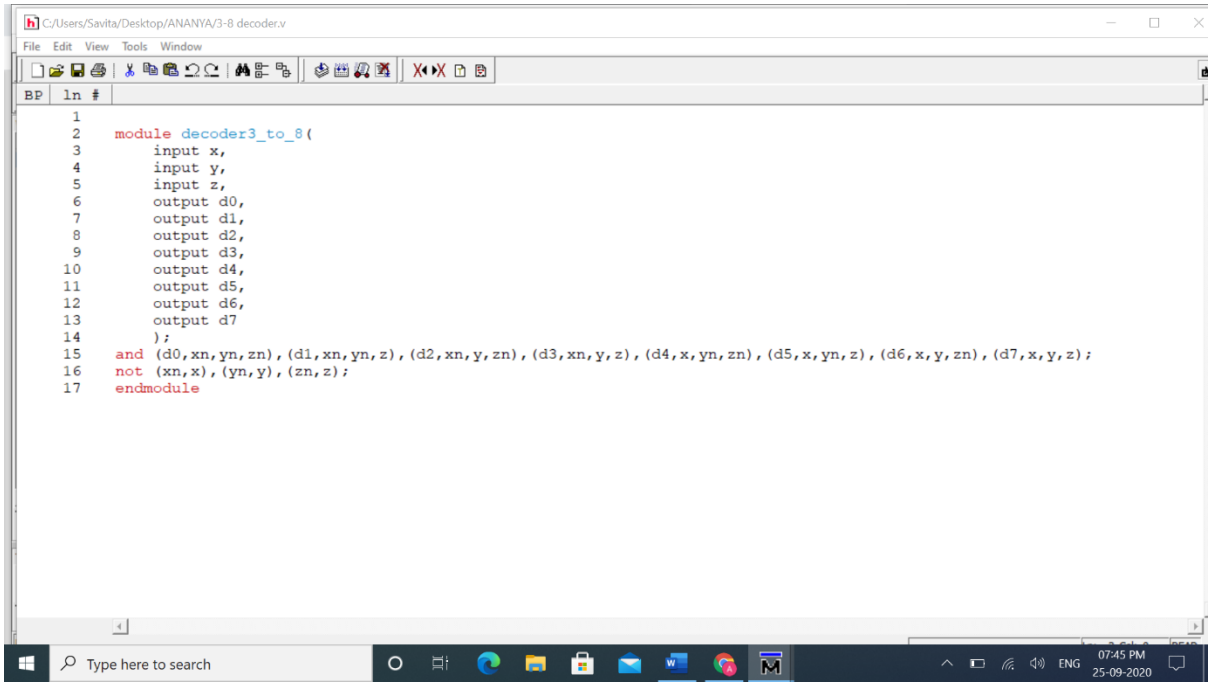
**LOGIC DIAGRAM:**




3 to 8 Line Decoder

| Inputs | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| x | y | z | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**CODE:**




**WAVEFORM:**