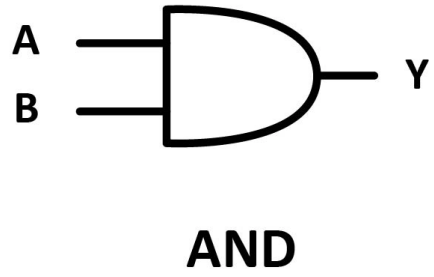
EXPERIMENT : GATE LEVEL MODELING.

AIM: Design AND GATE using gate level modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR(VERILOG).

LOGIC DIAGARM:

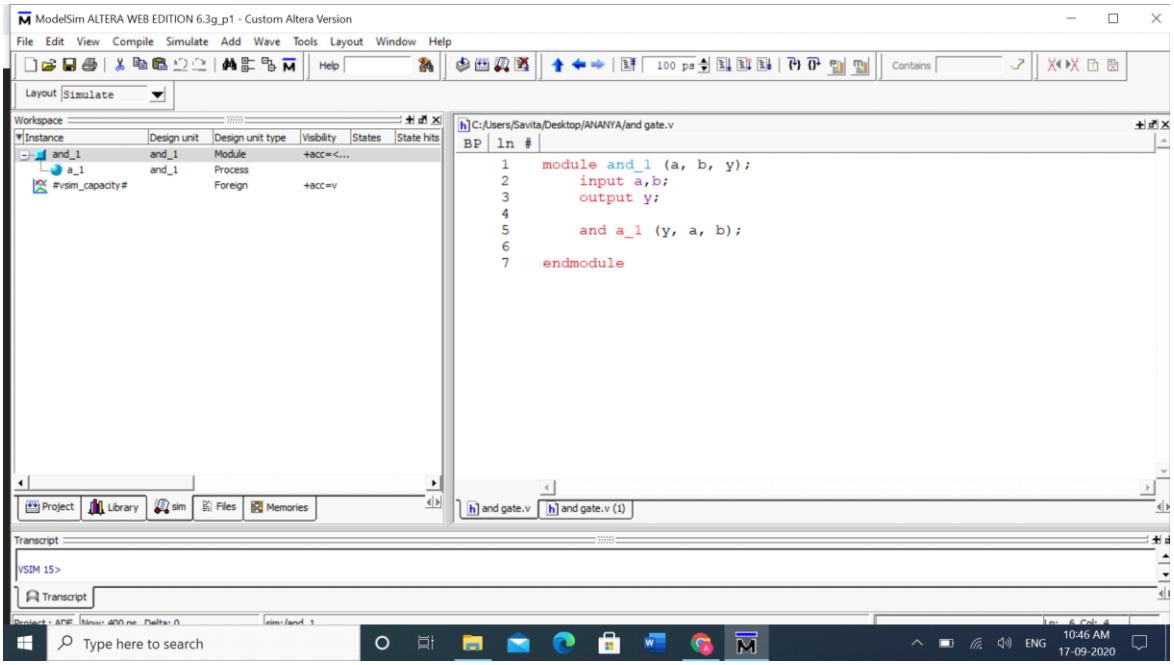
Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



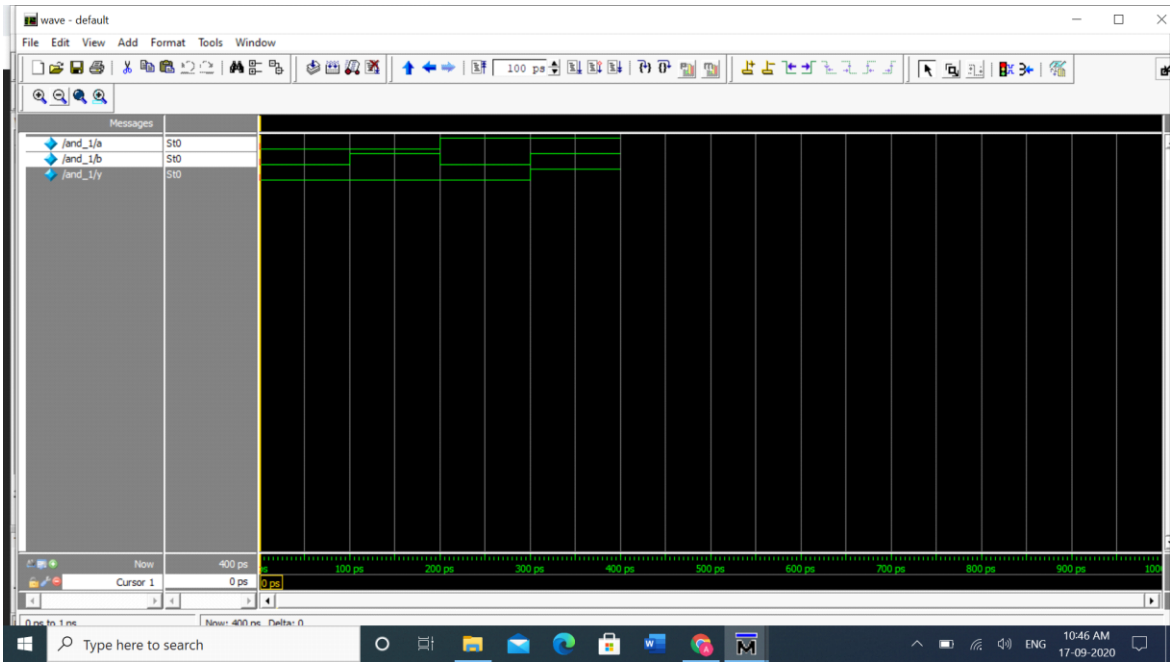
AND

Truth Table

CODE:



WAVEFORM:

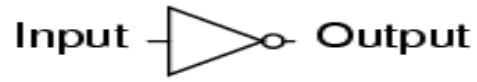


AIM: Design NOT GATE using gate level modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR(VERILOG).

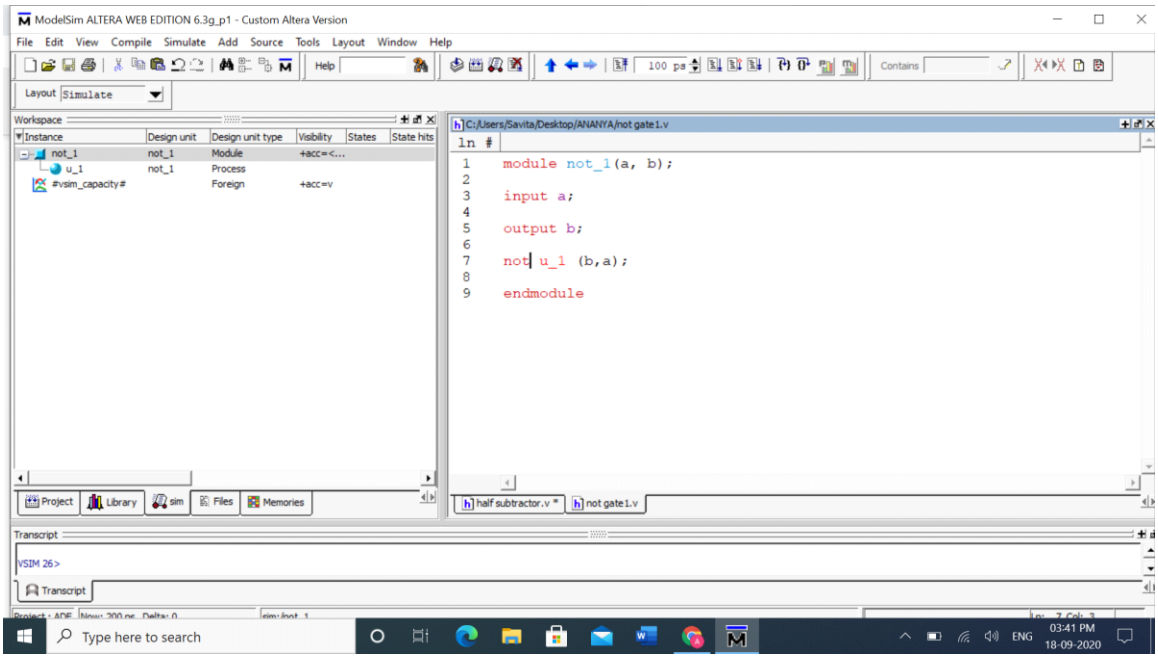
LOGIC DIAGARM:

NOT gate truth table

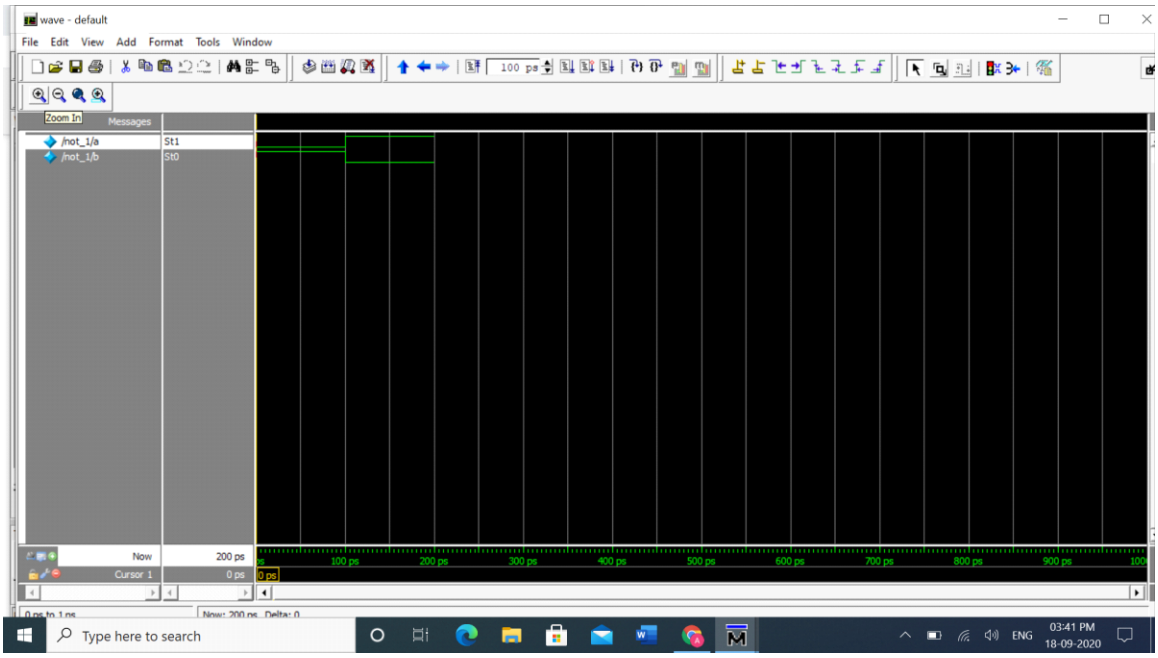


Input	Output
0	1
1	0

CODE:



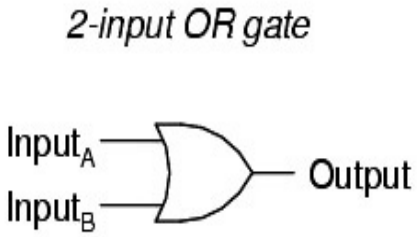
WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Zoom In
Messages
/not_1/a
/not_1/b
St1
St0
Now
200 ps
Cursor 1
0 ps
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
Type here to search
ENG
03:41 PM
18-09-2020

AIM: Design OR GATE using gate level modeling .

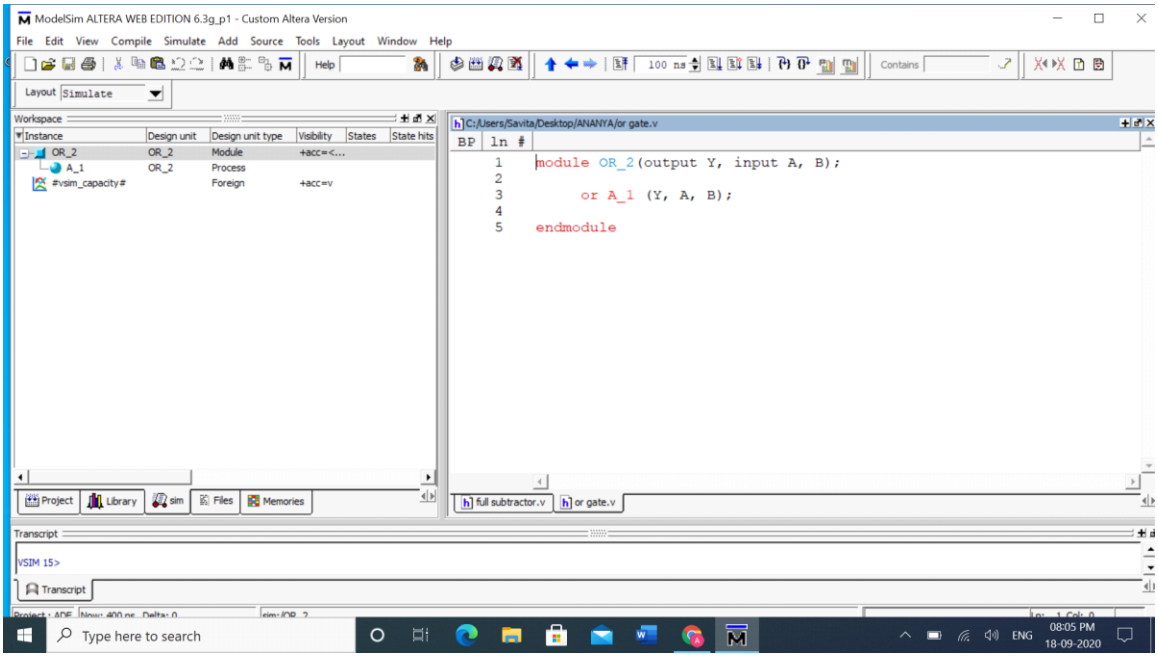
SOFTWARE REQUIRED: MODEL SIMULATOR(VERILOG).

LOGIC DIAGARM:

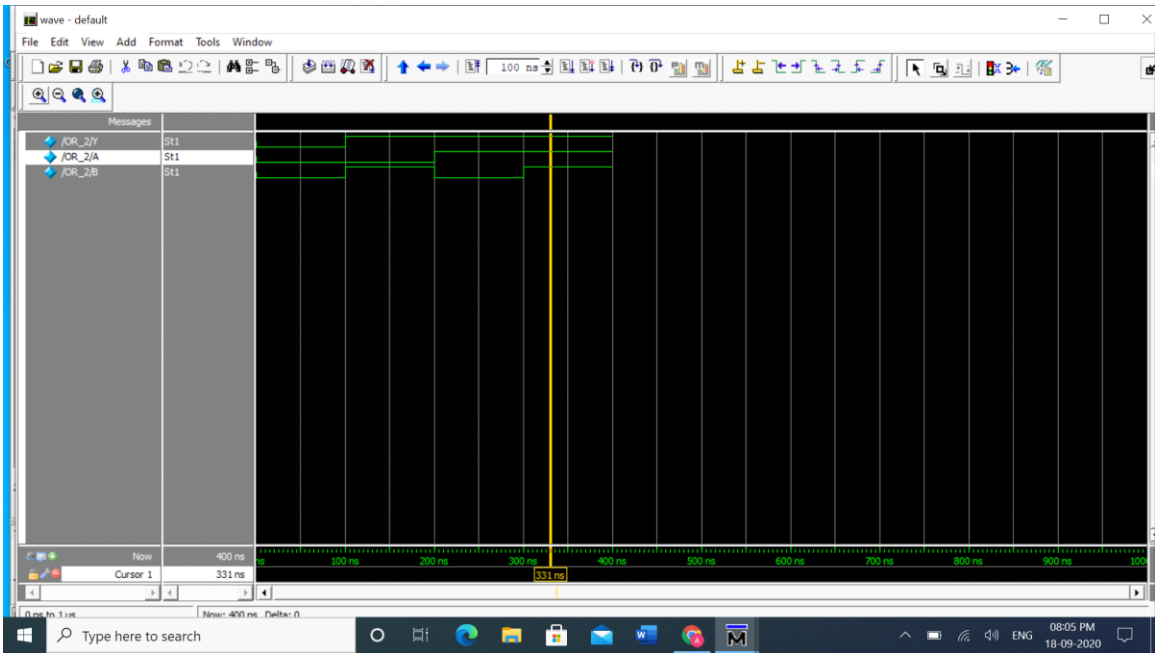


A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

CODE:



WAVEFORM:

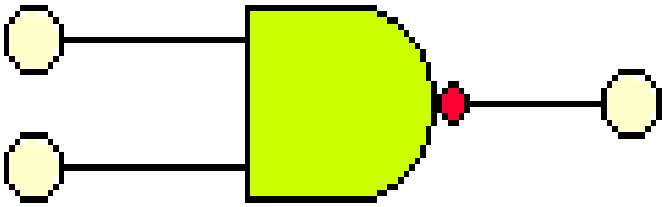

wave - default
File Edit View Add Format Tools Window
Messages
/OR_2/Y
/OR_2/A
/OR_2/B
St1
Now
400 ns
Cursor 1
331 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
Type here to search
ENG
08:05 PM
18-09-2020

AIM: Design UNIVERSAL GATES using gate level modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

A) – NAND GATE:

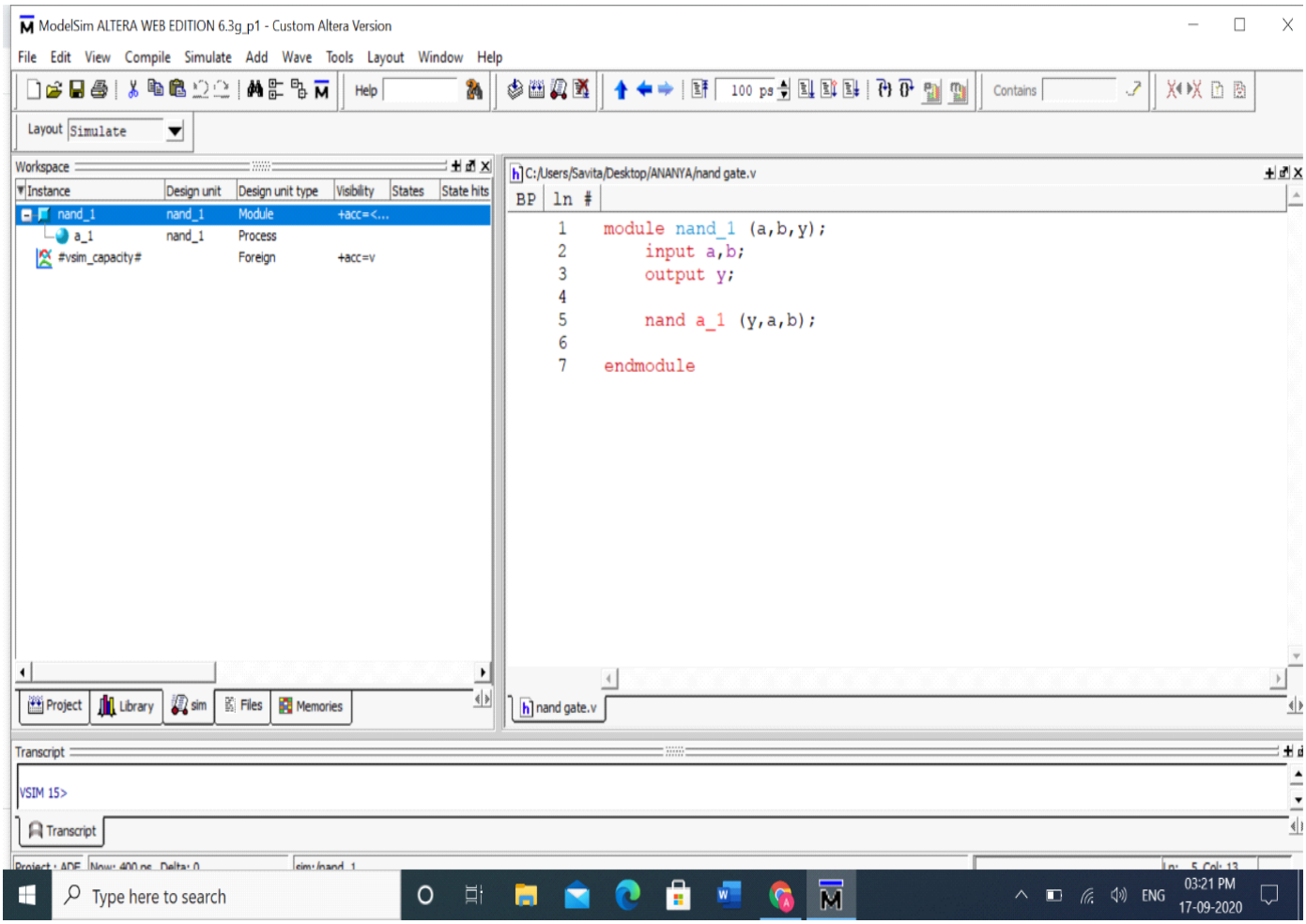
LOGIC DIAGARM:



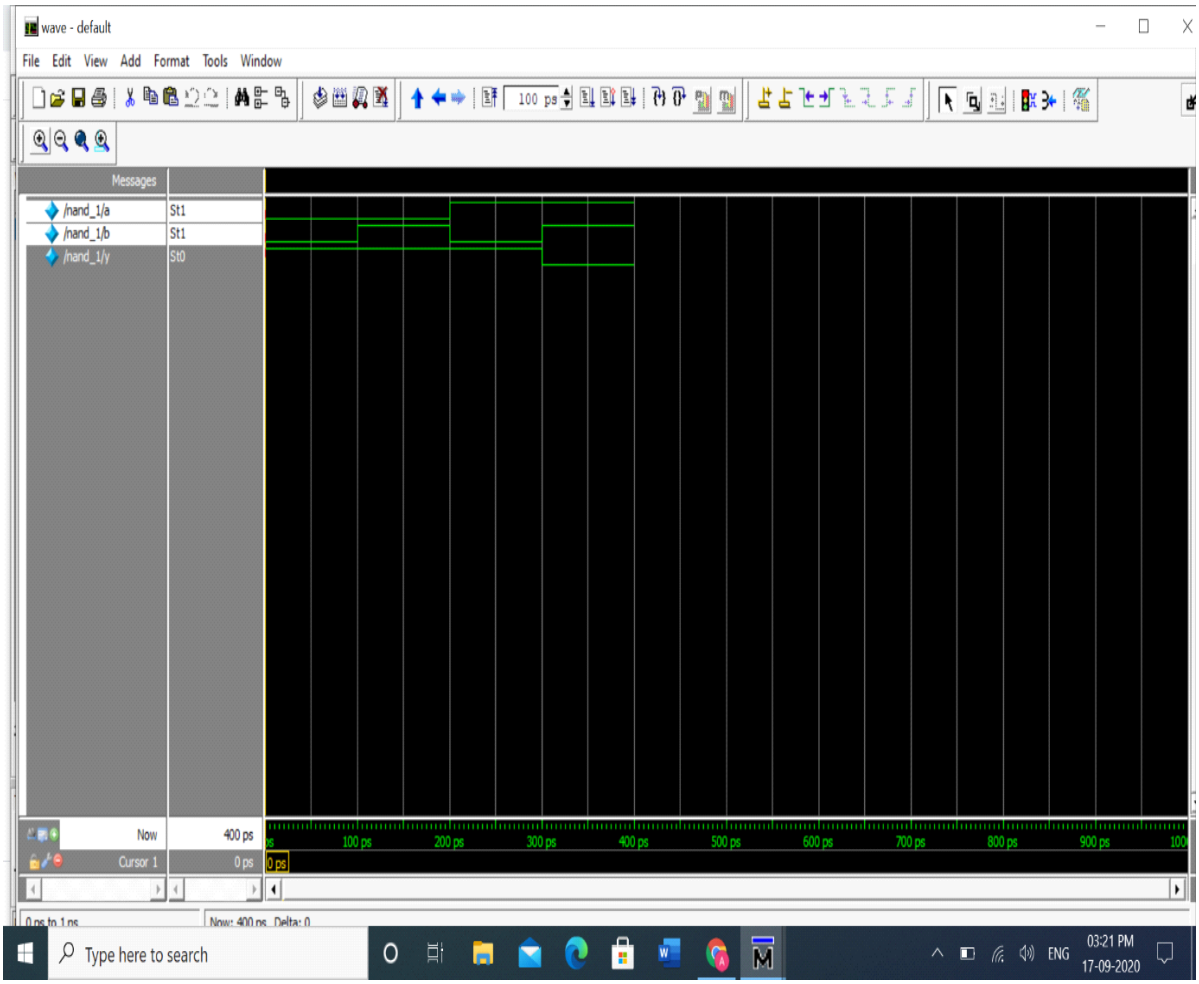
TRUTH TABLE:

Input		Output
A	B	Y= $\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

CODE:

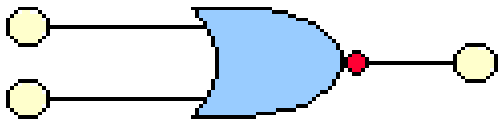

ModelSim ALTERA WEB EDITION 6.3g_p1 - Custom Altera Version
File Edit View Compile Simulate Add Wave Tools Layout Window Help
Layout Simulate
Workspace
Instance Design unit Design unit type Visibility States State hits
nand_1 nand_1 Module +acc=<...
a_1 nand_1 Process
#vsim_capacity# Foreign +acc=v
Project Library sim Files Memories
C:/Users/Savita/Desktop/ANANYA/nand gate.v
BP ln #
1 module nand_1 (a,b,y);
2 input a,b;
3 output y;
4
5 nand a_1 (y,a,b);
6
7 endmodule
nand gate.v
Transcript
VSIM 15>
Transcript
Type here to search
ENG
03:21 PM
17-09-2020

WAVEFORM:



B) NOR:

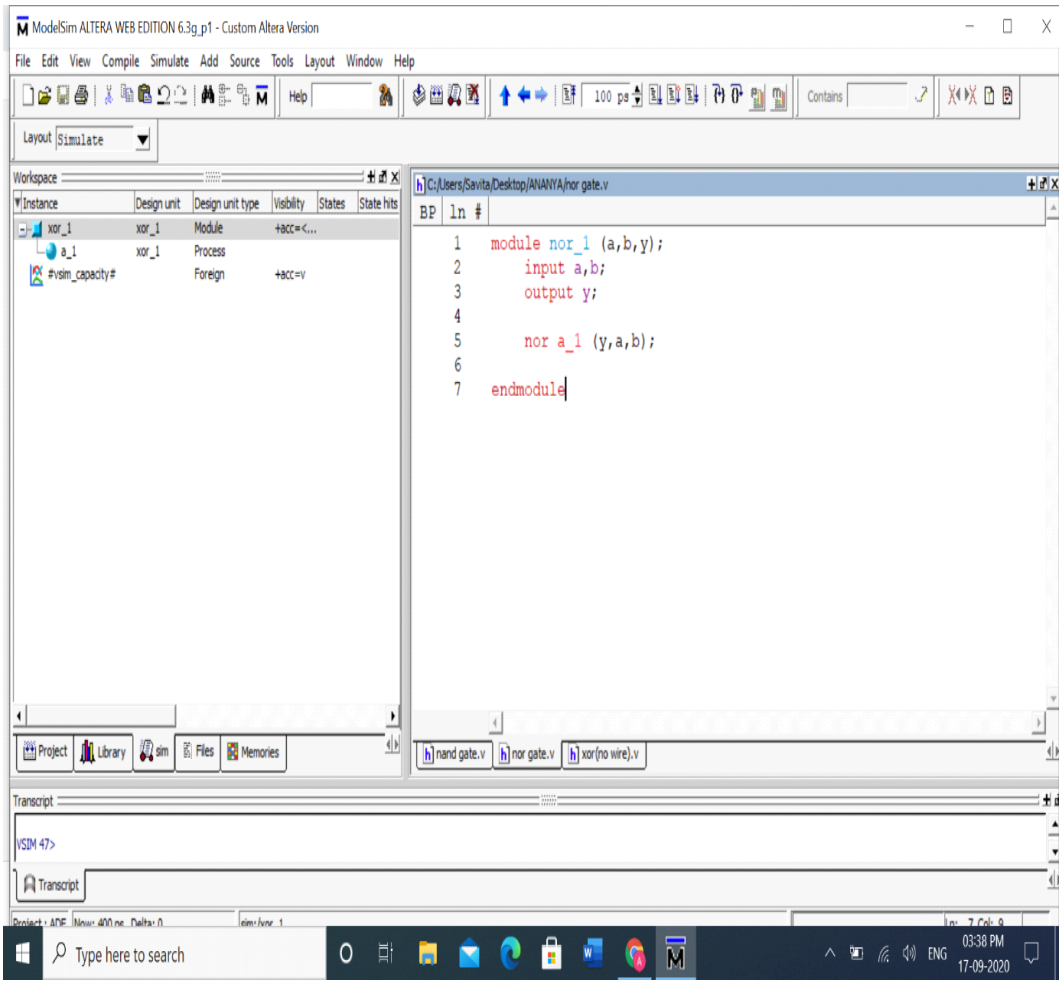
LOGIC DIAGRAM:



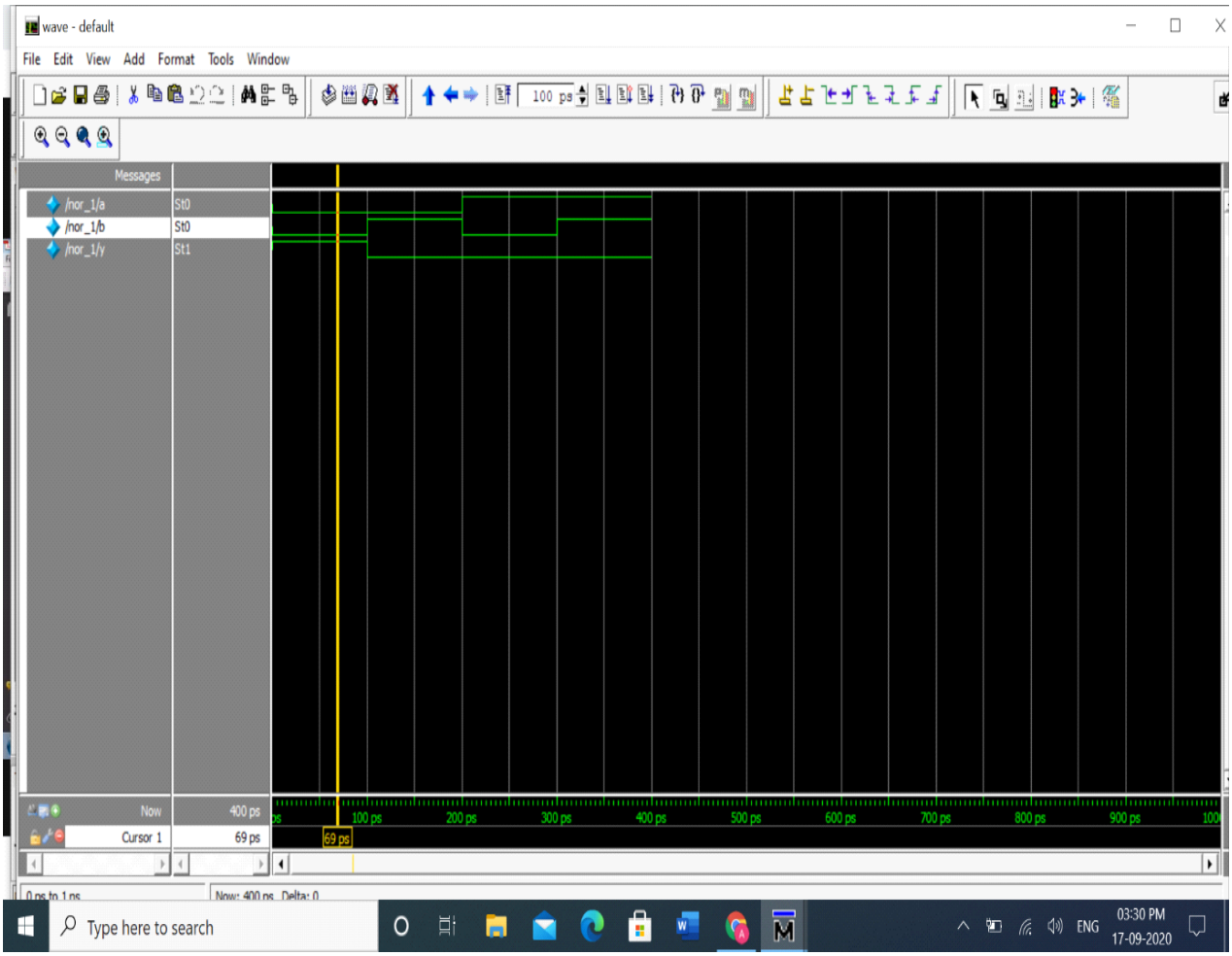
TRUTH TABLE:

Input		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

CODE:

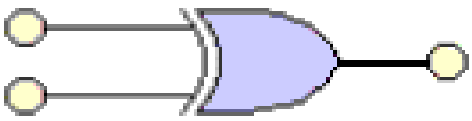


WAVEFORM:



C) -EX_OR GATE:

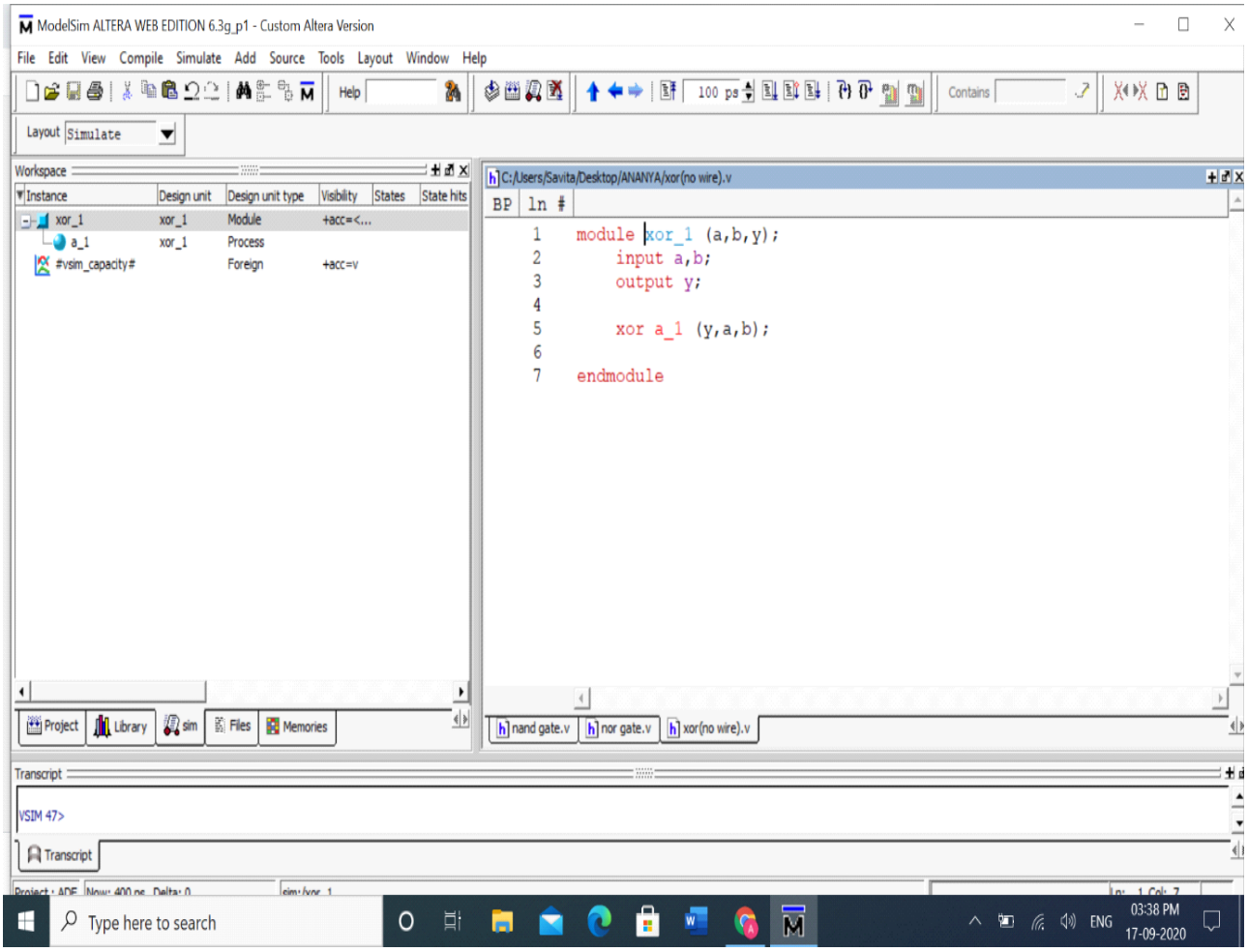
LOGIC DIAGRAM:



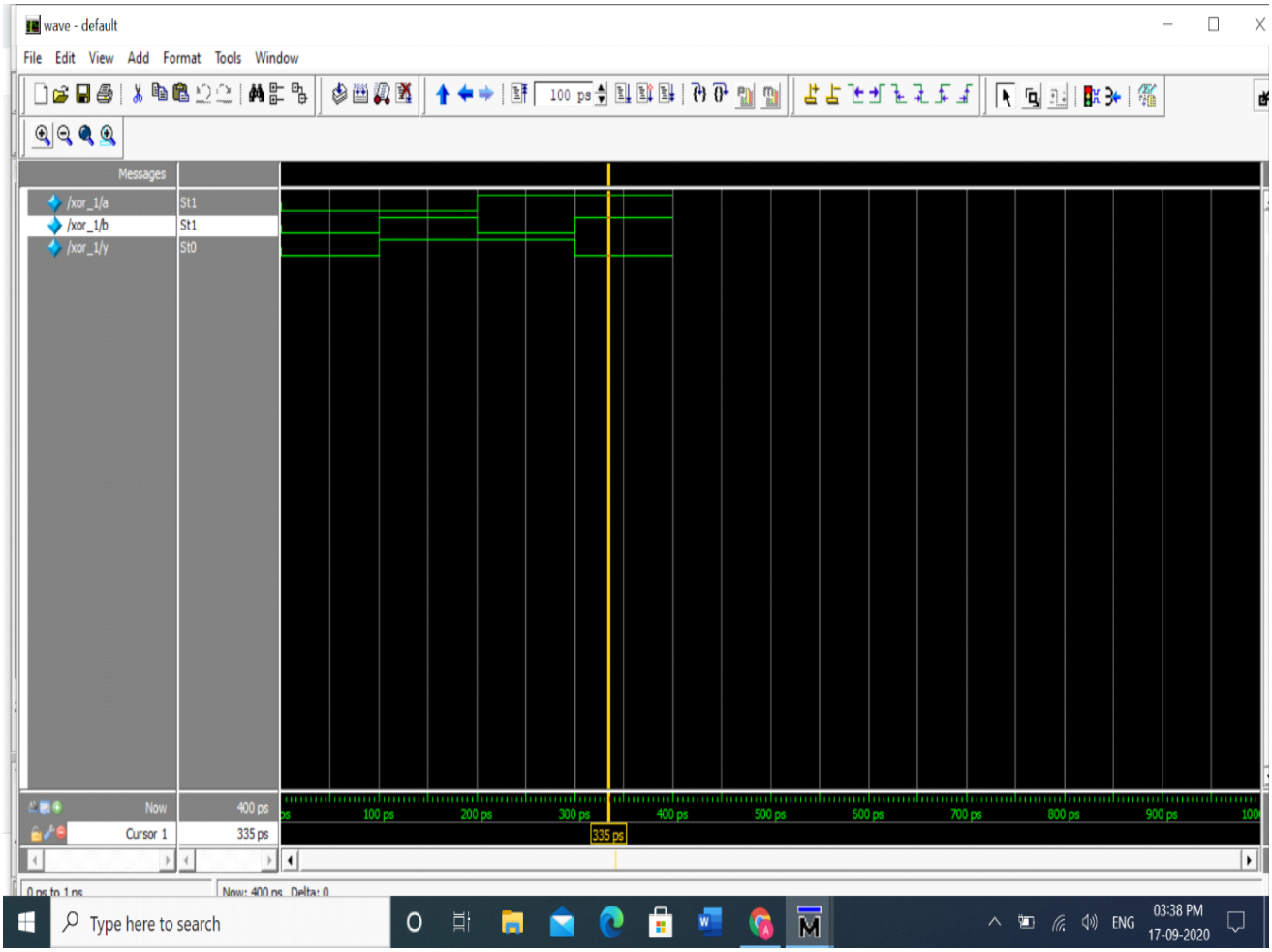
TRUTH TABLE:

XOR Truth Table		
A	**B**	**Q**
0	0	0
0	1	1
1	0	1
1	1	0

CODE:

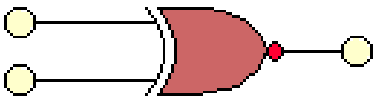


WAVEFORM:



D) – EX_NOR GATE:

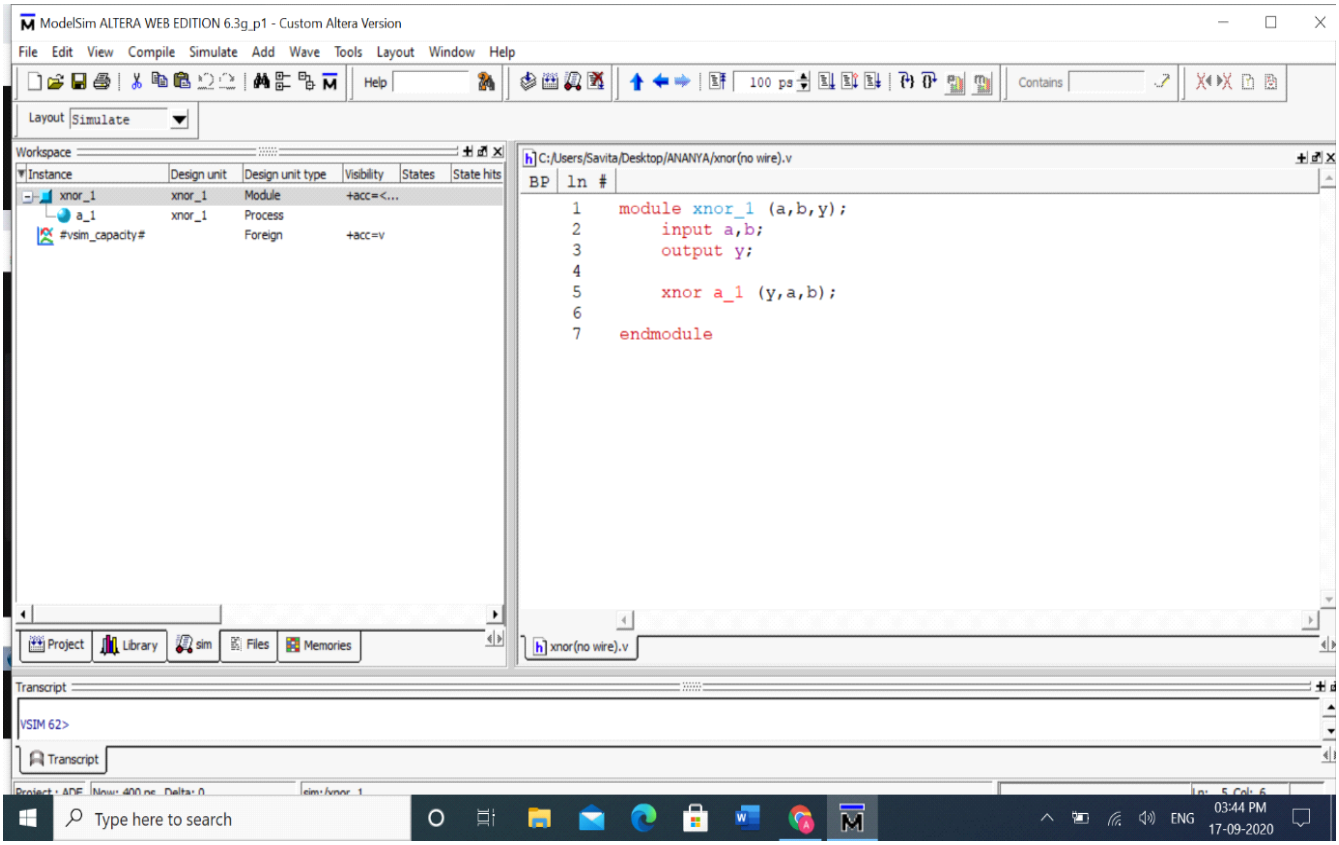
LOGIC DIAGRAM:



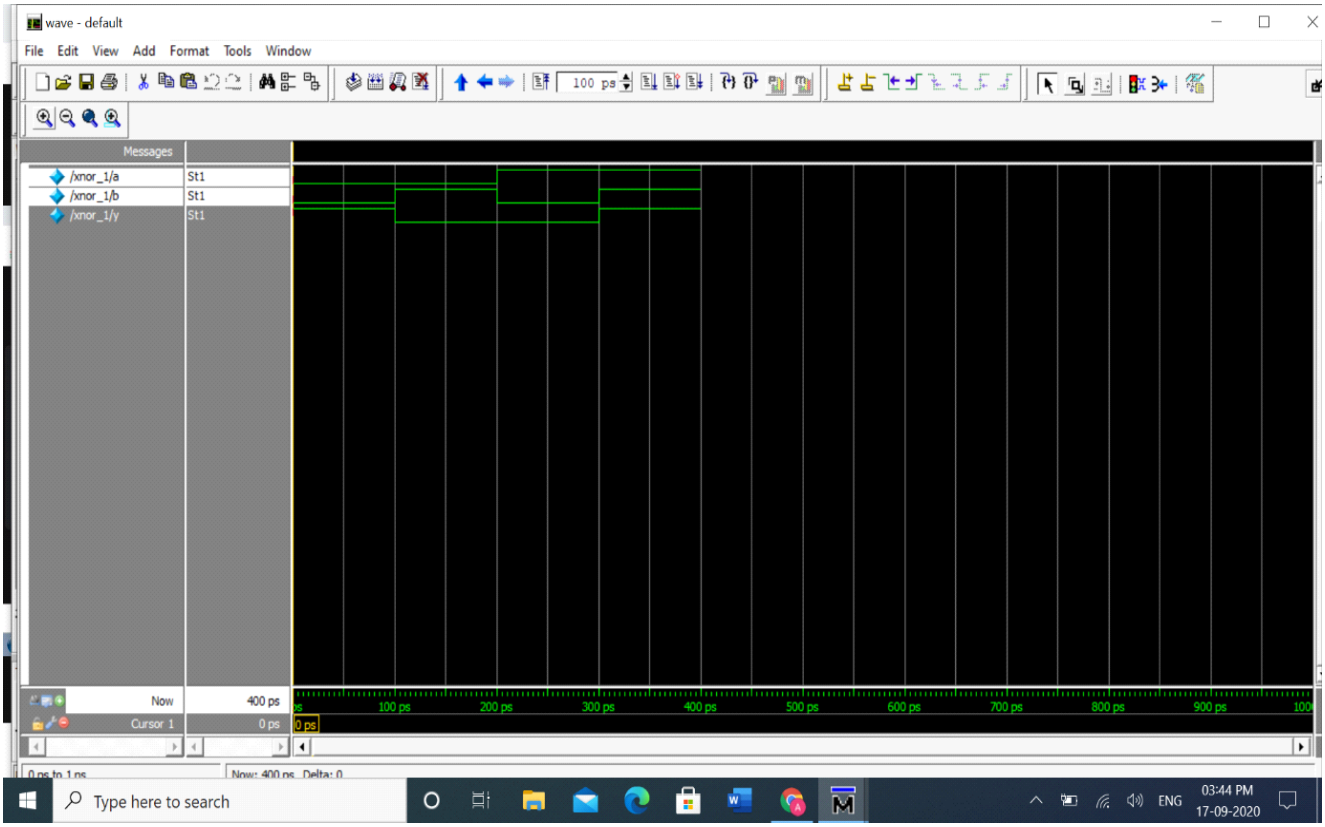
TRUTH TABLE:

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	1

CODE:



WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/xnor_1/a
/xnor_1/b
/xnor_1/y
St1
St1
St1
Now
400 ps
Cursor 1
0 ps
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
Type here to search
ENG
03:44 PM
17-09-2020

AIM: Design EX_OR GATE using gate level modeling with wire syntax .

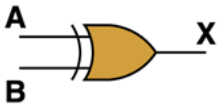
SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

LOGIC DIAGRAM:

Boolean Expression

$$X = A \oplus B$$

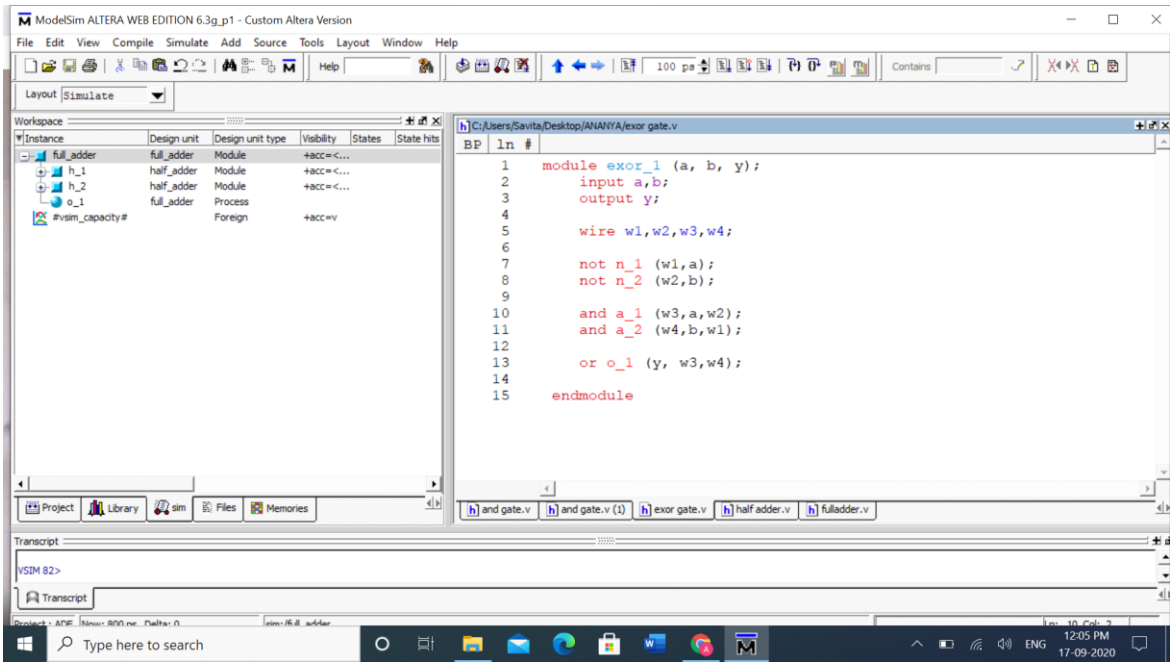
Logic Diagram Symbol



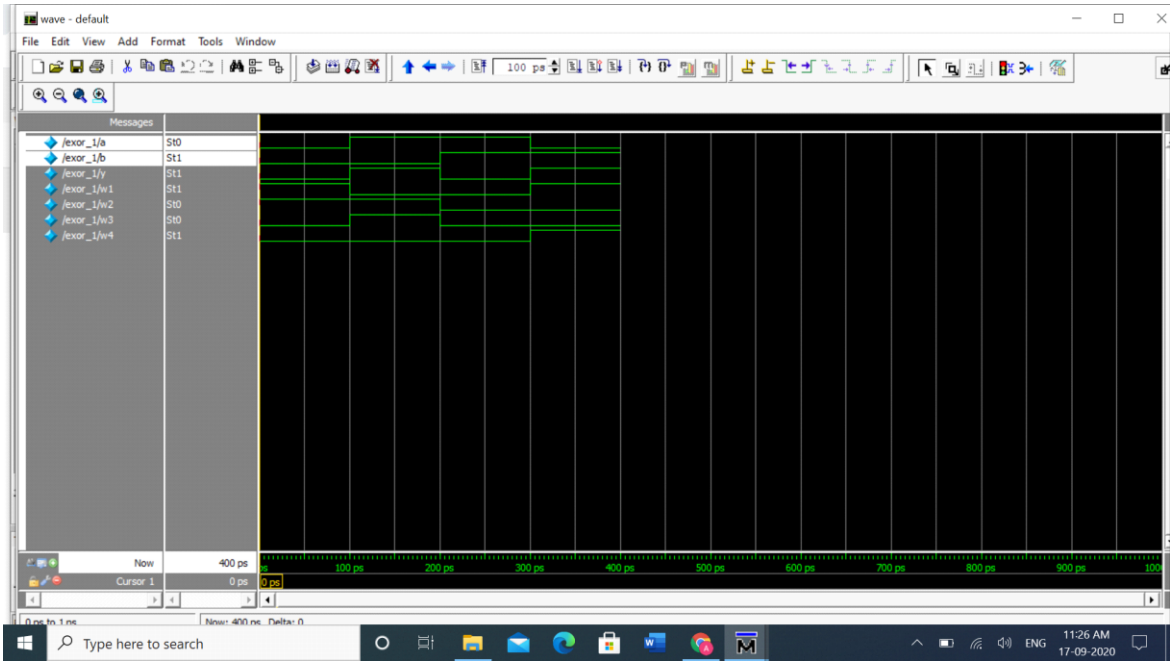
Truth Table

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

CODE:



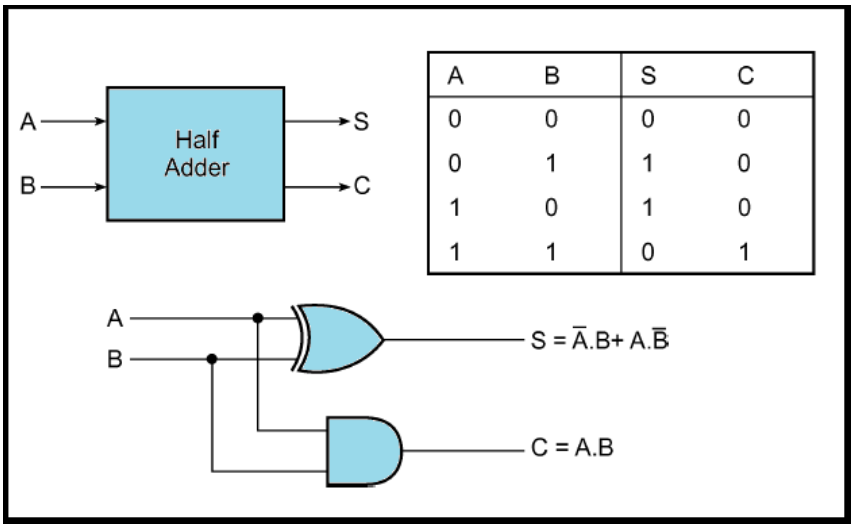
WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/exor_1/a
/exor_1/b
/exor_1/y
/exor_1/w1
/exor_1/w2
/exor_1/w3
/exor_1/w4
St0
St1
St1
St1
St0
St0
St1
Now
400 ps
Cursor 1
0 ps
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
Type here to search
ENG
11:26 AM
17-09-2020

AIM: Design HALF ADDER using gate level modeling .

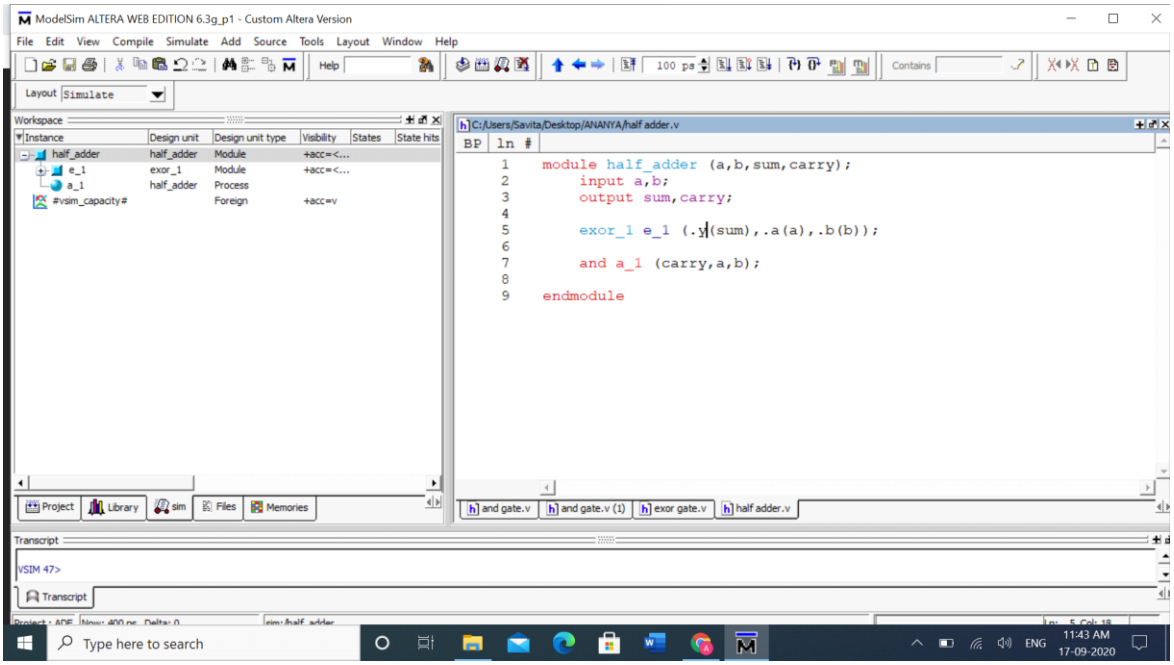
SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

LOGIC DIAGRAM:

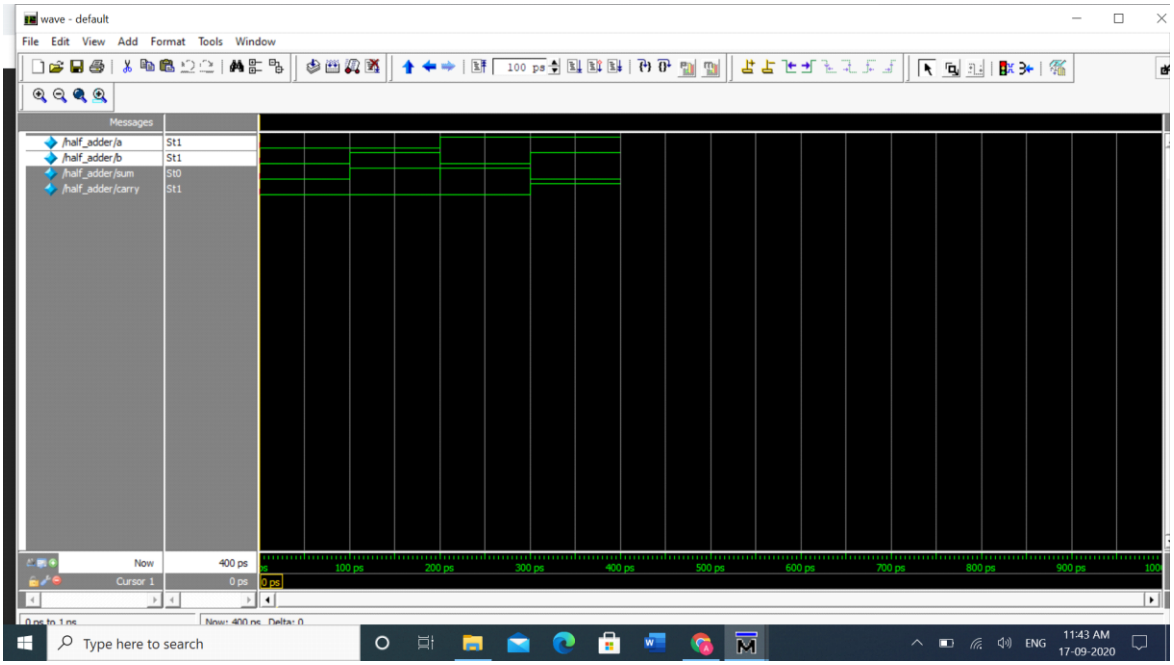


A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

CODE:



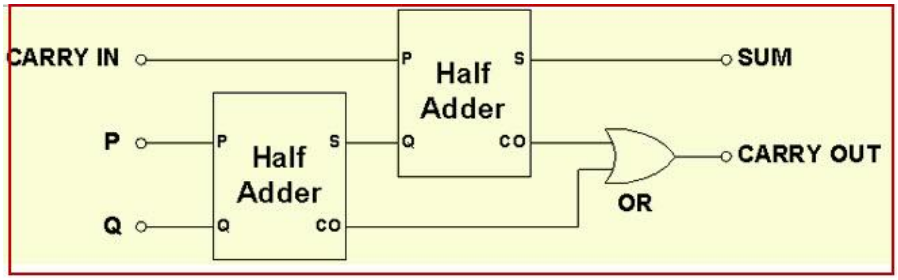
WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/half_adder/a
/half_adder/b
/half_adder/sum
/half_adder/carry
St1
St1
St0
St1
Now
400 ps
Cursor 1
0 ps
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
Type here to search
ENG
11:43 AM
17-09-2020

AIM: Design FULL ADDER using gate level modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

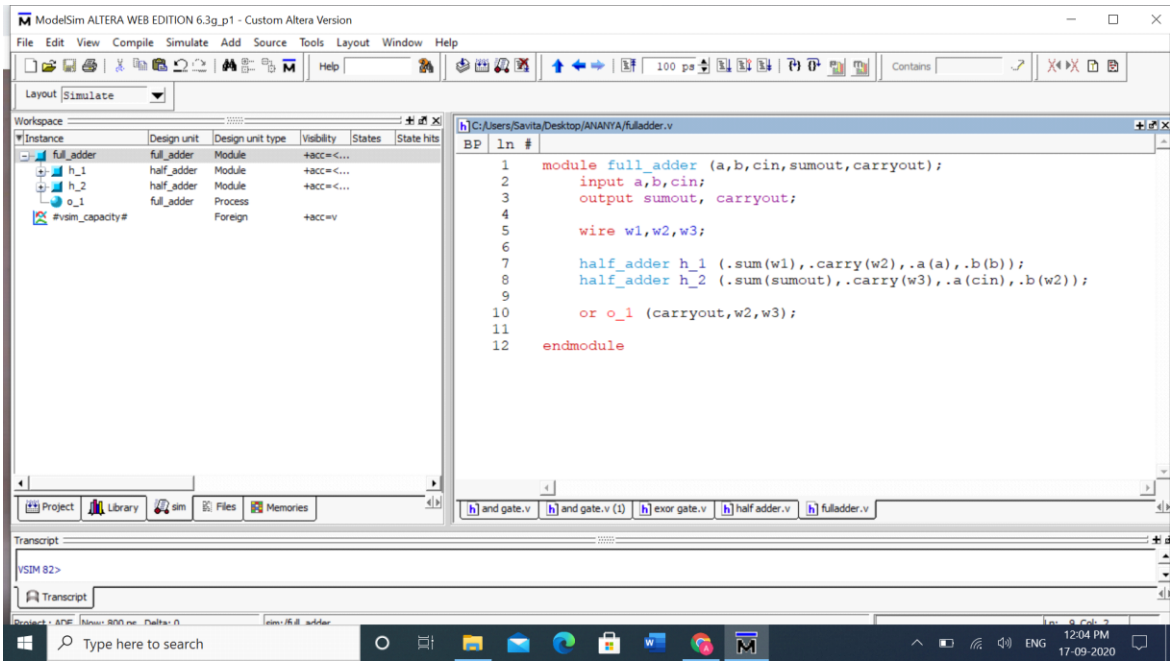
LOGIC DIAGRAM:



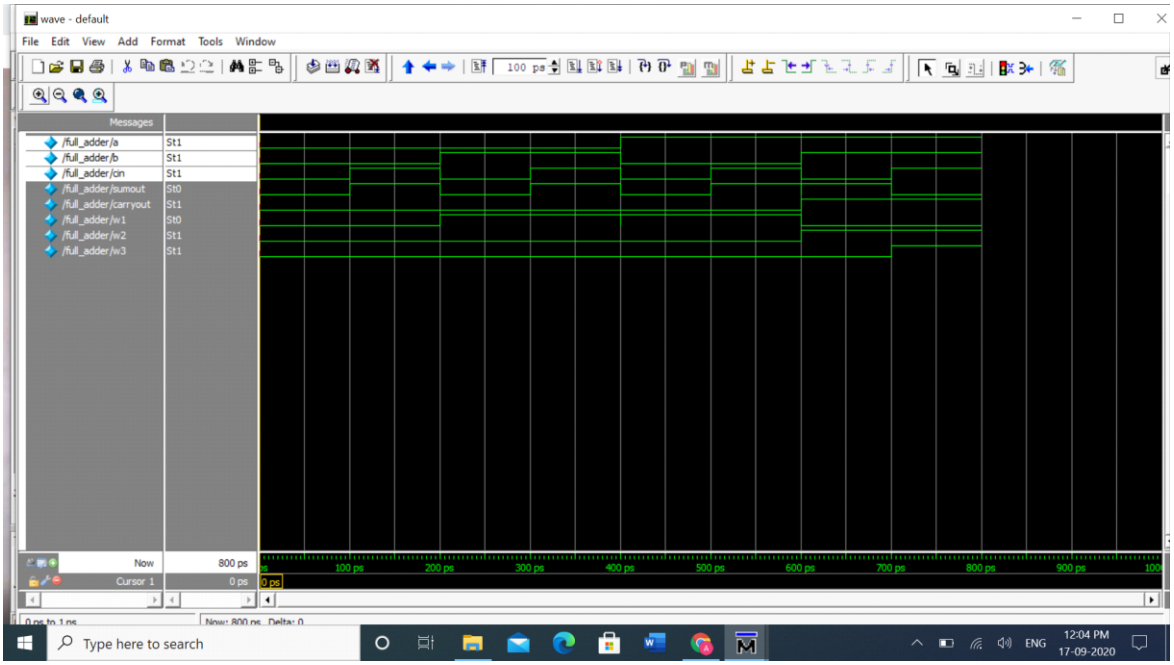
TRUTH TABLE:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

CODE:


ModelSim ALTERA WEB EDITION 6.3g_p1 - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Window Help
Workspace
Instance Design unit Design unit type Visibility States State hits
full_adder full_adder Module +acc=<...
h_1 half_adder Module +acc=<...
h_2 half_adder Module +acc=<...
o_1 full_adder Process
#vsim_capacity# Foreign +acc=v
C:/Users/Savita/Desktop/ANANYA/fulladder.v
BP ln #
1 module full_adder (a,b,cin,sumout,carryout);
2 input a,b,cin;
3 output sumout, carryout;
4
5 wire w1,w2,w3;
6
7 half_adder h_1 (.sum(w1),.carry(w2),.a(a),.b(b));
8 half_adder h_2 (.sum(sumout),.carry(w3),.a(cin),.b(w2));
9
10 or o_1 (carryout,w2,w3);
11
12 endmodule
Project Library sim Files Memories
and gate.v and gate.v (1) exor gate.v half adder.v fulladder.v
Transcript
VSIM 82>
Transcript
Type here to search
ENG
12:04 PM
17-09-2020

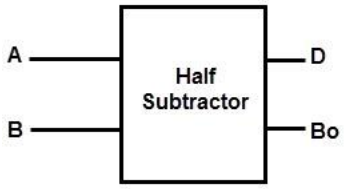
WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/full_adder/a St1
/full_adder/b St1
/full_adder/cin St1
/full_adder/sumout St0
/full_adder/carryout St1
/full_adder/w1 St0
/full_adder/w2 St1
/full_adder/w3 St1
Now 800 ps
Cursor 1 0 ps
100 ps 200 ps 300 ps 400 ps 500 ps 600 ps 700 ps 800 ps 900 ps
Type here to search
ENG
12:04 PM
17-09-2020

AIM: Design FULL ADDER using gate level modeling .

SOFTWARE REQUIRED: MODEL SIMULATOR. (VERILOG).

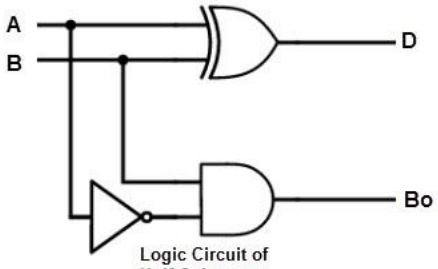
LOGIC DIAGRAM:



Block Diagram

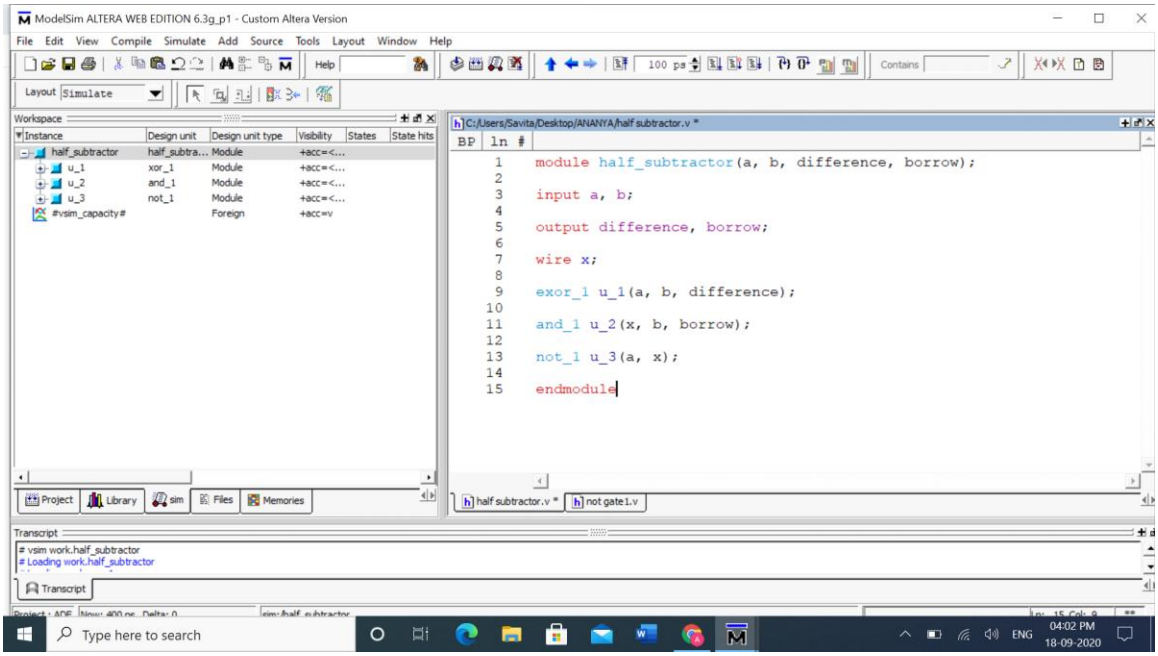
A	B	D	B_o
0	0	**0**	**0**
0	1	**1**	**1**
1	0	**1**	**0**
1	1	**0**	**0**

Truth Table

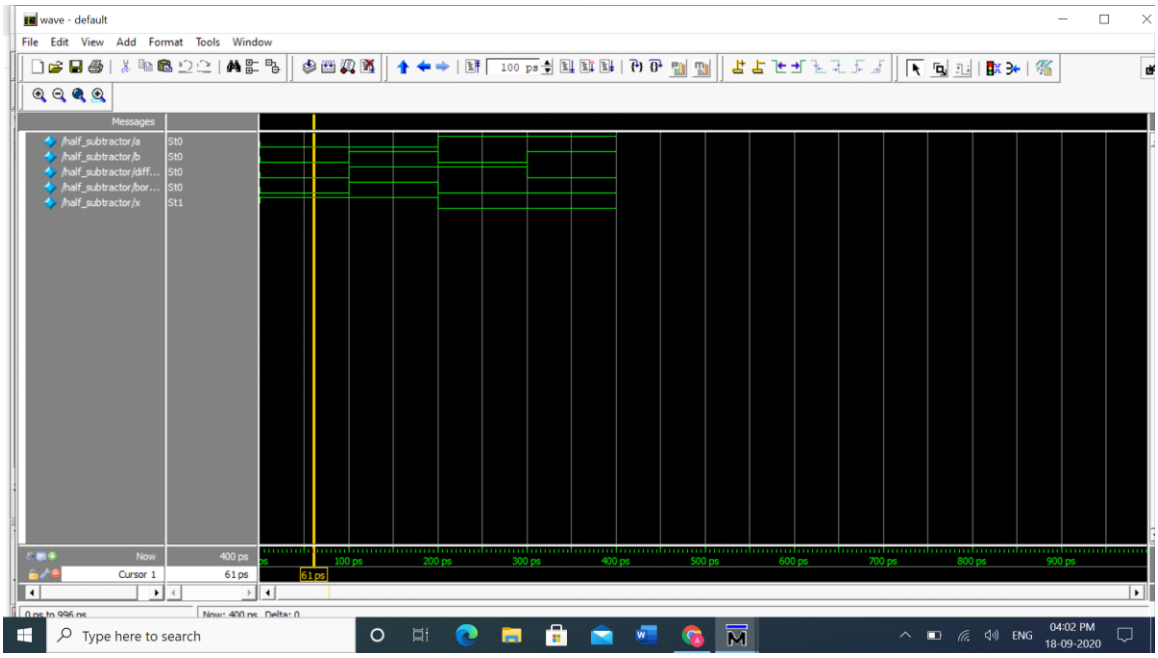


Logic Circuit of Half Subtractor

CODE:



WAVEFORM:


wave - default
File Edit View Add Format Tools Window
Messages
/half_subtractor/a
/half_subtractor/b
/half_subtractor/diff...
/half_subtractor/bor...
/half_subtractor/x
St0
St0
St0
St0
St1
Now
400 ps
Cursor 1
61 ps
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
Type here to search
ENG
04:02 PM
18-09-2020