# SRMIST

## NCR CAMPUS, MODINAGAR

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

**Analog and Digital Electronics Laboratory (18CSS201J)**

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| **Title of Experiment** | **: Experiment No. 5 : CMOS Inverter using PSPICE** |
| **Name of the candidate** | **: Ananya Gupta** |
| **Register Number** | **: RA1911003030265** |
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# Experiment No. 5 : CMOS Inverter using PSPICE

**Aim:** Design and implement CMOS inverter, measure propagation delay or rising and falling edge using PSPICE.

**Apparatus Require:** PSPICE Software

**Parameter Table:**

| PARAMETRS | PMOS | NMOS |
|---|---|---|
| L | **1µ** | **1 µ** |
| W | 20 **µ** | 5 **µ** |
| VTO | -2 | 2 |
| KP | $4.5e^{-4}$ | 2 |
| CBD | 5p | 5p |
| CBS | 2p | 2p |
| RD | 5 | 5 |
| RB | 0 | 0 |
| RS | 2 | 2 |
| RG | 0 | 0 |
| RDS | 1Meg | 1 Meg |
| CGSO | 1p | 1p |
| CGDO | 1p | 1p |
| CGBO | 1p | 1p |

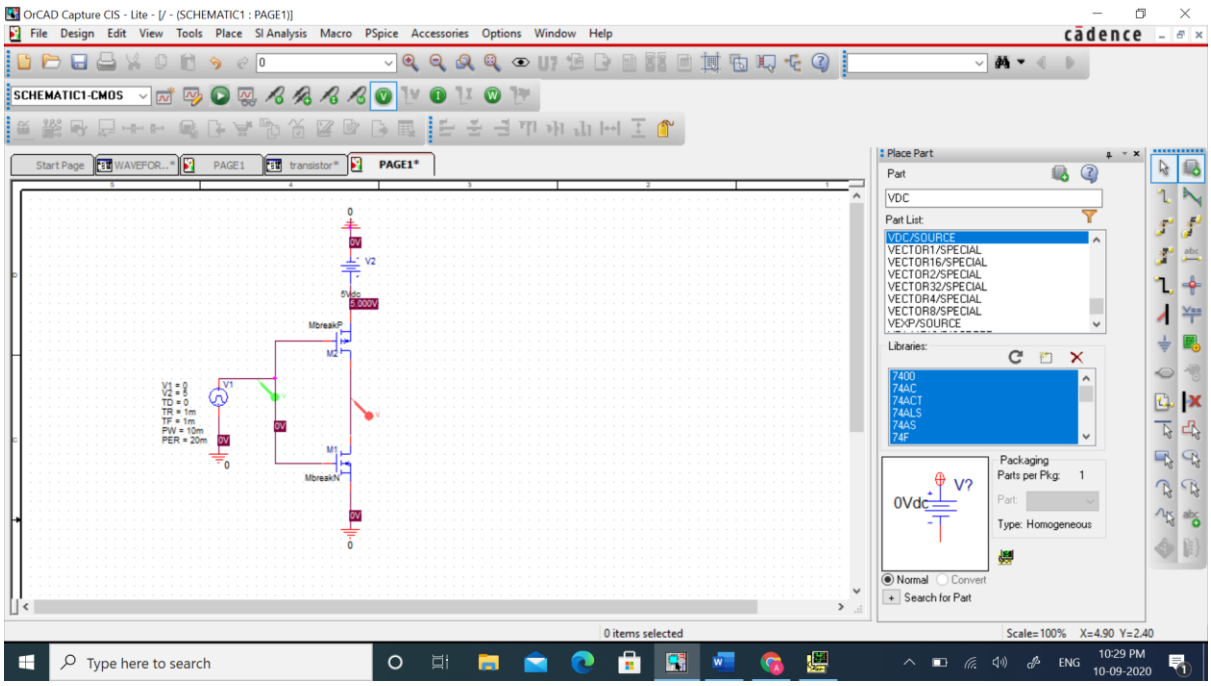
**Theory:**

**(i) Inverter**

CMOS is widely used in digital IC's because of their high speed, low power dissipation and it can be operated at high voltages resulting in improved noise immunity. The inverter consists of two MOSFETs. The source of p-channel device is connected to +VDD and that of n-channel device is connected to ground. The gates of two devices are connected as common input.

## Circuit Diagram:

## Inverter:




## GRAPH:

## Inverter: