PROJECT REPORT

Subject: Digital VLSI Design

Subject code: UE21EC251B

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AIM:

To design a schematic for a 2:4 decoder using transmission gate logic and verify its working, finding average power at one output node, say D0.

SOFTWARE TOOL:

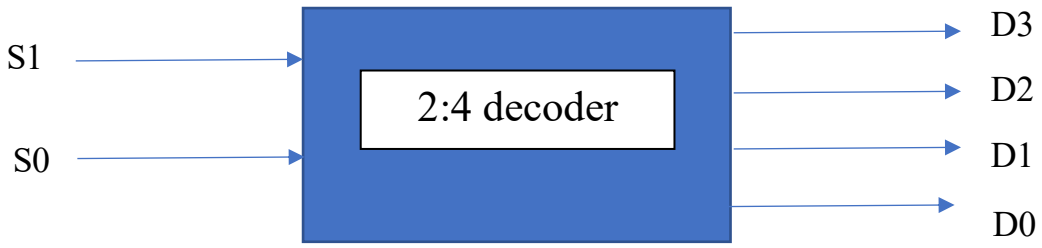
Cadence Virtuoso

THEORY:

Decoder:

Decoder is a combinational circuit that has ‘n’ input lines and maximum of 2n output lines. One of these outputs will be active high based on the combination of inputs present. That means decoder detects a particular code. The outputs of the decoder are nothing but the min terms of ‘n’ input variables lines.

A 2:4 decoder is a combinational circuit that takes in two inputs S0 and S1, and produces four outputs D0, D1, D2, D3. The two inputs S0 and S1 represent a two-bit binary number, and the four outputs represent the four possible combinations of the two bits.

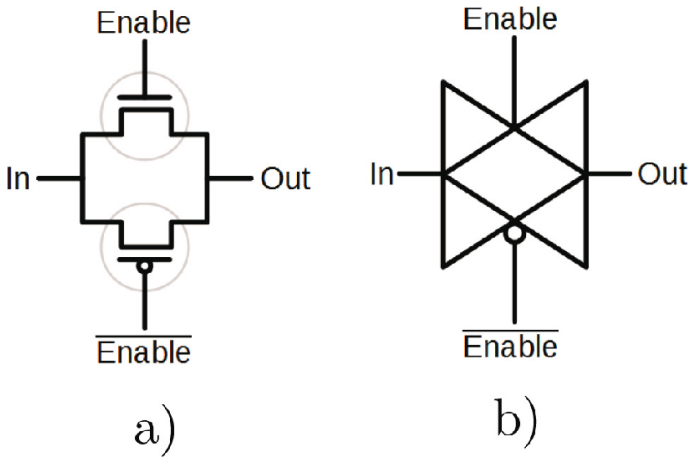


Transmission gates:

Transmission gates are electronic devices used in digital circuits that provide a low resistance path between two points in a circuit when they are enabled, and a high resistance path when they are disabled. They are also known as pass gates or analog switches.

A transmission gate consists of two complementary metal-oxide-semiconductor (CMOS) transistors, one PMOS and one NMOS, connected in parallel between the input and output nodes of the gate. When the transmission gate is enabled, both transistors turn on, providing a low resistance path between the input and output

nodes. When the transmission gate is disabled, both transistors turn off, providing a high resistance path between the input and output nodes.



TRUTH TABLE:

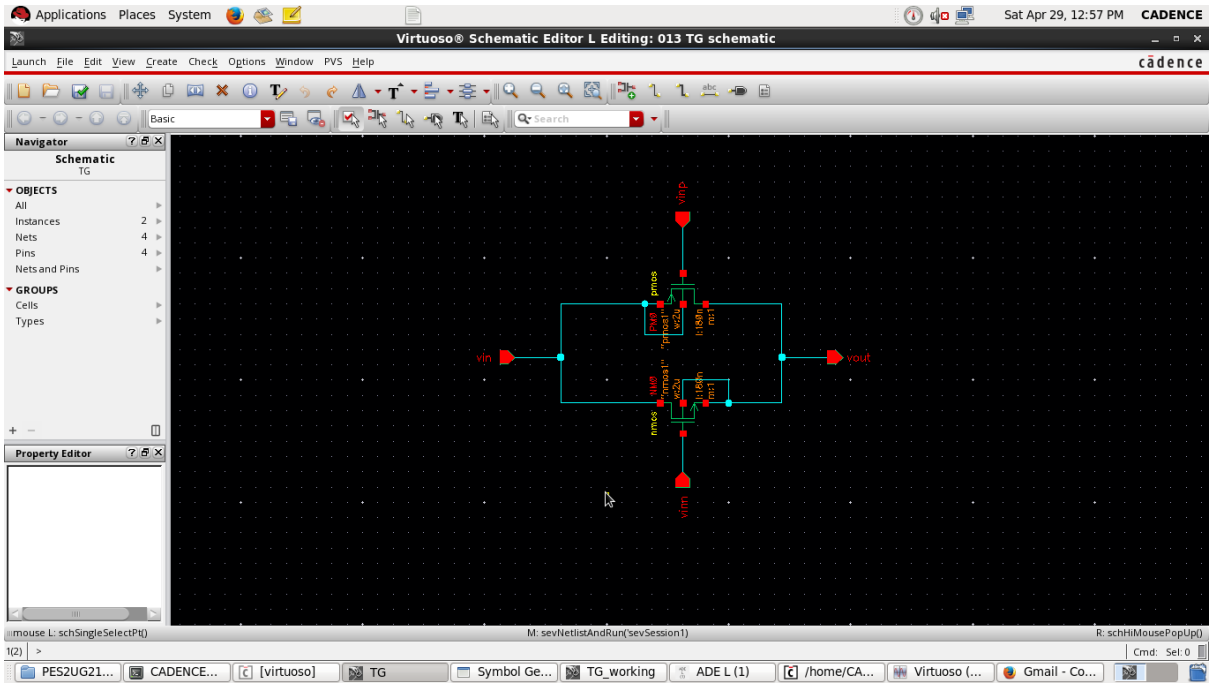
2:4 decoder:

S1	S0	D3	D2	D1	D0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

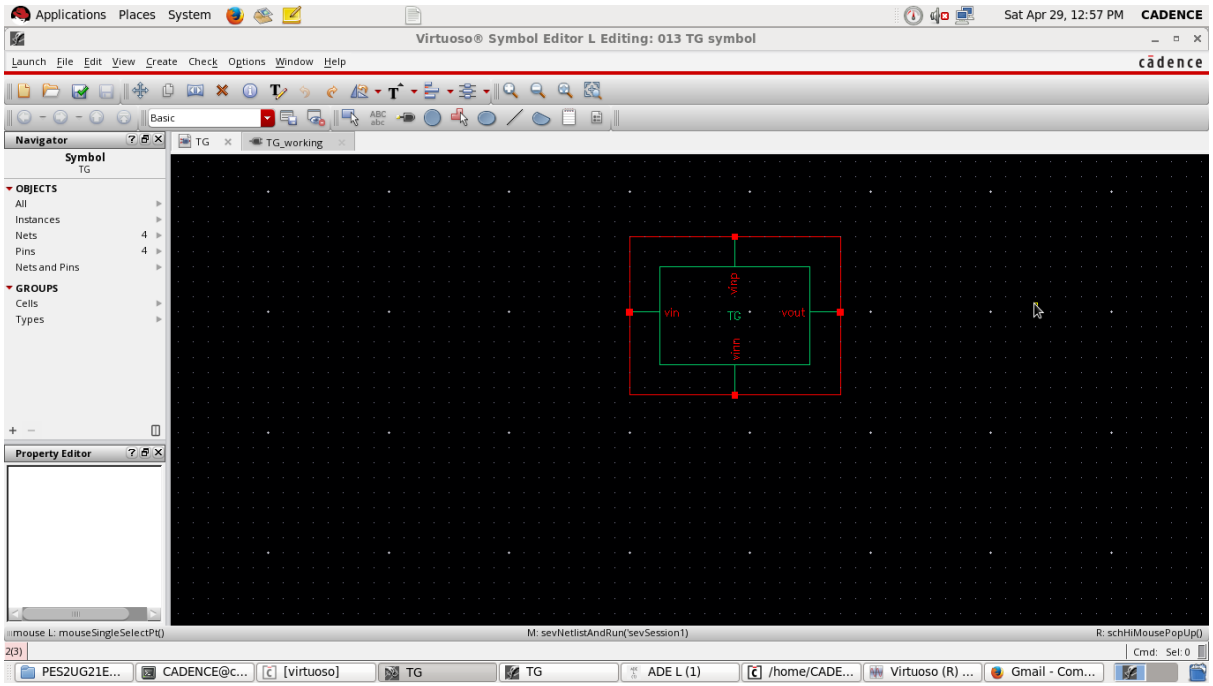
Transmission gate:

Enable	IN	OUT
0	X	Z
1	0	0
1	1	1

RESULTS:

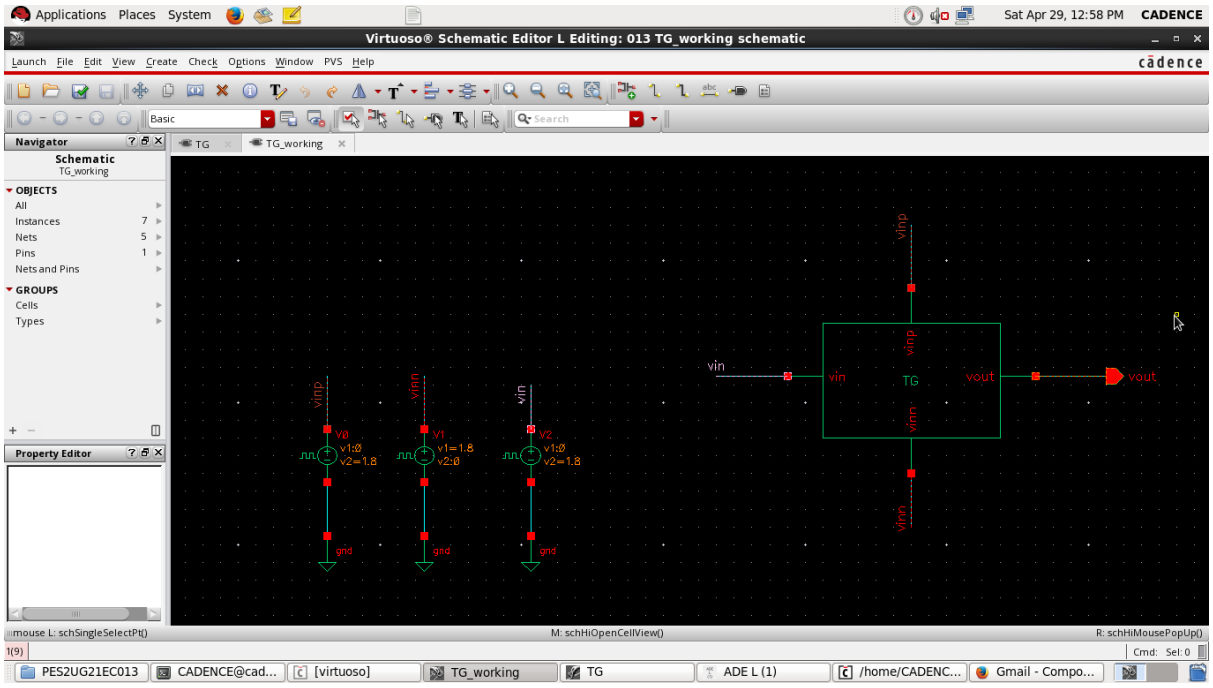


The above image shows the schematic of a transmission gate where **vin** and **vout** is the input and output respectively. **vinn** and **vinp** are the gate voltages provided to the NMOS and PMOS respectively. They are complimentary in nature. A symbol will be generated for the above schematic:

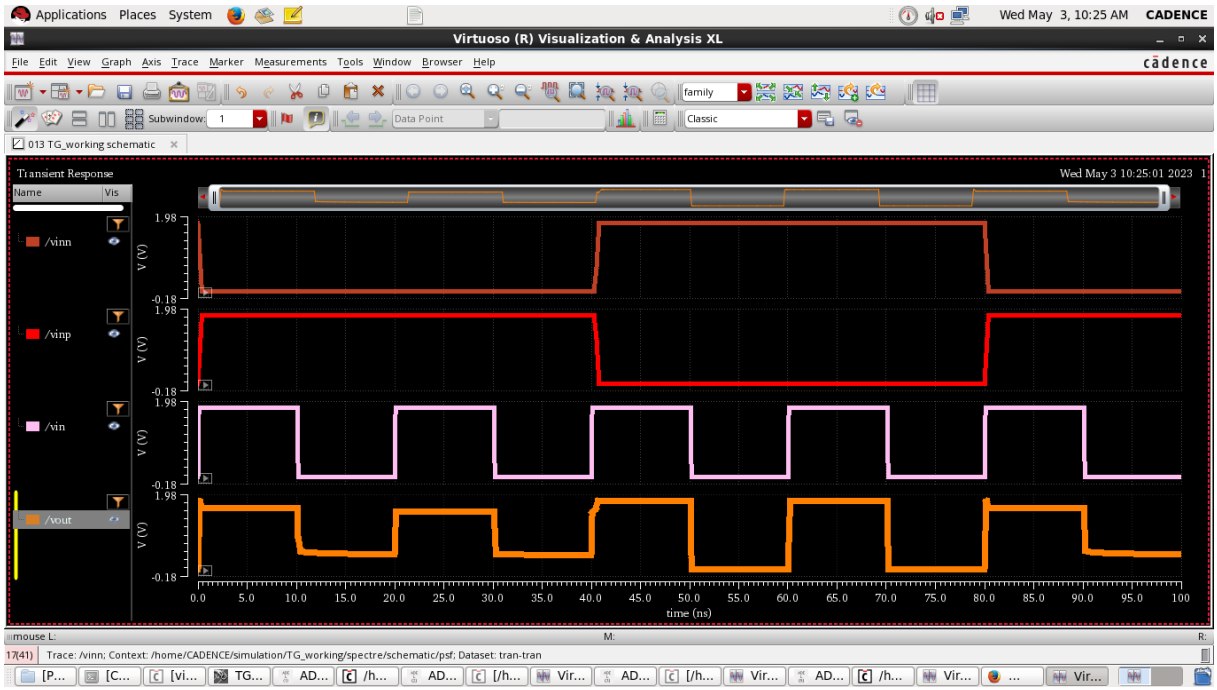


The name for the symbol is given as **TG**.

Now the symbol will be tested if it satisfies all the test cases.

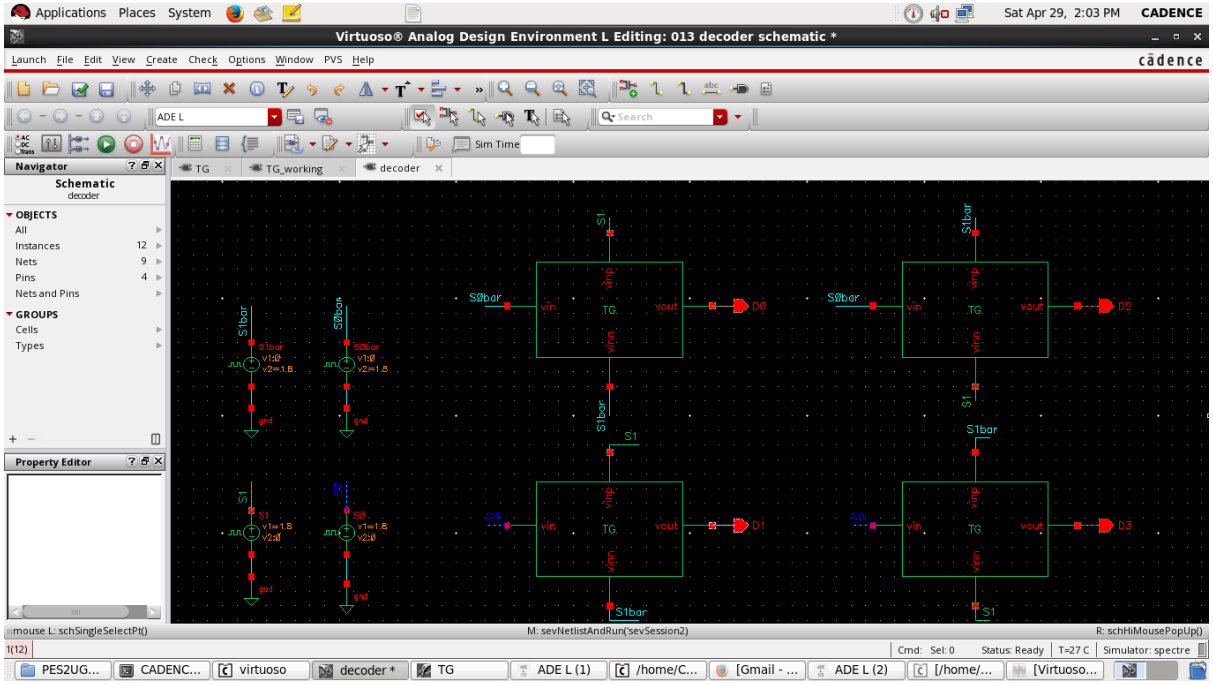


The output timing diagram thus obtained when the above schematic is executed is as follows:



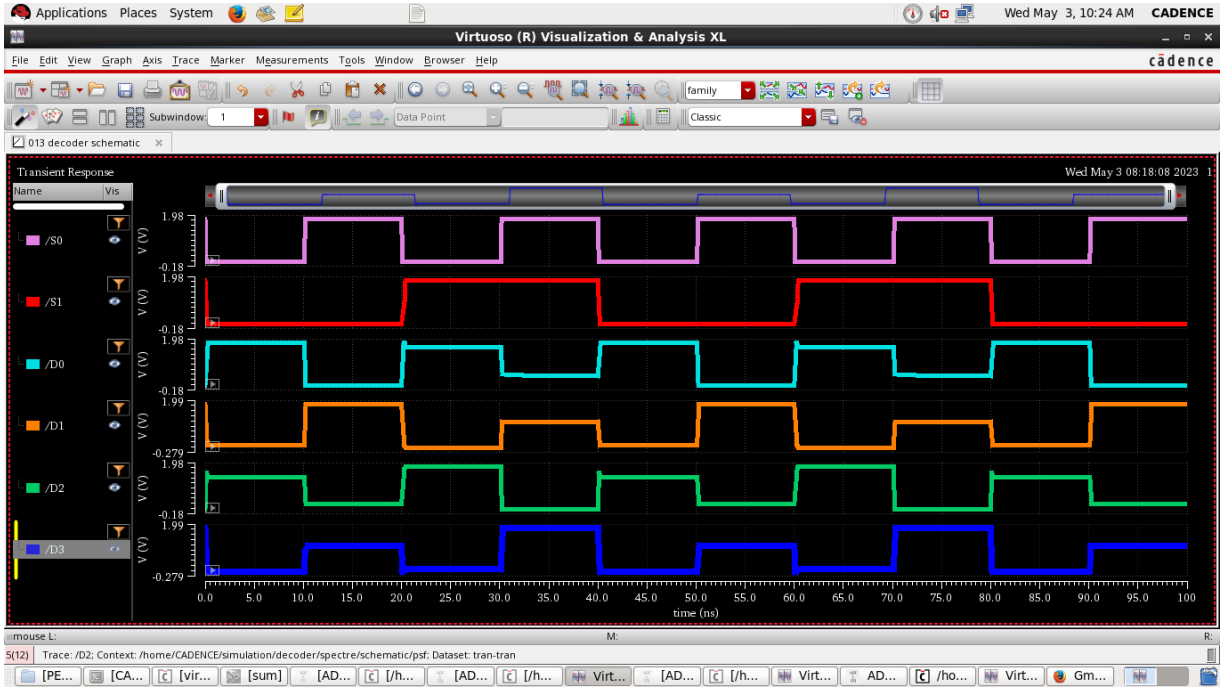
We can observe that the output follows the input and hence the functionality of the transmission gate TG is verified.

A schematic for 2:4 decoder using the above transmission gate TG is constructed:

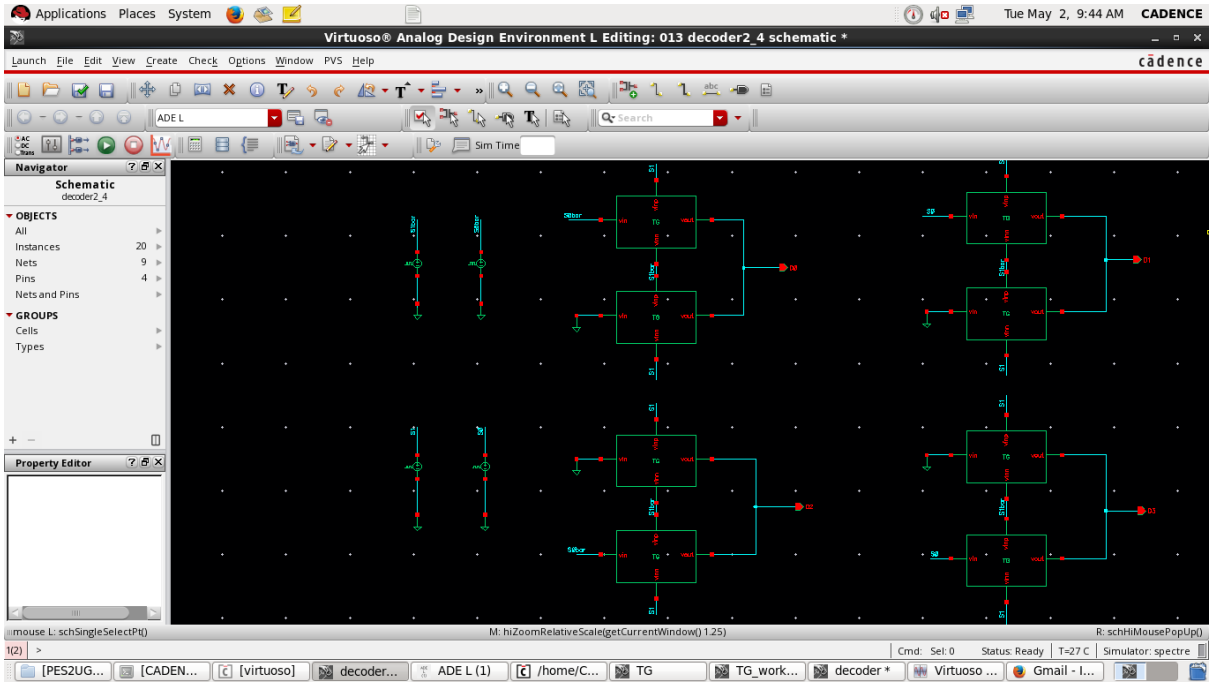


One transmission gate is used to generate each output. Therefore, there are a total of 4 transmission gates.

The timing diagram when the above schematic is executed:

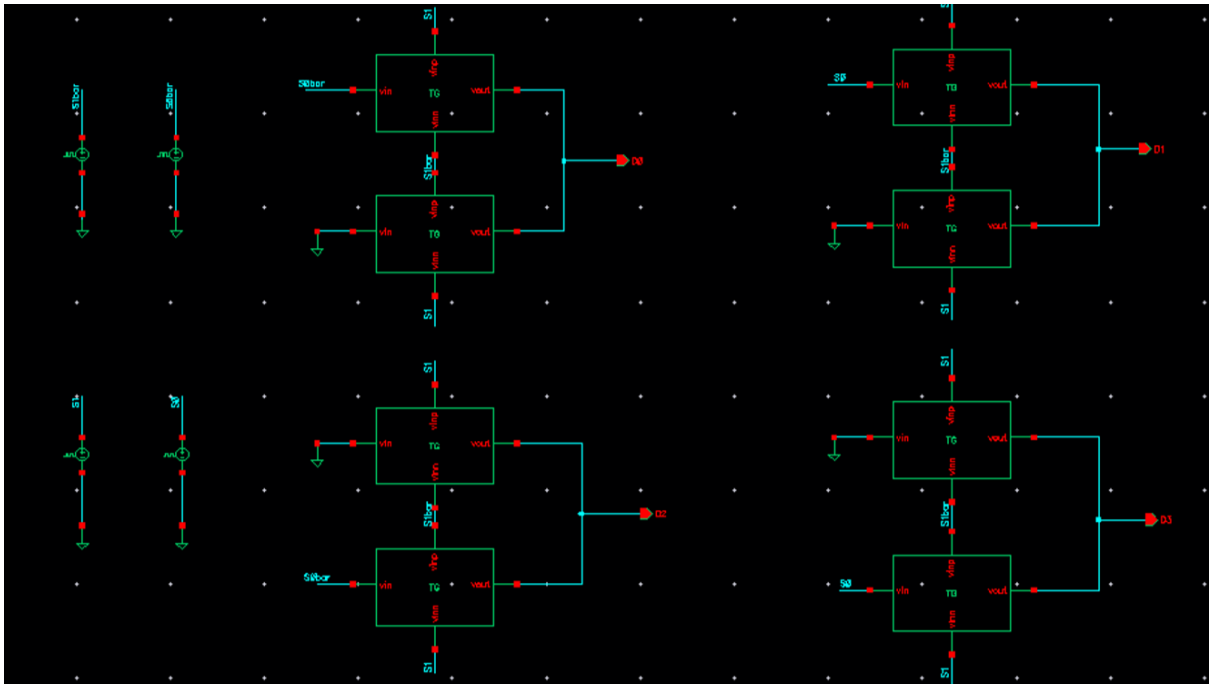


We observe that at certain test cases we obtain the Z value as output. To eliminate this condition, a new schematic is constructed:

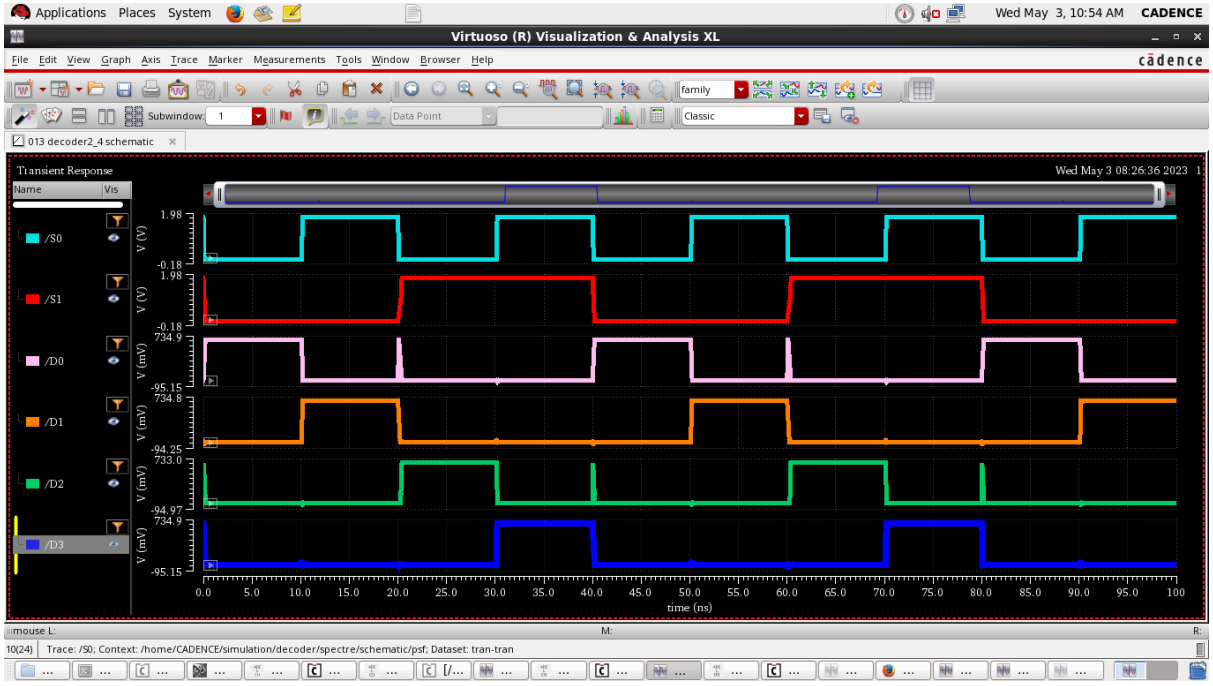


In this case, two transmission gates are used to generate each output. Therefore, a total of 8 transmission gates are used.

Zoomed in image:

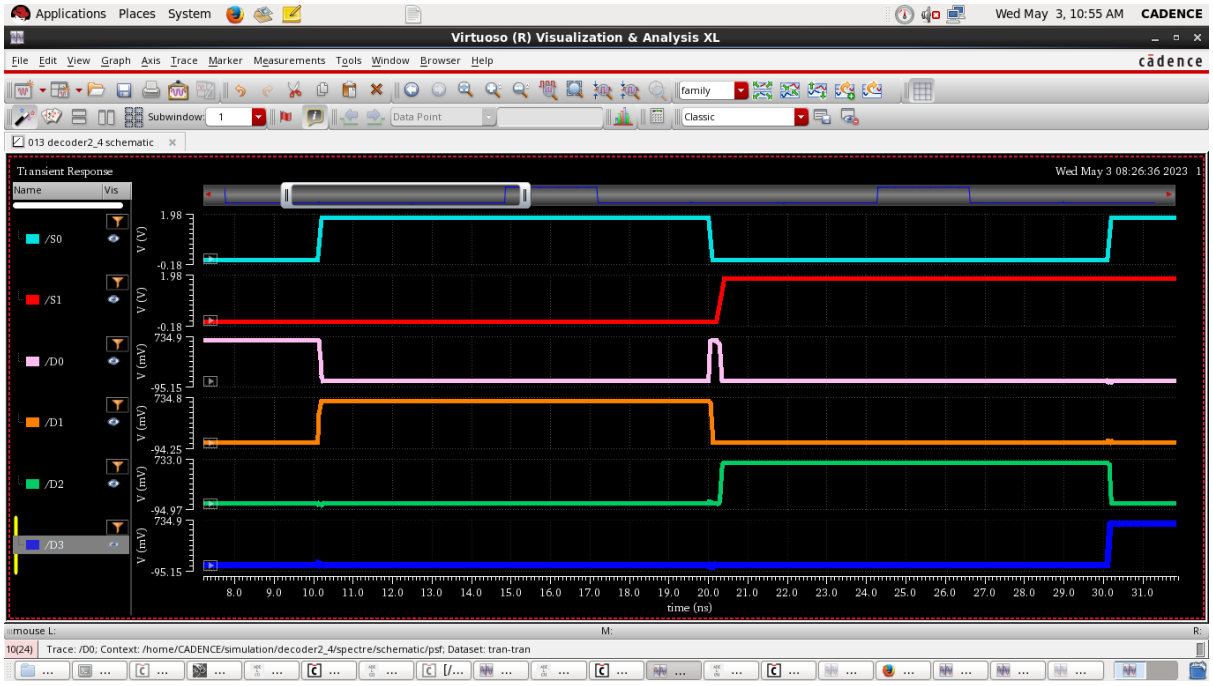


The resulting timing diagram after execution of above schematic:



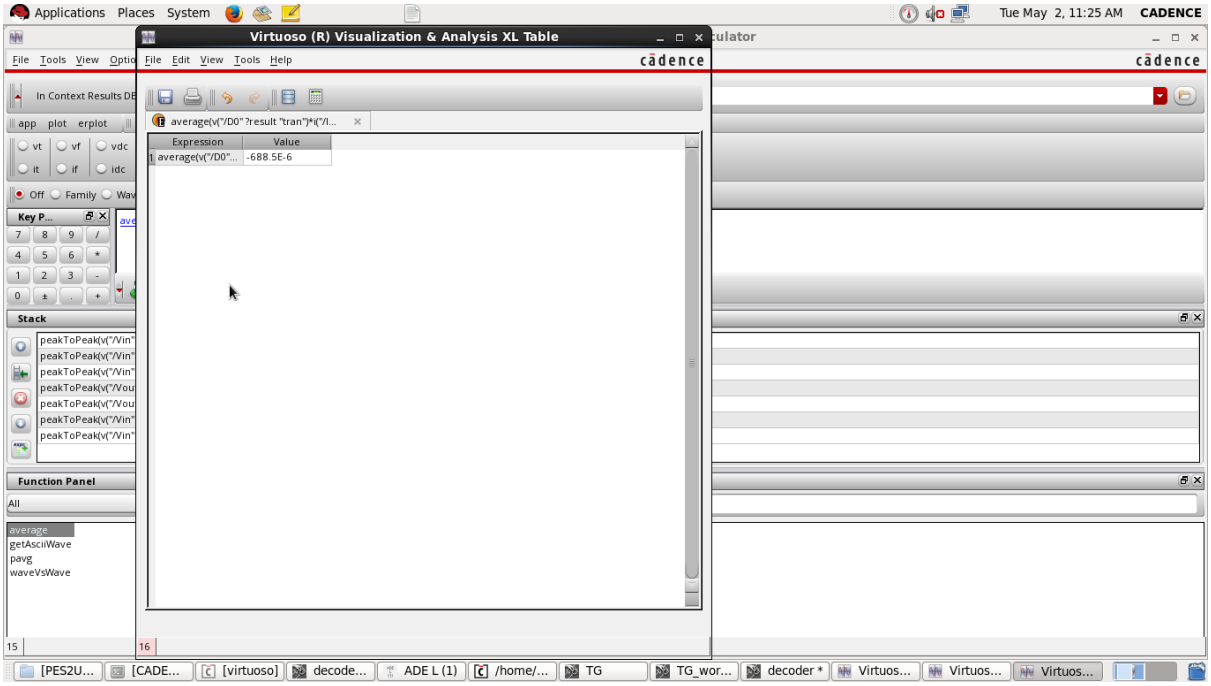
It is observed that all the Z values are eliminated and the timing diagram satisfies all the test cases of the truth table.

However, there are certain spikes at some points in the outputs.



In the above image, we can observe the spike prominently as it is zoomed in. The spike is caused due to the delay between the input signals S1 and S0. S1 lags behind S0. S0 starts transitioning from logic 1 to logic 0 at 20 ns. However, S1 starts transitioning from logic 0 to logic 1 at 20.3 ns. The output for D0 before 20 ns, when S0=1 and S1=0 is logic 0 and the output after 20.5 ns when S0=0 and S1=1 is also logic 0. Between 20 ns and 20.5 ns, S0 and S1 are in transition phase and due to a delay between them, in the region between 20 ns and 20.3 ns, S0=0 and S1 is still logic 0. Therefore, the output D0 reads as logic 1 in this region.

Average power calculations:



Average power at D0 is calculated by measuring the voltage across and current through the transmission gates corresponding to D0.

CONCLUSION:

Decoders are commonly used in digital circuits to decode binary information and to enable or disable various other circuit elements based on the decoded information. Here are some common applications of decoders:

1.Memory Address Decoding

2.Display Driver

3.Programmable Logic Arrays (PLAs)

4.Address Decoding for I/O Devices

5.Data Routing

Overall, decoders are an essential building block in digital circuits, allowing binary information to be decoded and used to control various other circuit elements.