



PROJECT REPORT

Subject: Low Power VLSI

Subject code: UE21EC342BB3

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AIM:

Analysis of average, static and dynamic power for 4 bit and 2 bit multiplier built in structural method involving basic gates, muxes, half adder and full adder.

TOOL USED:

Cadence Virtuoso

THEORY:

Static power:

Static power is the power consumed when there is no circuit activity or you can say, when the circuit is in quiescent mode. In the presence of a supply voltage, even if we withdraw the clocks and don't change the inputs to the circuit, the circuit will still consume some power, called the static power consumption. It is mainly due to the leakage currents that flows, when the transistor is in off-state.

$$P_{static} = V_{dd}I_{cc}$$

V_{dd}: Voltage applied to a logic IC

I_{cc}: Static supply current

Dynamic power:

Dynamic power is the power consumed when the circuit is in operation, which means we have applied supply voltage, applied clock and changed the inputs. One of the main components of dynamic power is switching power.

Switching power:

Dissipation due to the charging and discharging of total load, which includes the output capacitors and other parasitic capacitors. At a very high level, we can say the switching power dissipation,

$$P_{switch} = \alpha V_{dd}^2 C_L f$$

where,

α = switching activity

V_{dd} = supply voltage

C_L = total load capacitance

f = frequency of operation

Average power:

The average power of a digital circuit is a measure of the average rate at which energy is consumed by the circuit during its operation.

$$P_{avg} = \frac{1}{T} \int_0^T P(t) dt$$

Multiplier architecture:

A 4-bit serial multiplier is a digital circuit that multiplies two 4-bit binary numbers in a serial manner, meaning it processes the binary digits one by one rather than all at once. This type of multiplier is commonly used in various digital systems where area efficiency or power consumption is critical.

Working:

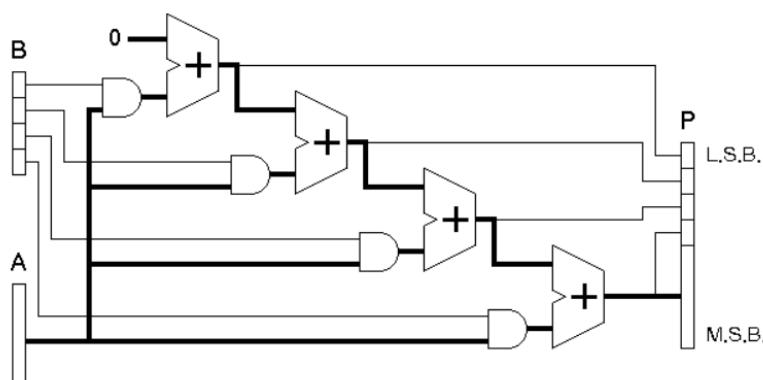
1. The two 4-bit binary numbers to be multiplied are fed serially into the multiplier circuit, one bit at a time, usually starting with the least significant bit (LSB) and ending with the most significant bit (MSB).
2. As each bit of the multiplier is input serially, partial products are generated by multiplying the multiplicand (the 4-bit number being multiplied) with the corresponding bit of the multiplier.
3. These partial products are accumulated to produce the final result.

$$\begin{array}{r}
 & \text{x3} & \text{x2} & \text{x1} & \text{x0} \\
 * & \text{y3} & \text{y2} & \text{y1} & \text{y0} \\
 \hline
 & \text{x3y0} & \text{x2y0} & \text{x1y0} & \text{x0y0} \\
 + & \text{x3y1} & \text{x2y1} & \text{x1y1} & \text{x0y1} \\
 + & \text{x3y2} & \text{x2y2} & \text{x1y2} & \text{x0y2} \\
 + & \text{x3y3} & \text{x2y3} & \text{x1y3} & \text{x0y3} \\
 \hline
 & \text{z7} & \text{z6} & \text{z5} & \text{z4} & \text{z3} & \text{z2} & \text{z1} & \text{z0}
 \end{array}$$

X0, X1, X2, X3 are the bits of the multiplicand.

Y0, Y1, Y2, Y3 are the bits of the multiplier.

X0Y0, X0Y1, X0Y2... etc are the partial products.



This is the basic architecture of a serial multiplier. It consists of a series of AND gates, half adders and full adders.

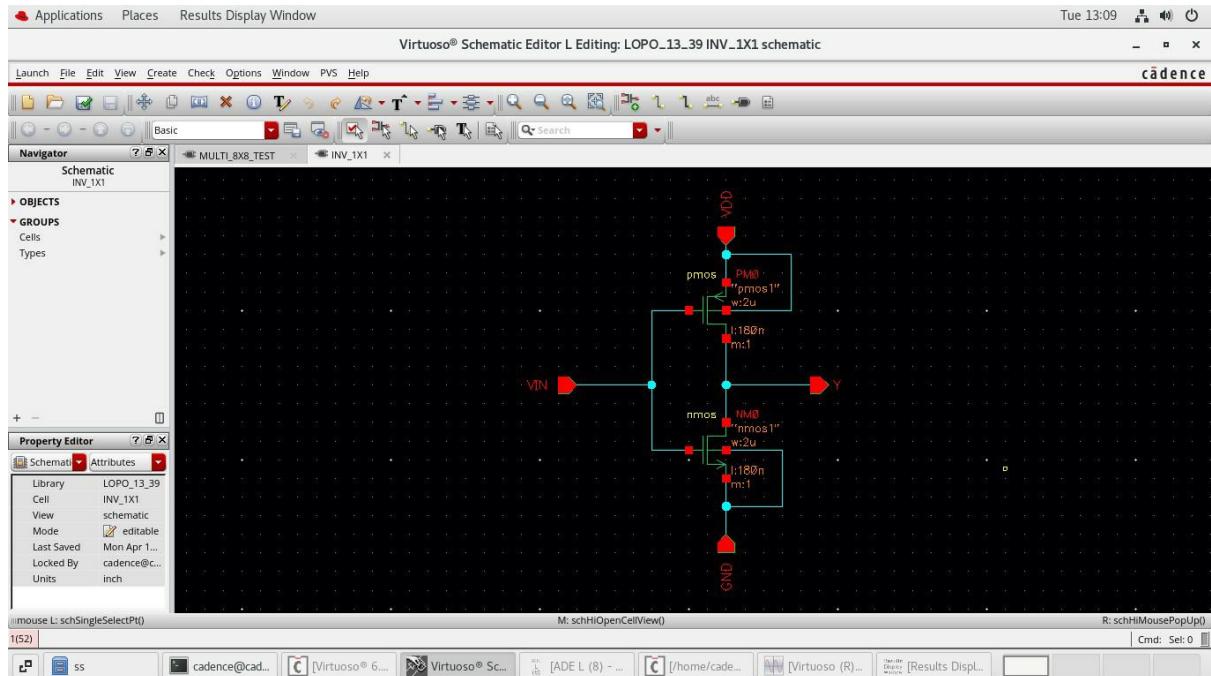
RESULTS:

Basic gates such as INV, NAND, AND, XOR are constructed using CMOS technology. We will be using these gates to build higher units in the architecture.

Inverter:

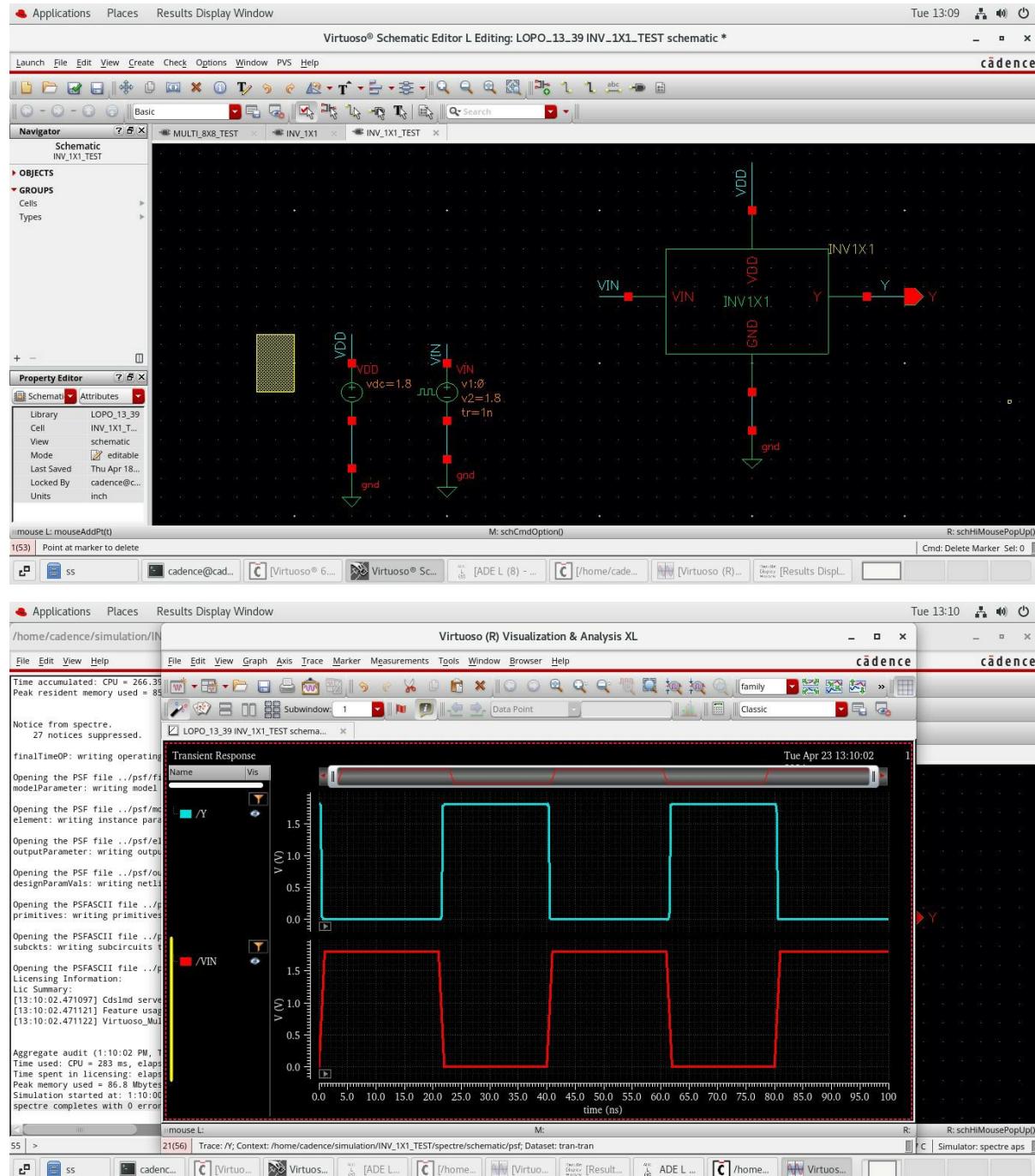
Schematic:

Inverter is constructed using CMOS technology. Input is given at Vin and output is tapped at Y.



Functionality test:

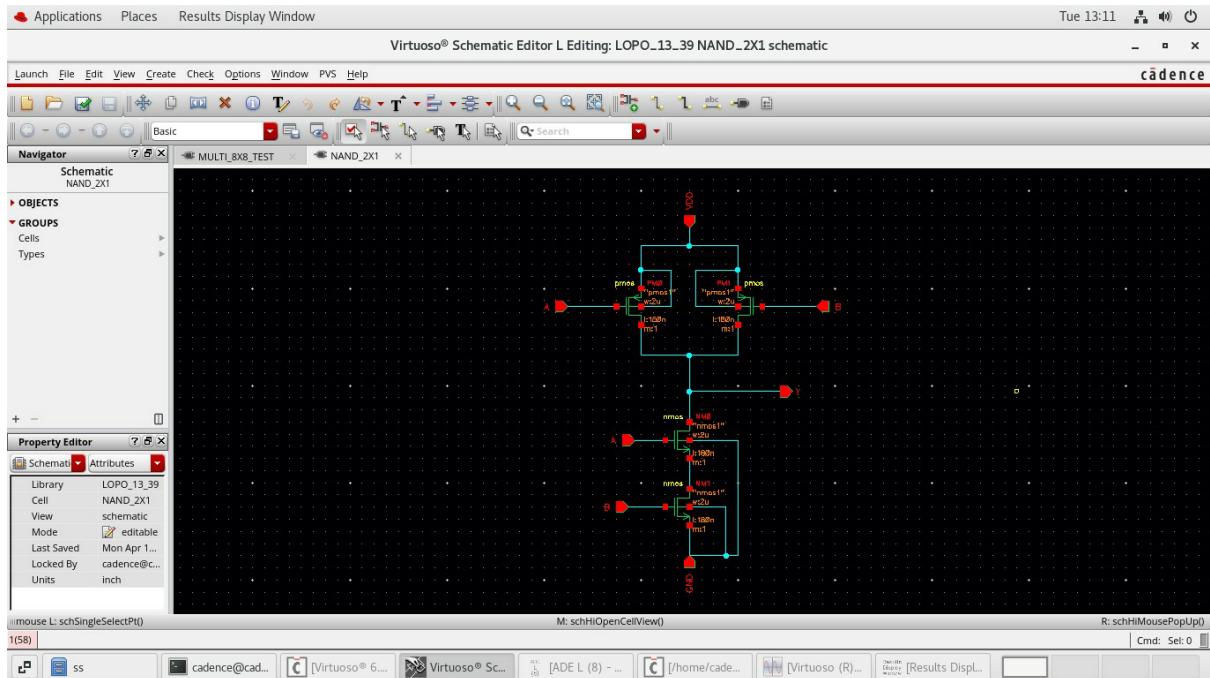
The working of the inverter is checked by giving pulsating input Vpulse. We observe in the waveform that the inverter works accordingly with respect to its truth table.



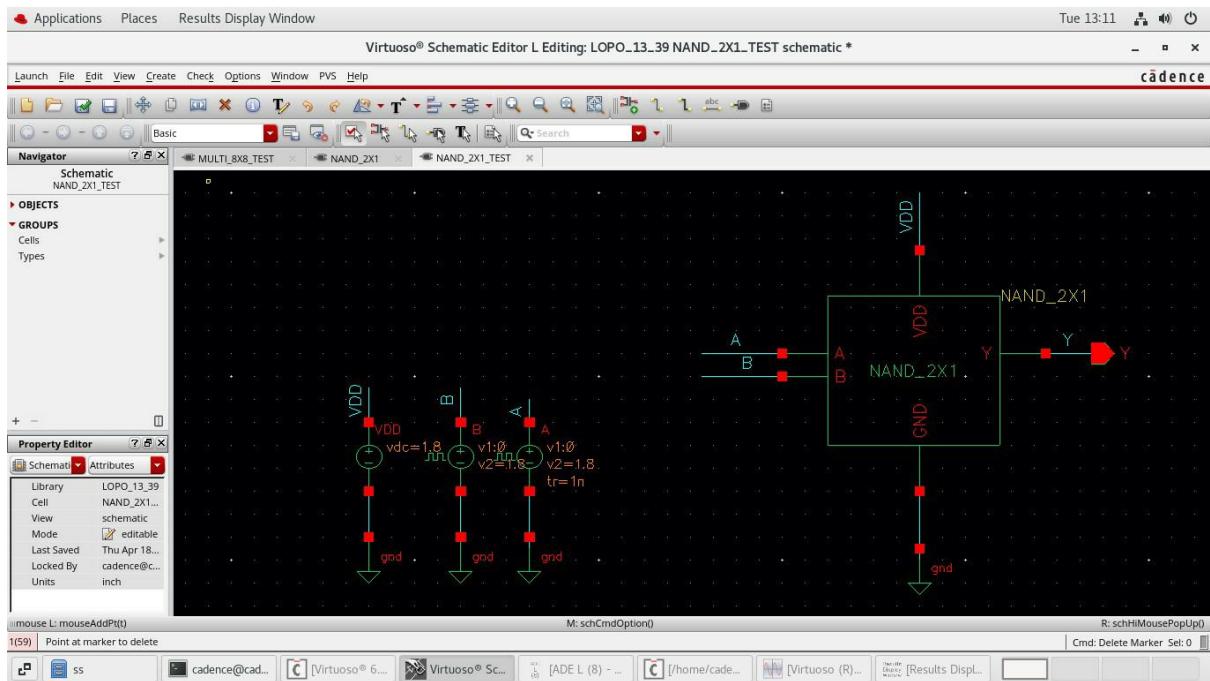
The same steps are followed for NAND gate, AND gate, OR gate and XOR gate, 2:1 MUX, Half adder and Full adder. Half adder and Full adder are implemented using the gates mentioned above using their symbols.

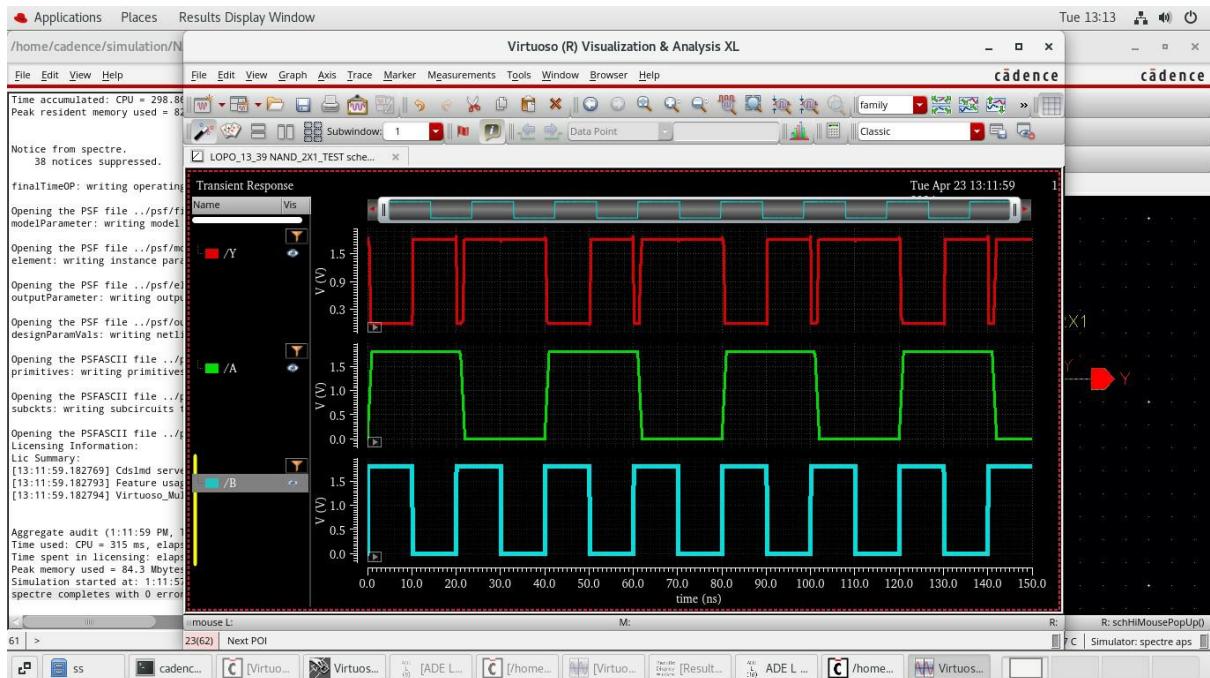
NAND gate:

Schematic:



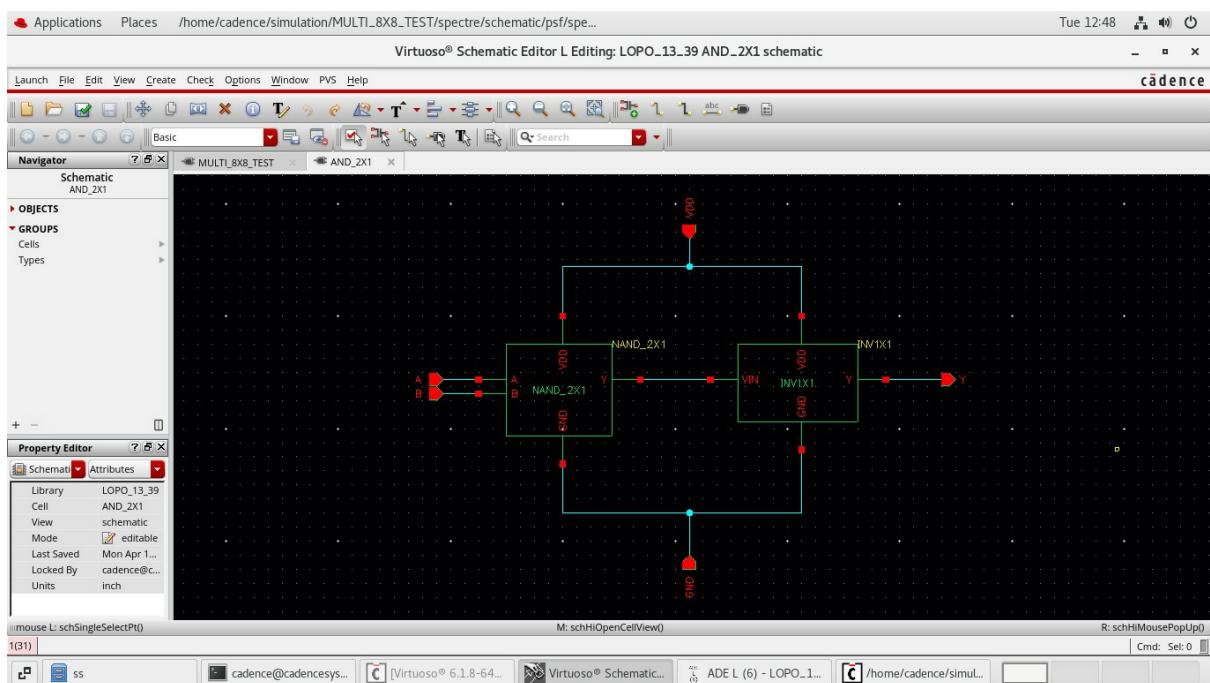
Functionality test:



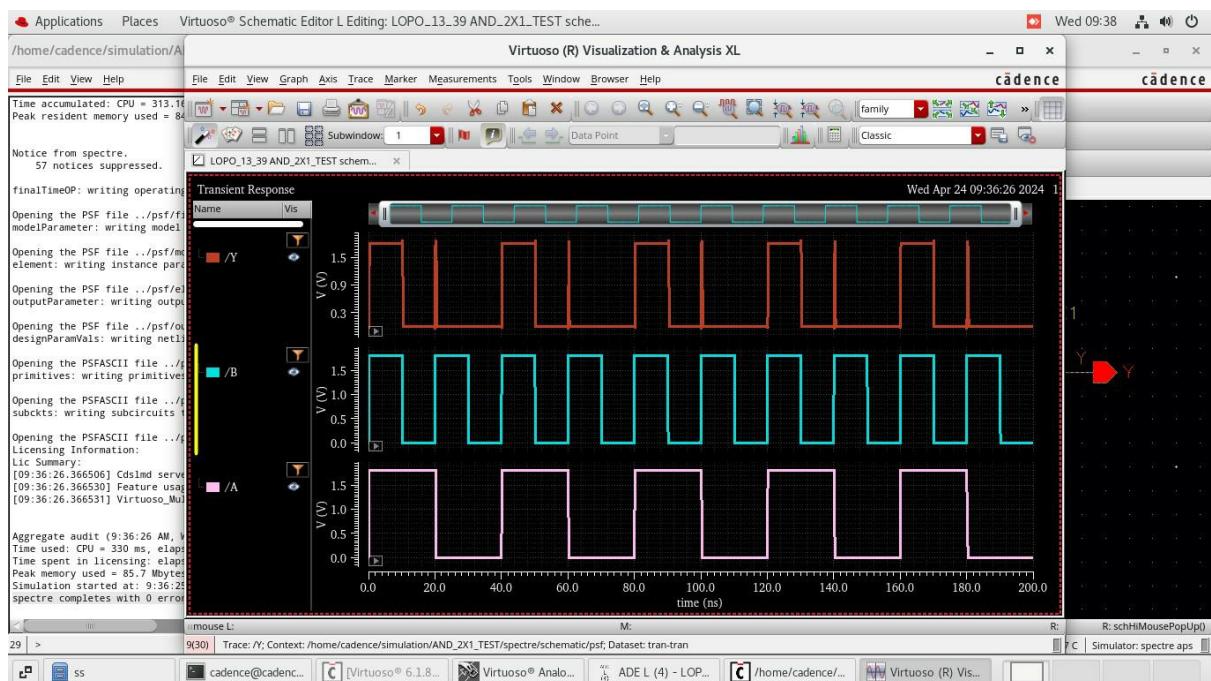
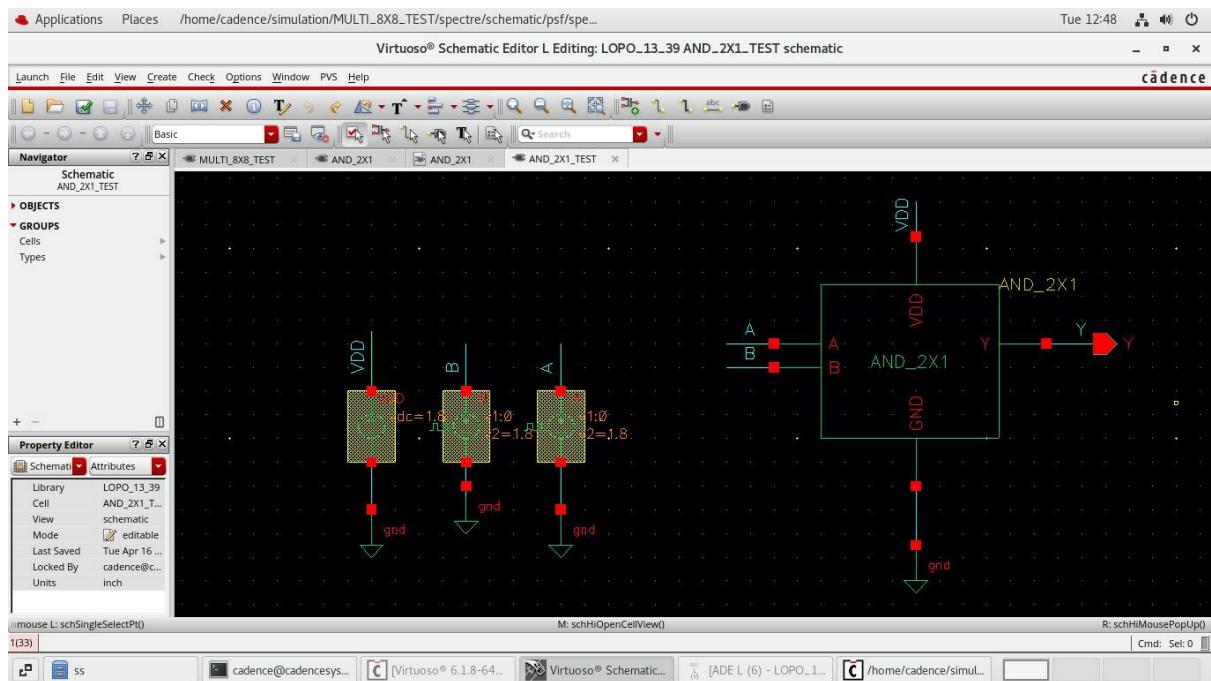


AND gate:

Schematic:

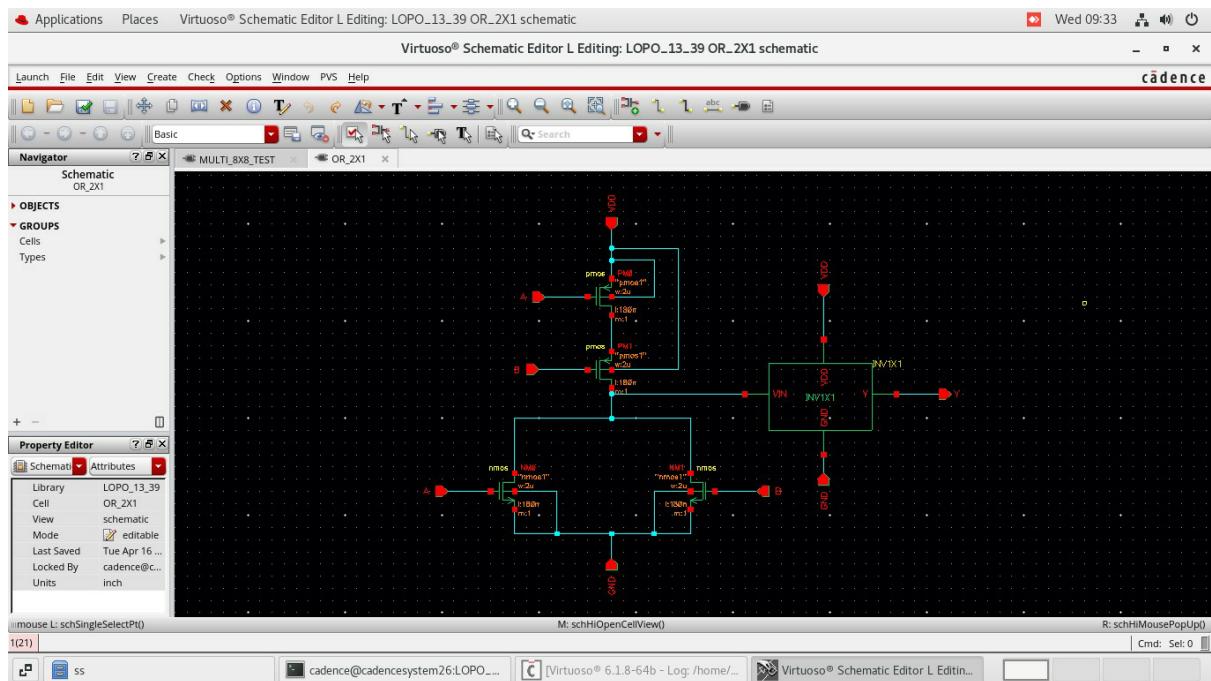


Functionality test:

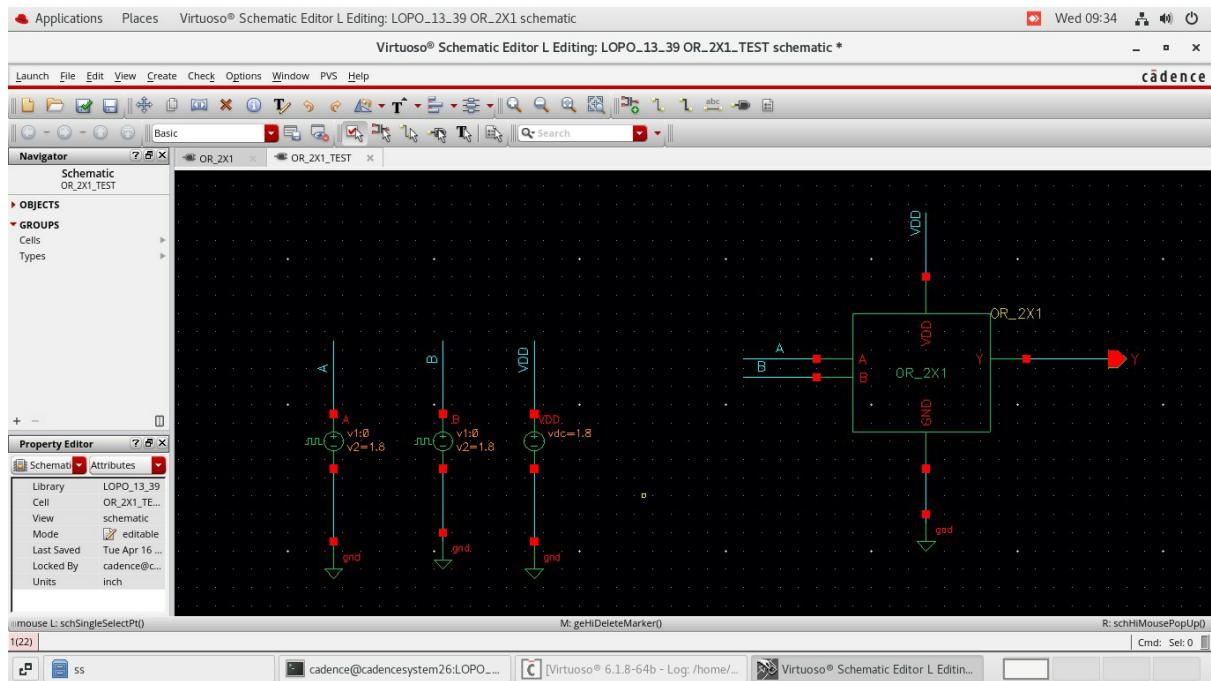


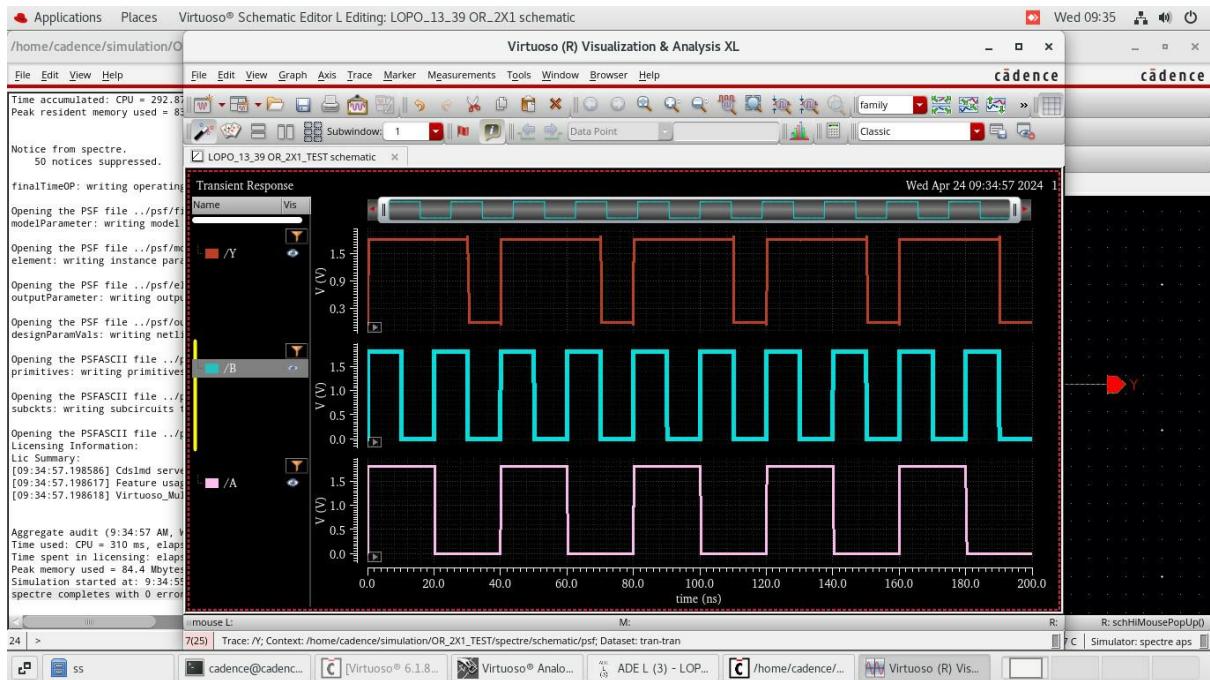
OR gate:

Schematic:



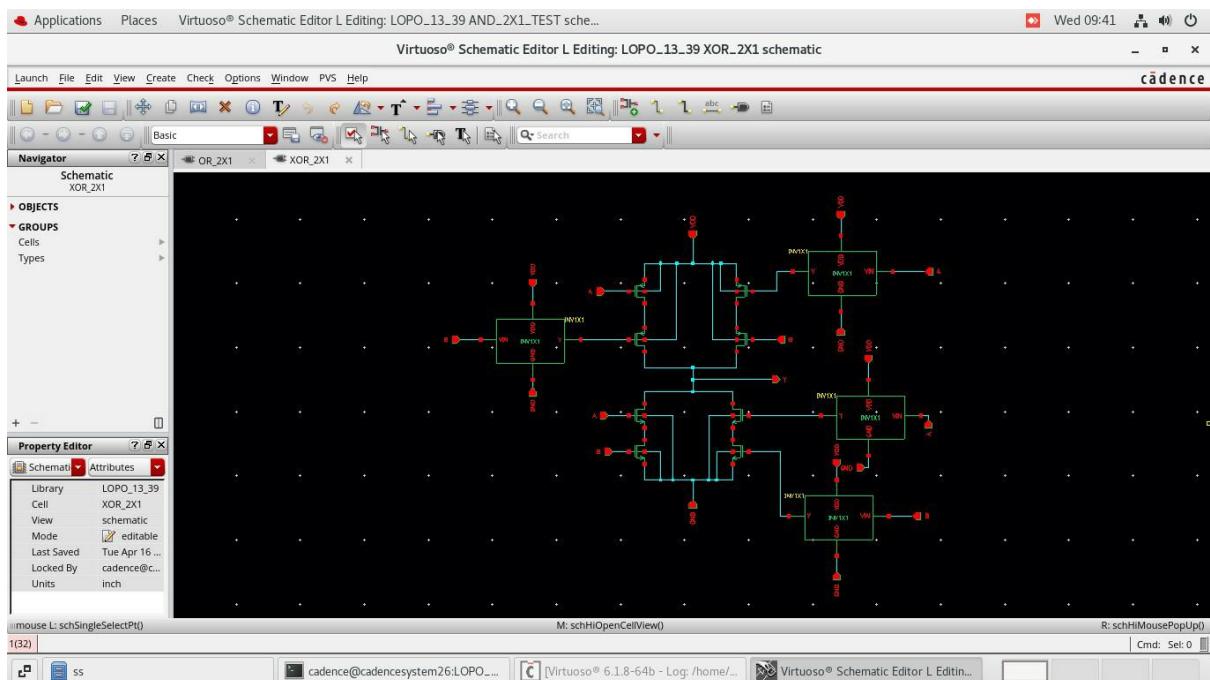
Functionality test:



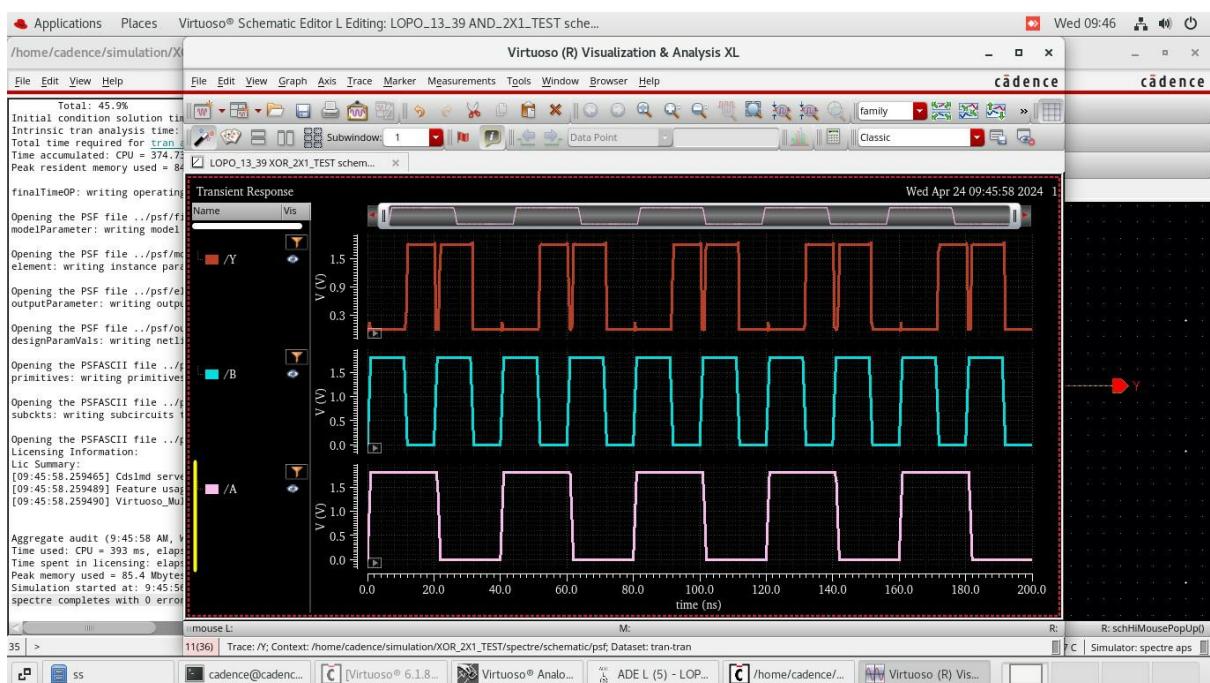
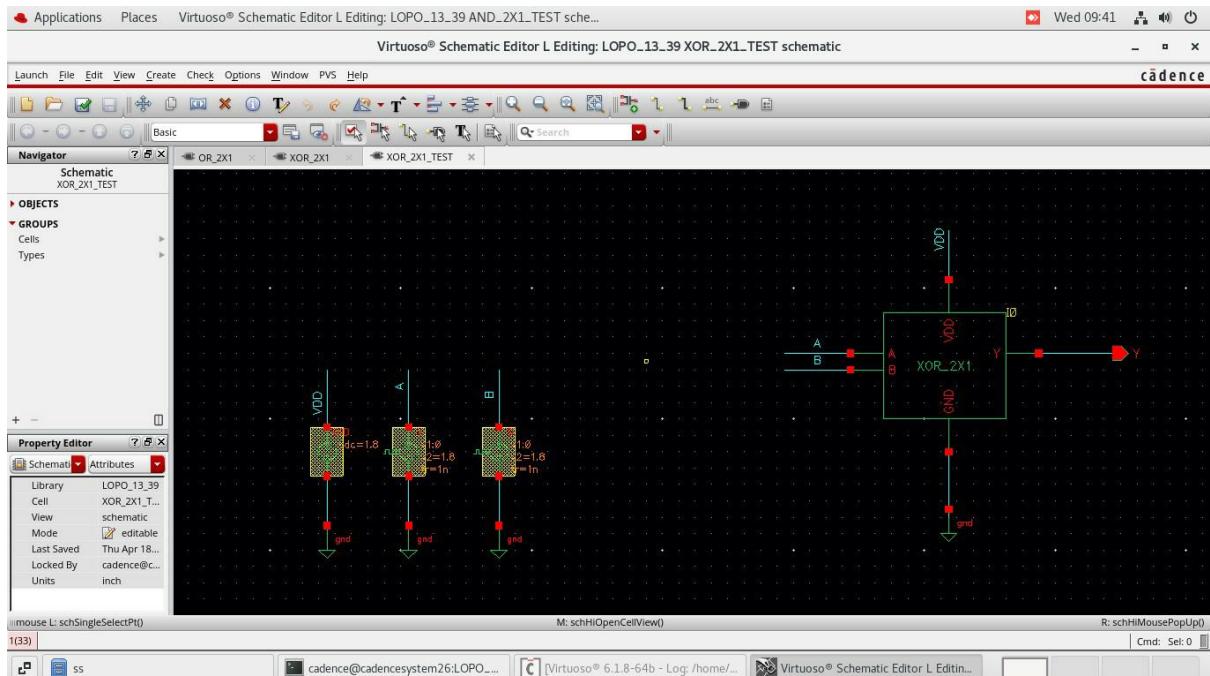


XOR gate:

Schematic:

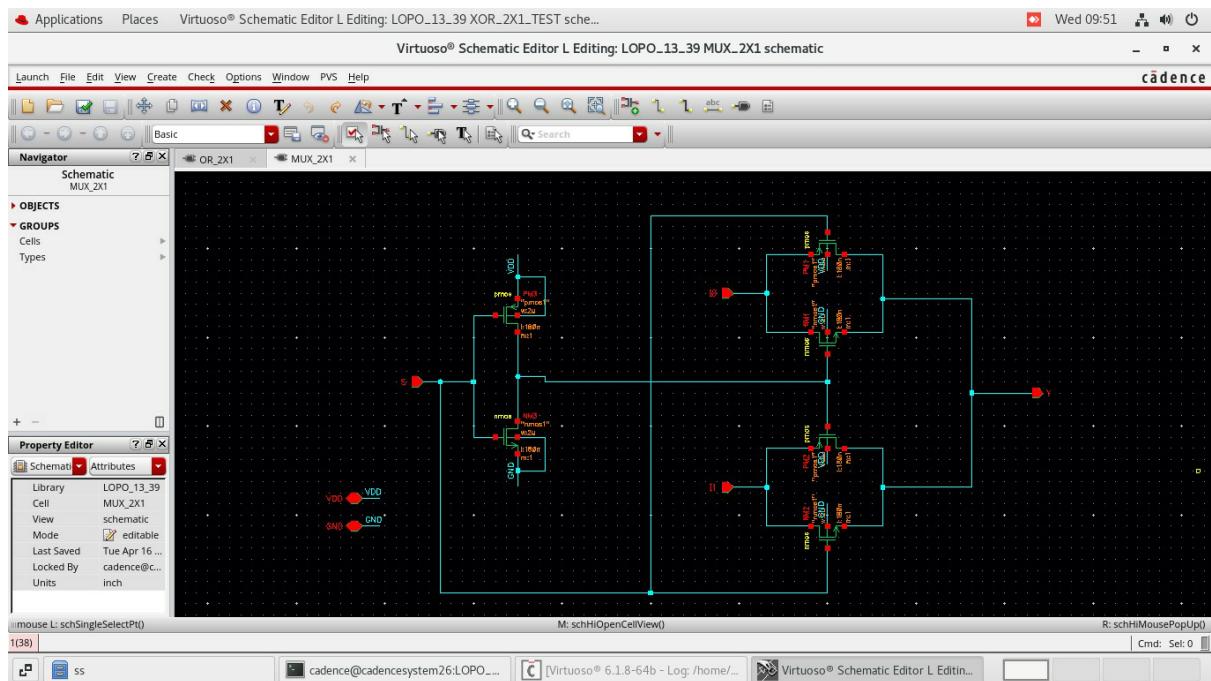


Functionality test:

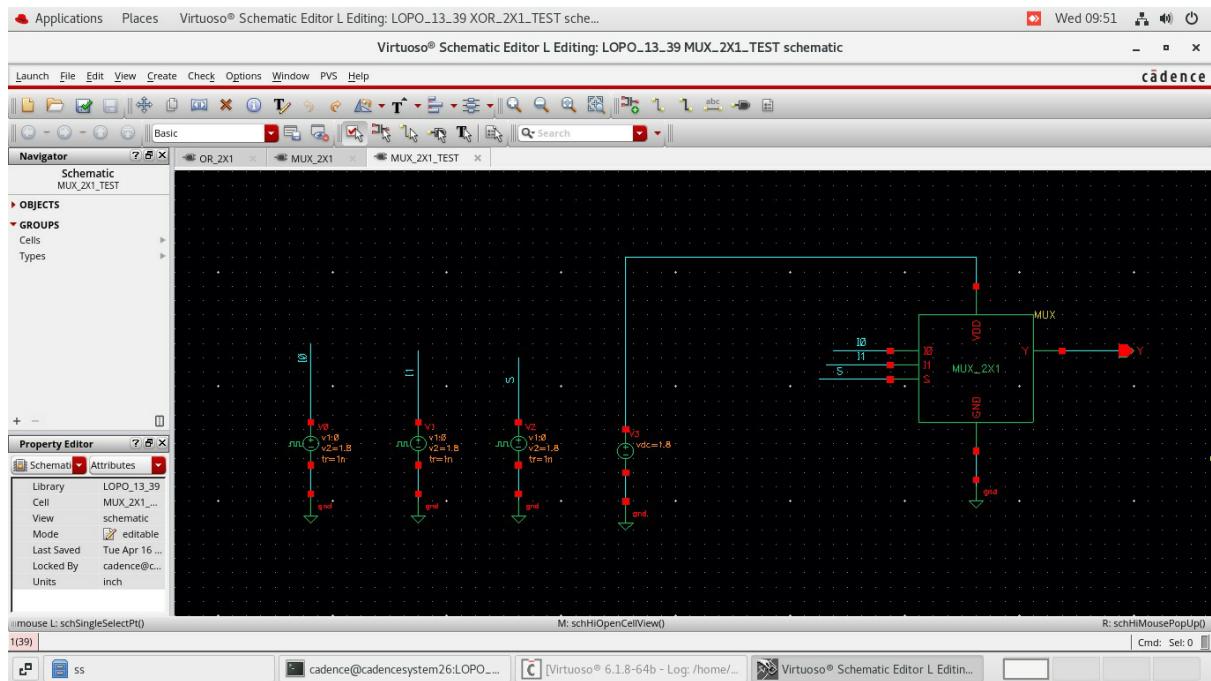


2:1 MUX:

Schematic:



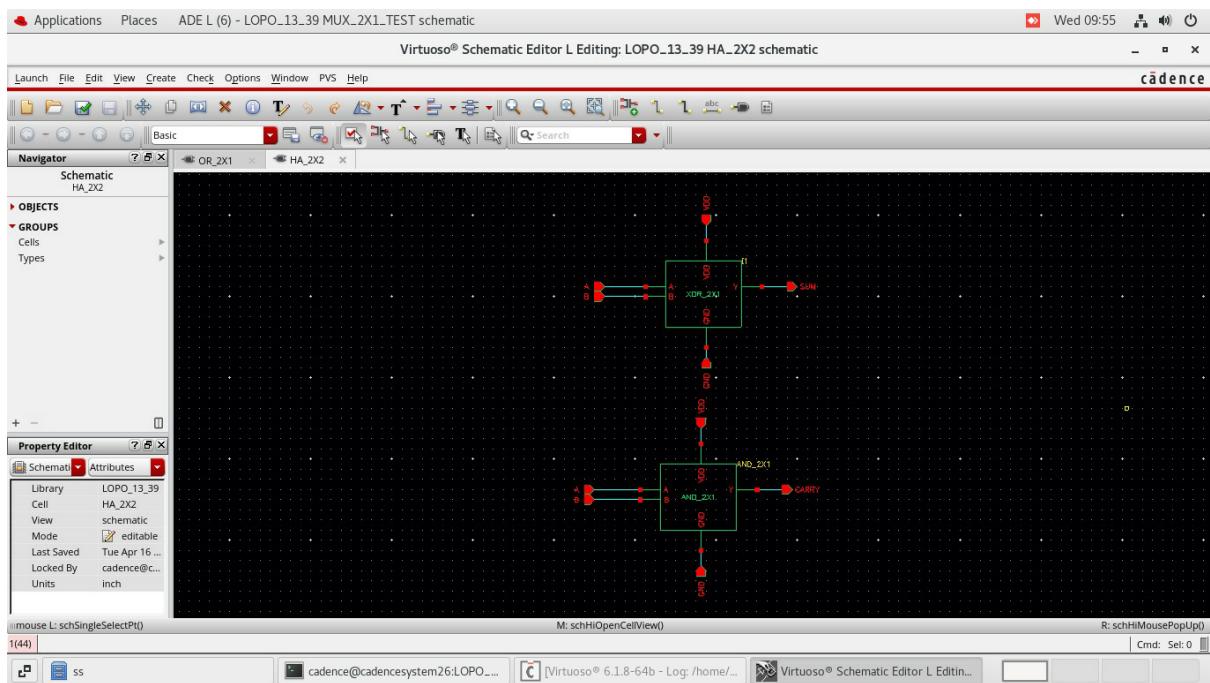
Functionality test:



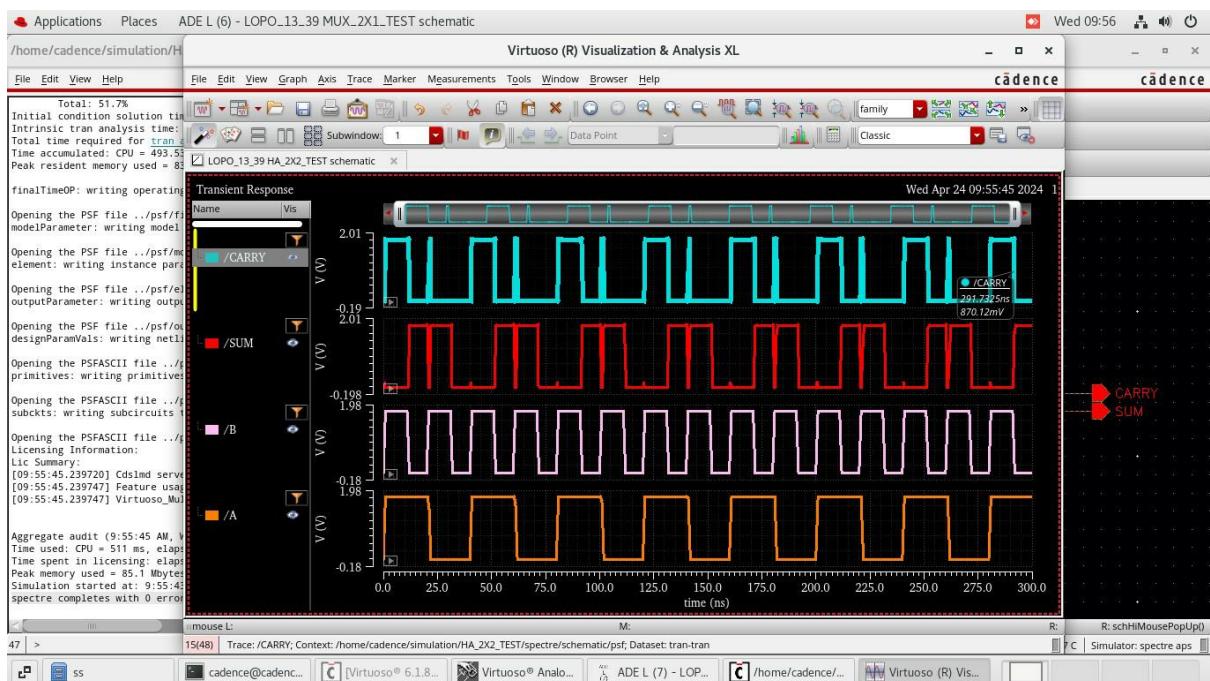
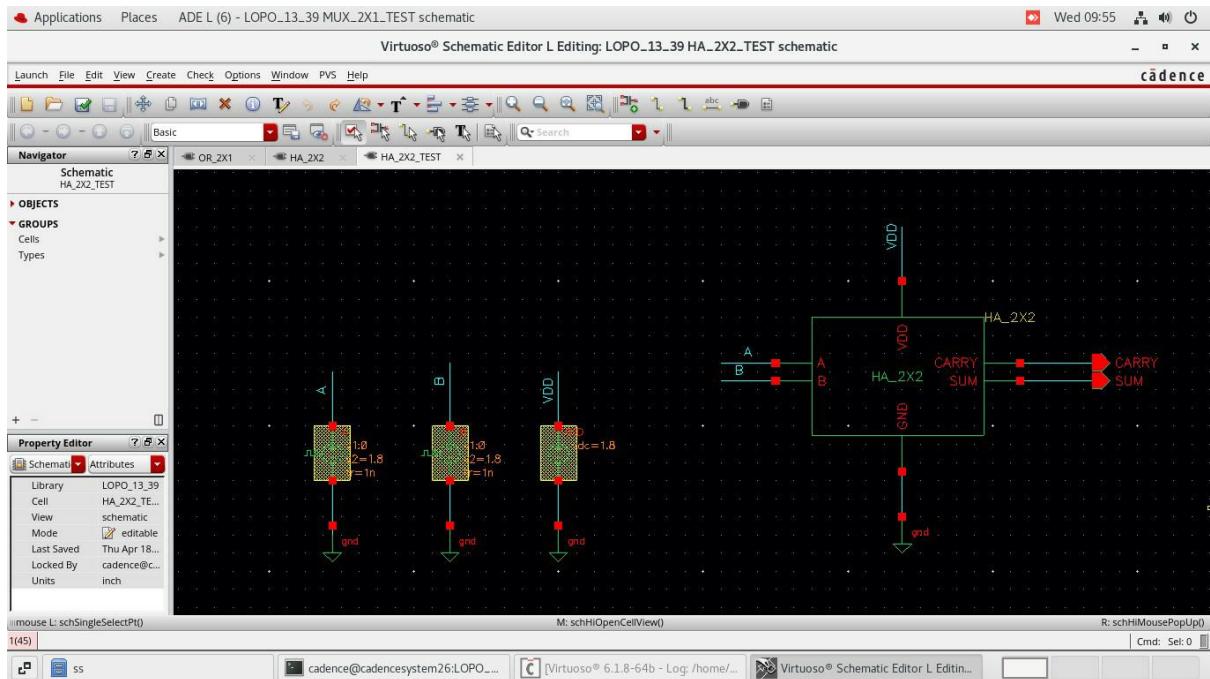


Half adder:

Schematic:

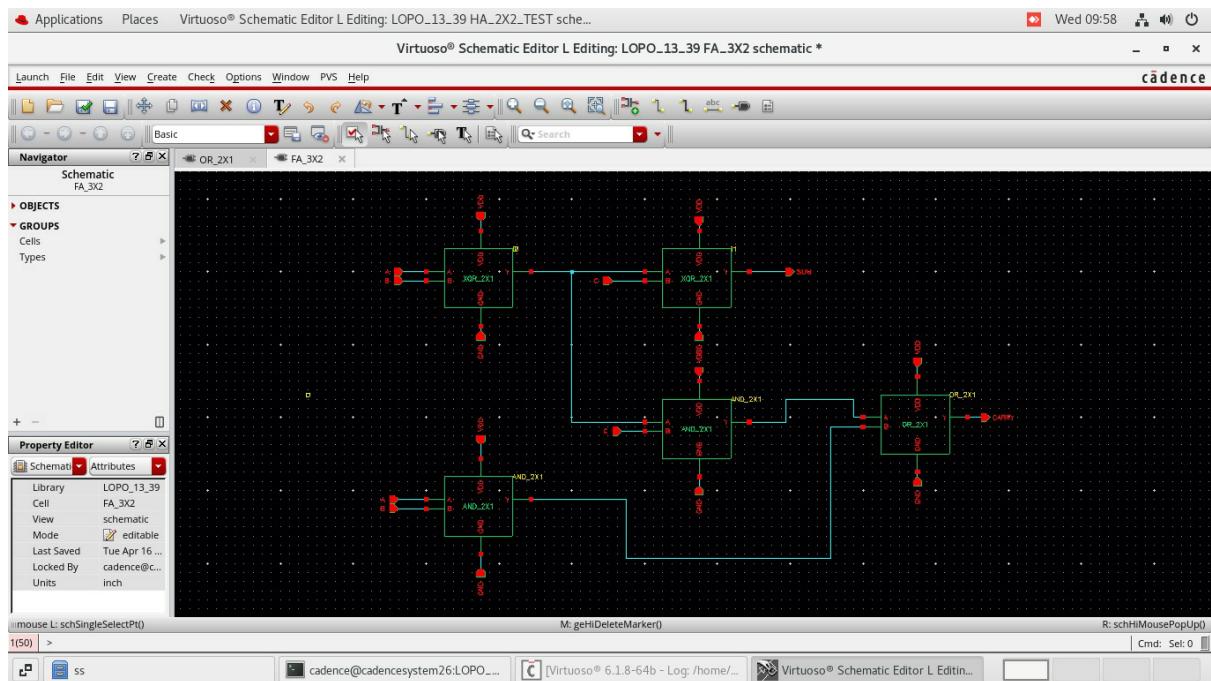


Functionality test:

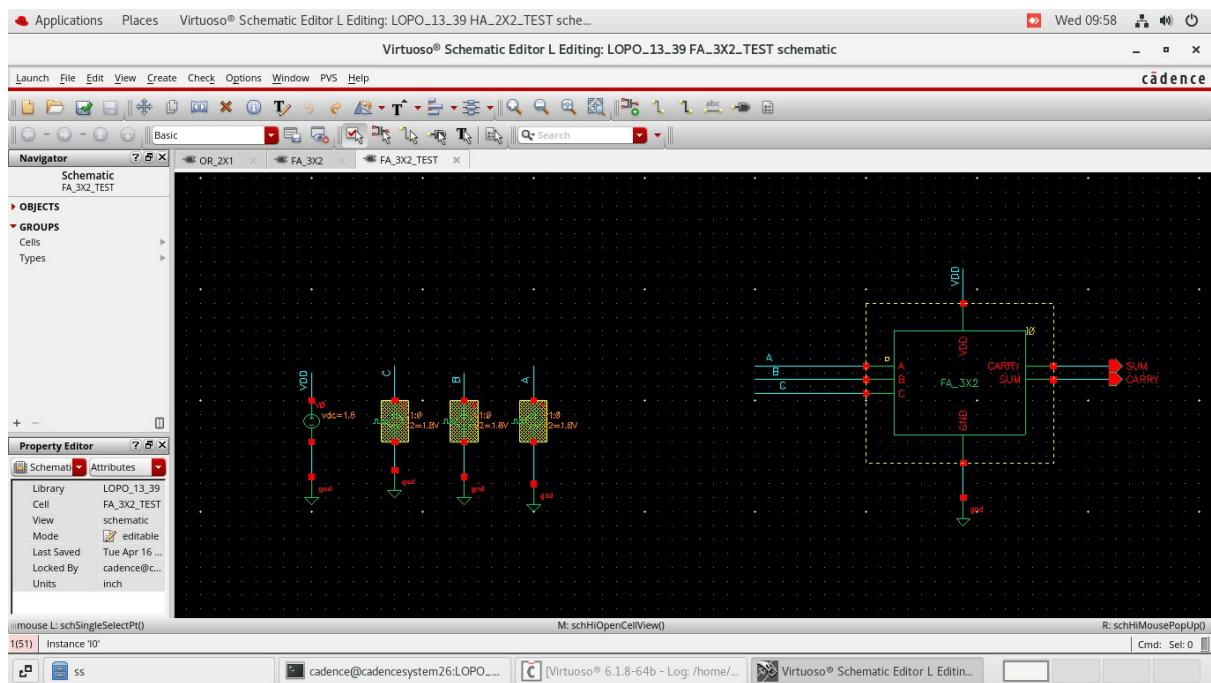


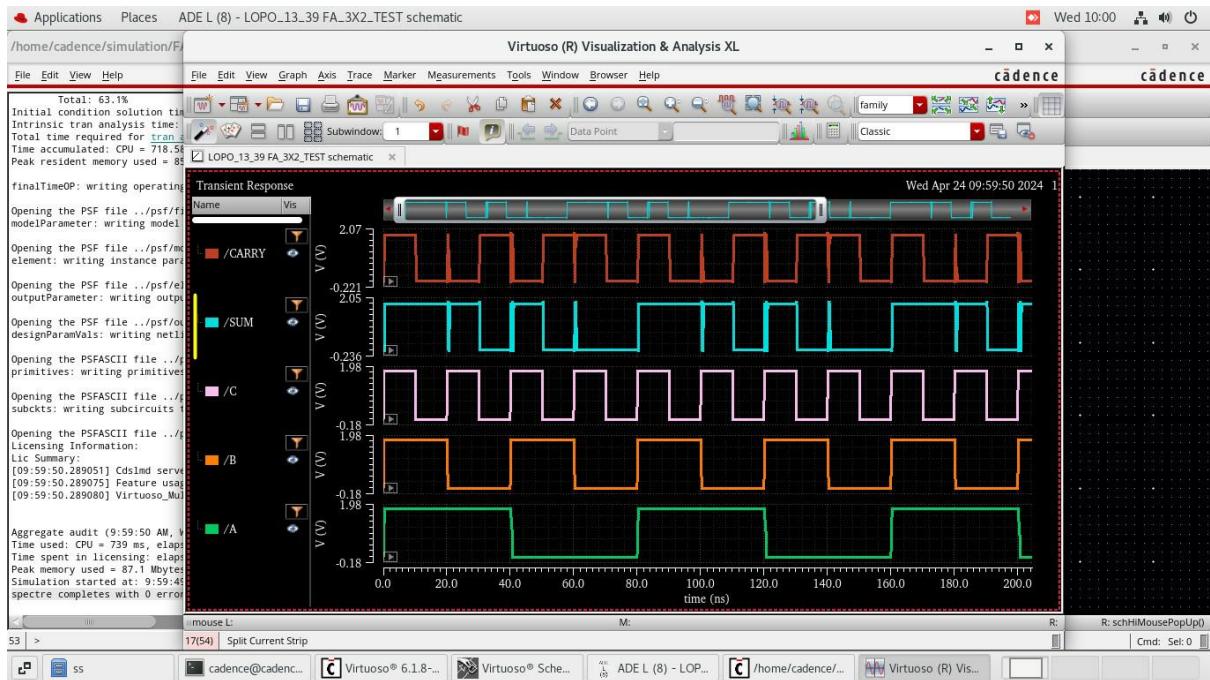
Full adder:

Schematic:



Functionality test:





2 bit Multiplier:

Using the above created cells we will implement a 2 bit multiplier.

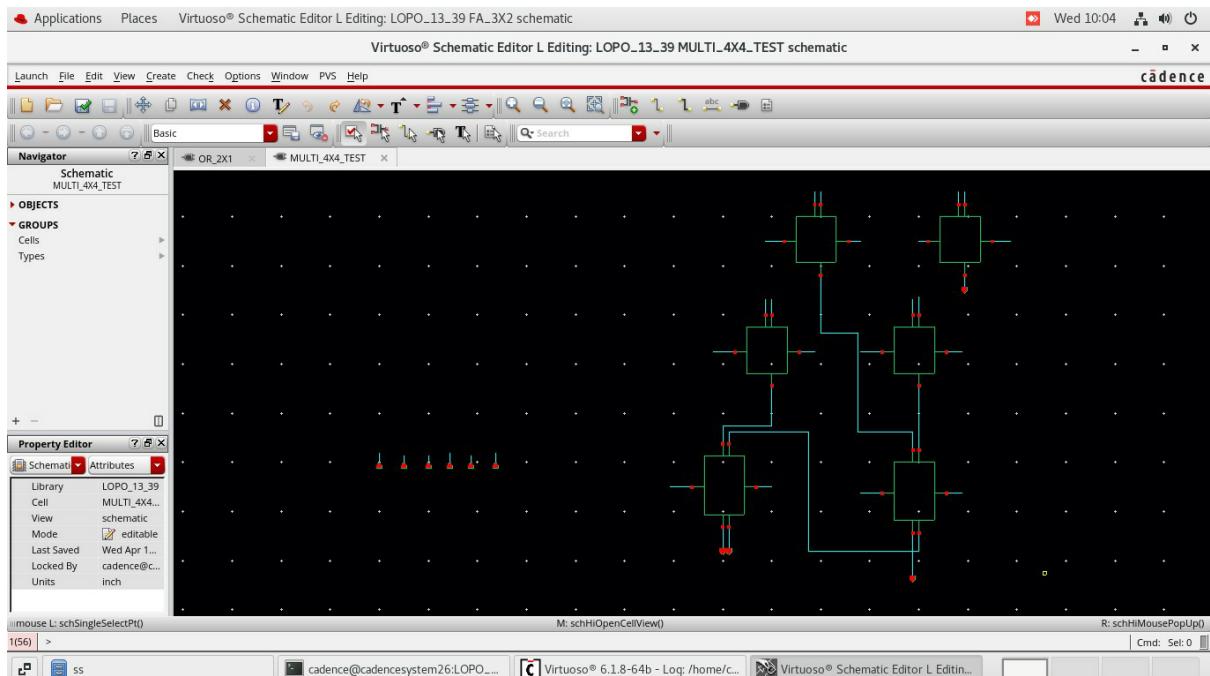
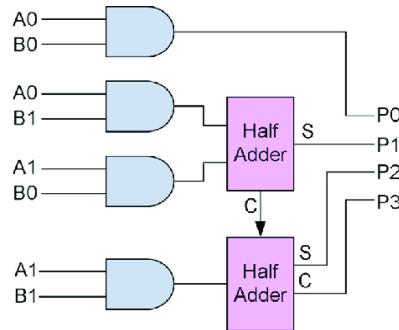
The truth table for the 2 bit multiplier is as follows:

A1	A0	B1	B0	R3	R2	R1	R0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

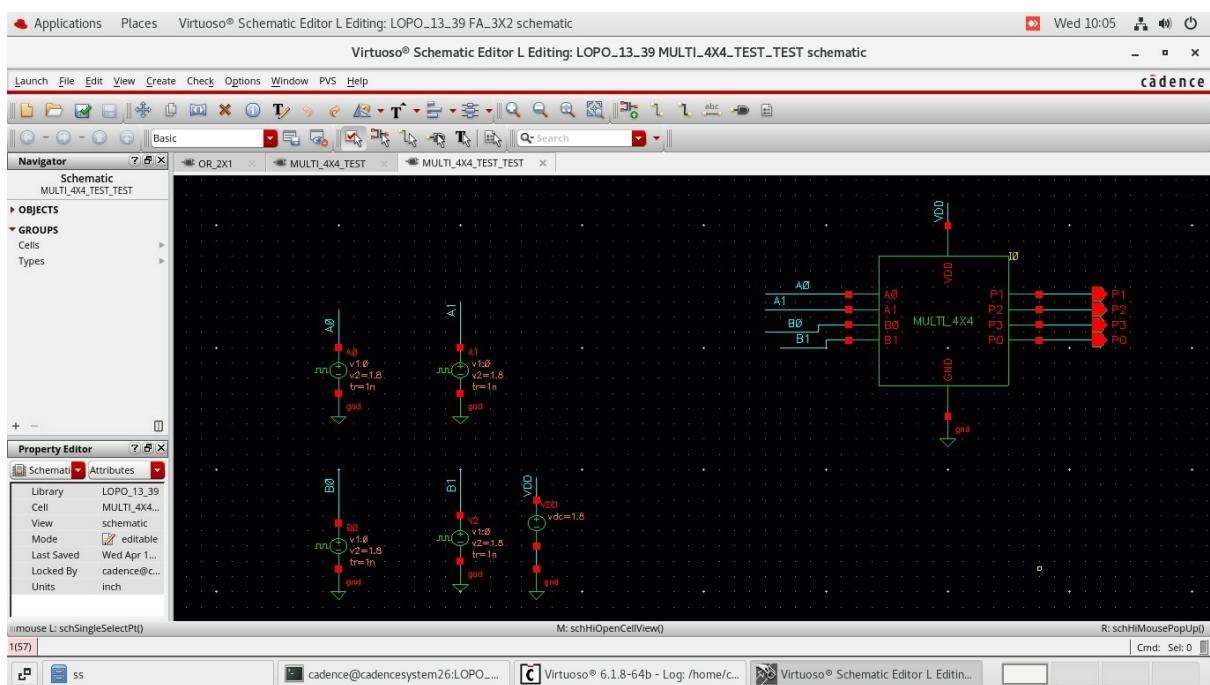
We are required to meet the values in the truth table in order to verify the functionality and proceed with the power calculations.

Schematic of 2 bit multiplier:

4 AND gates and 2 Half adders are used to construct a 2 bit multiplier. They are connected as shown.



Functionality test:



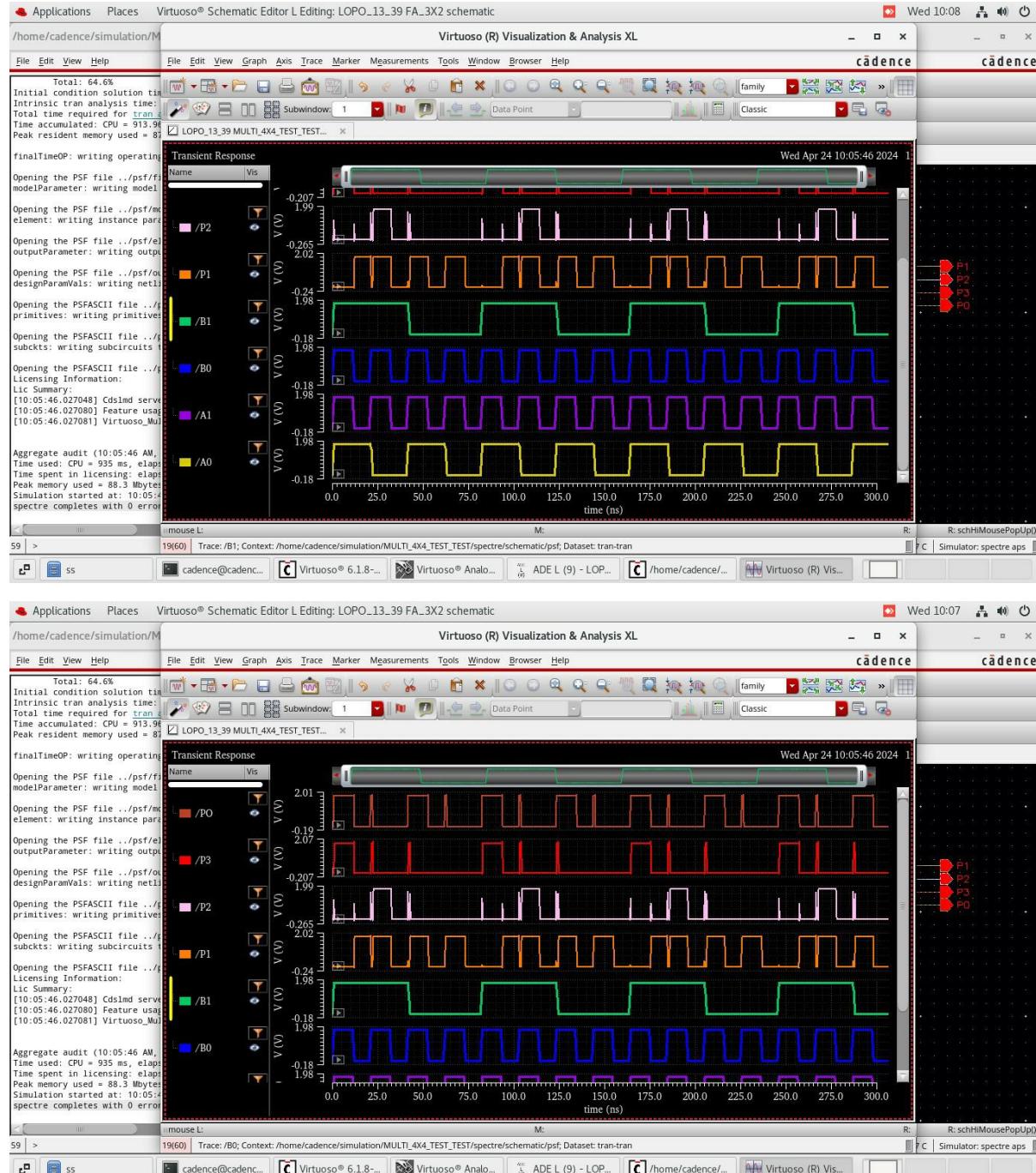
A0, A1 are the bits of the first input value.

B0, B1 are the bits of the second input value.

P0, P1, P2, P3 are the bit of the product.

MULT_4X4 is the symbol for the 2 bit multiplier.

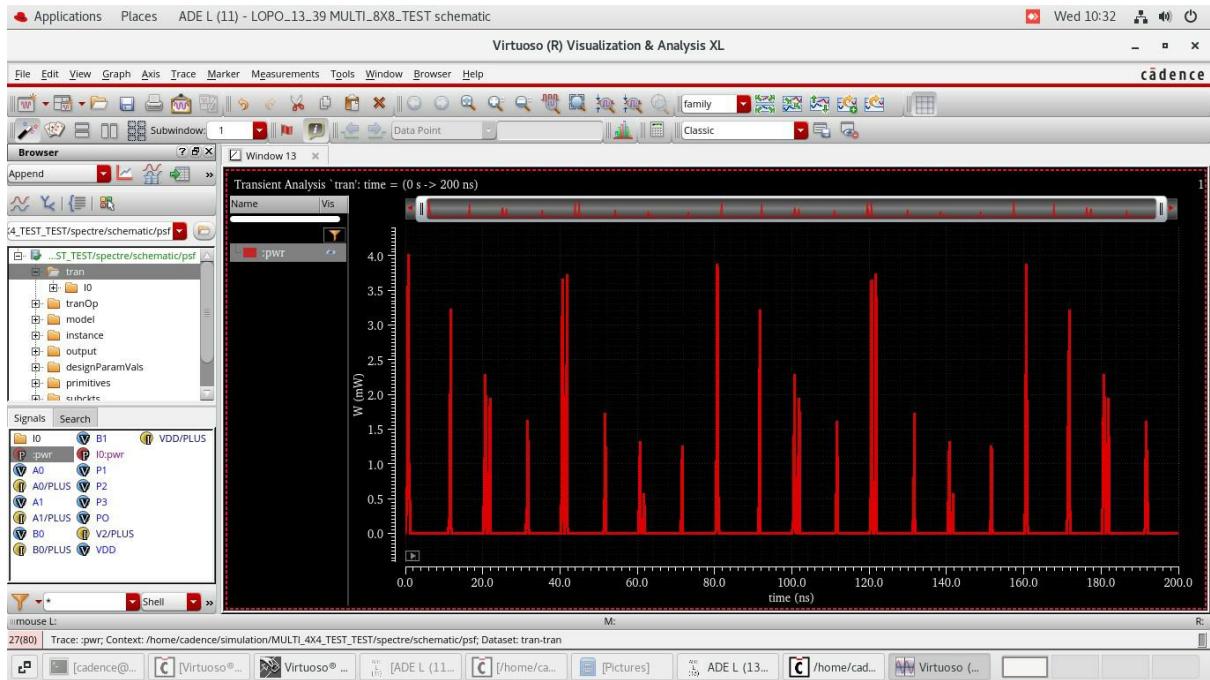
The waveforms for the 2 bit multiplier is as shown:



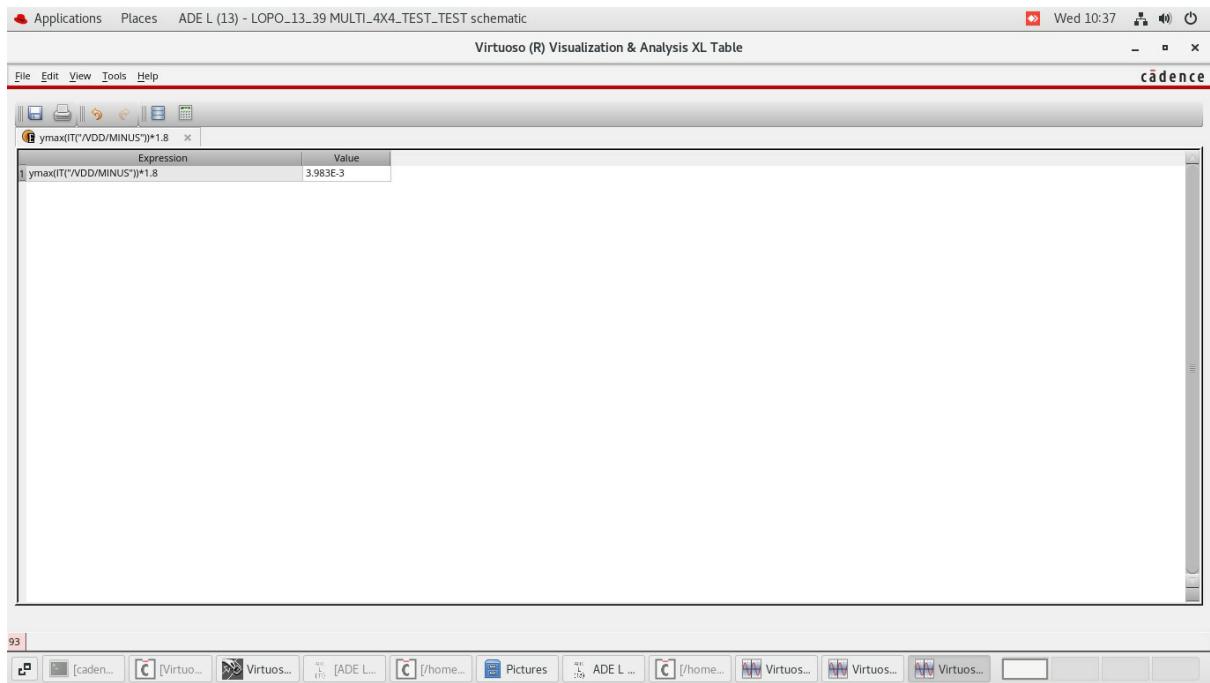
We observe that the behaviour of the waveform complies with the truth table and conclude that the 2 bit multiplier is functionally correct.

Power calculations:

The total power consumed vs time graph for the 2 bit multiplier is as shown:

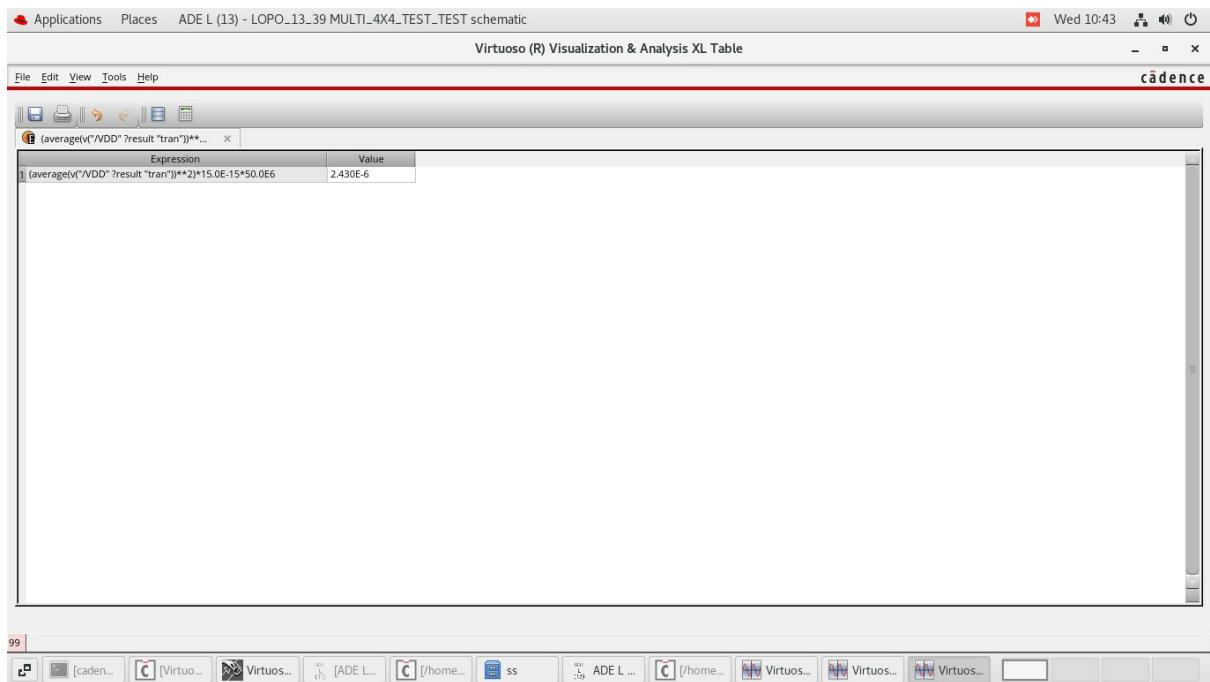


Static power is calculated as the product of Vdd and maximum Icc. Static power = 3.983 mW

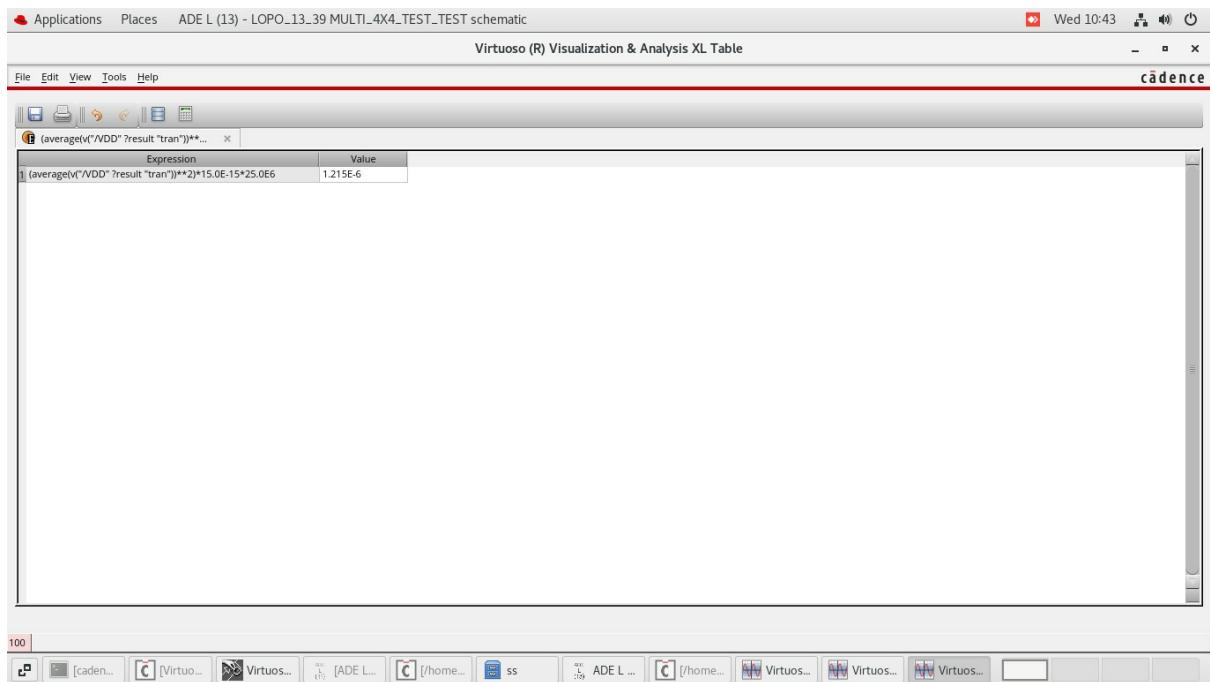


Dynamic power can be calculated for both maximum and minimum frequencies. Capacitance value is considered as 15 fF.

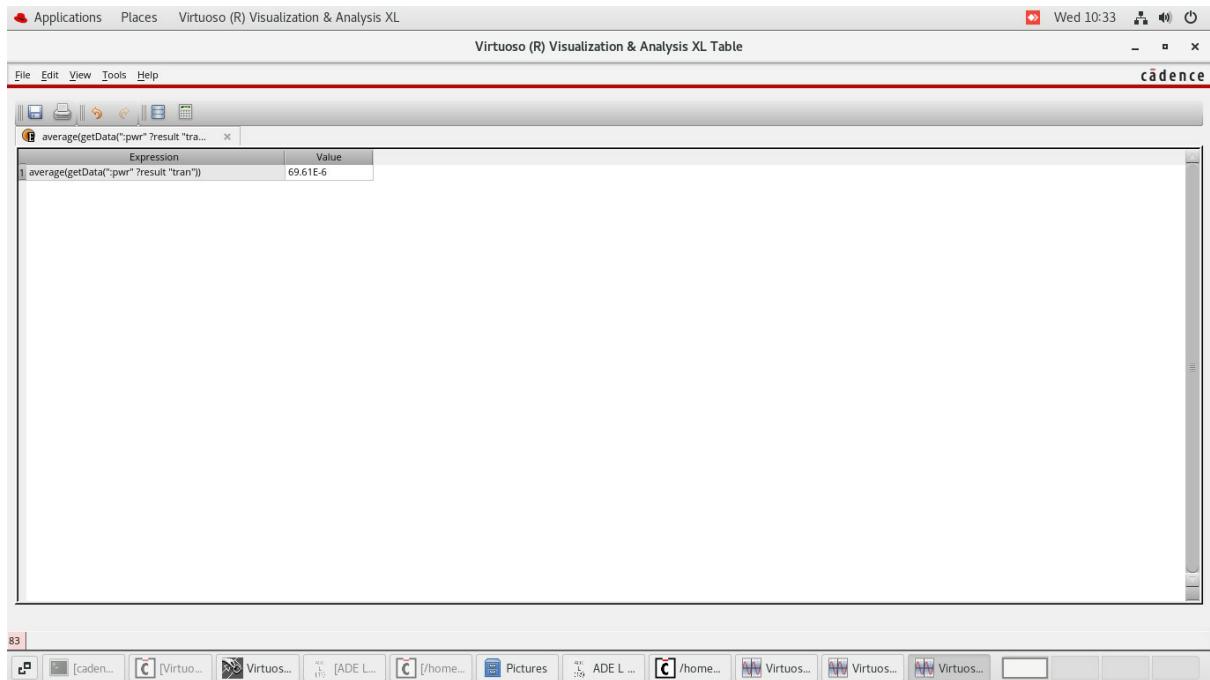
The input source with maximum frequency is A0 = 50 MHz (time period = 20 ns). Dynamic power = 2.43 uW.



The input source with minimum frequency is $B_0 = 25 \text{ MHz}$ (time period = 40 ns). Dynamic power = 1.21 uW.

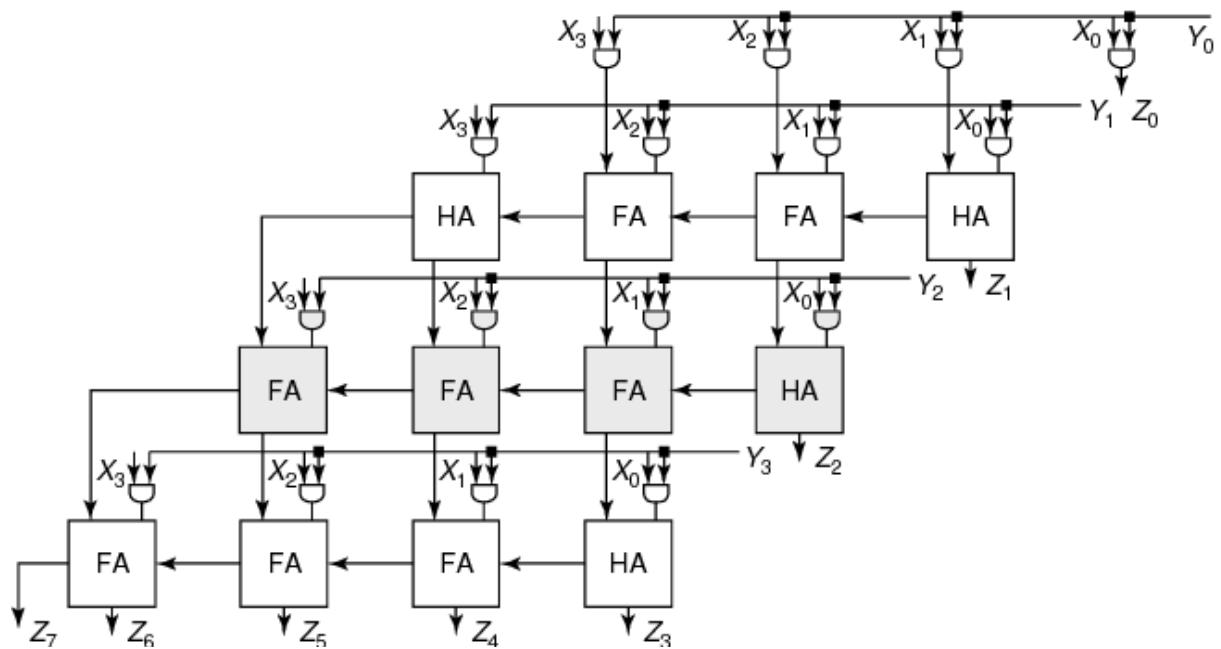


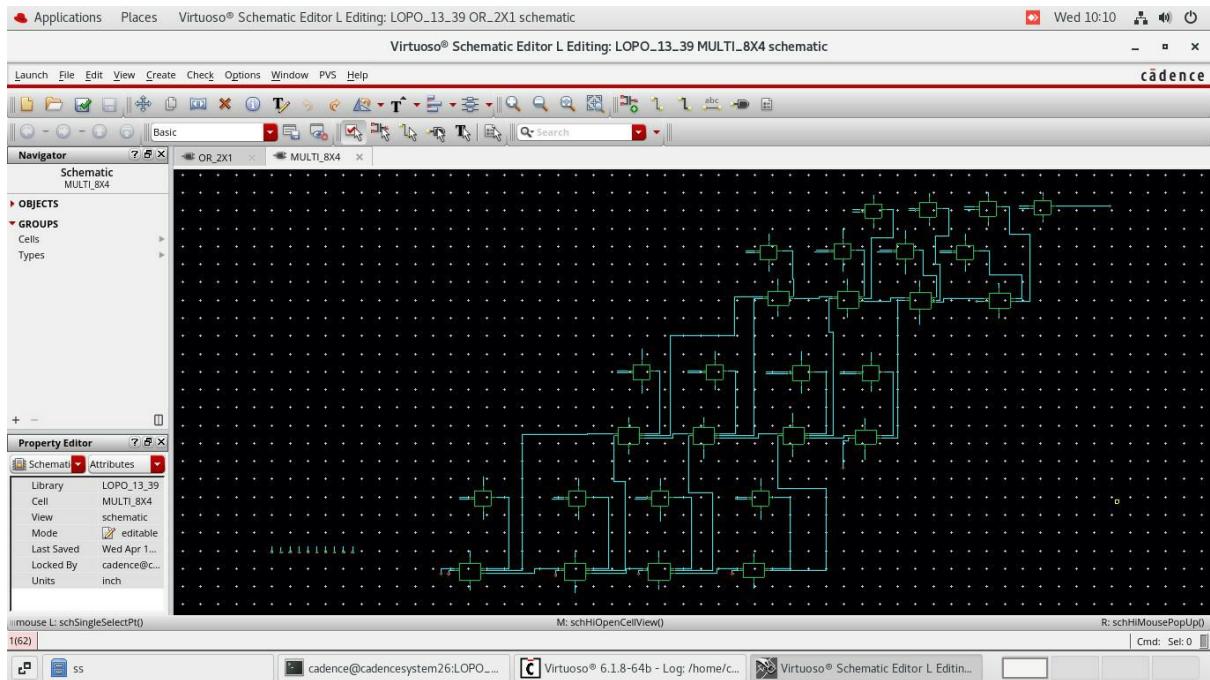
Average power is calculated using the total power vs time graph. Average power = 69.61 uW.



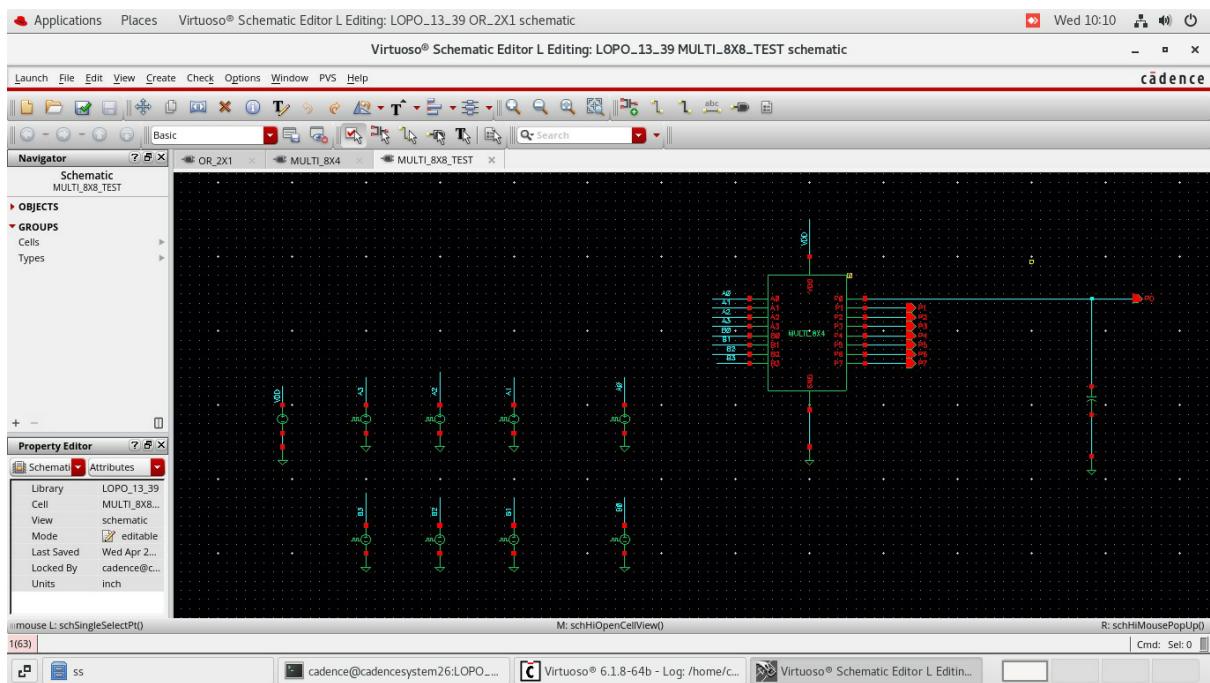
4 bit Multiplier:

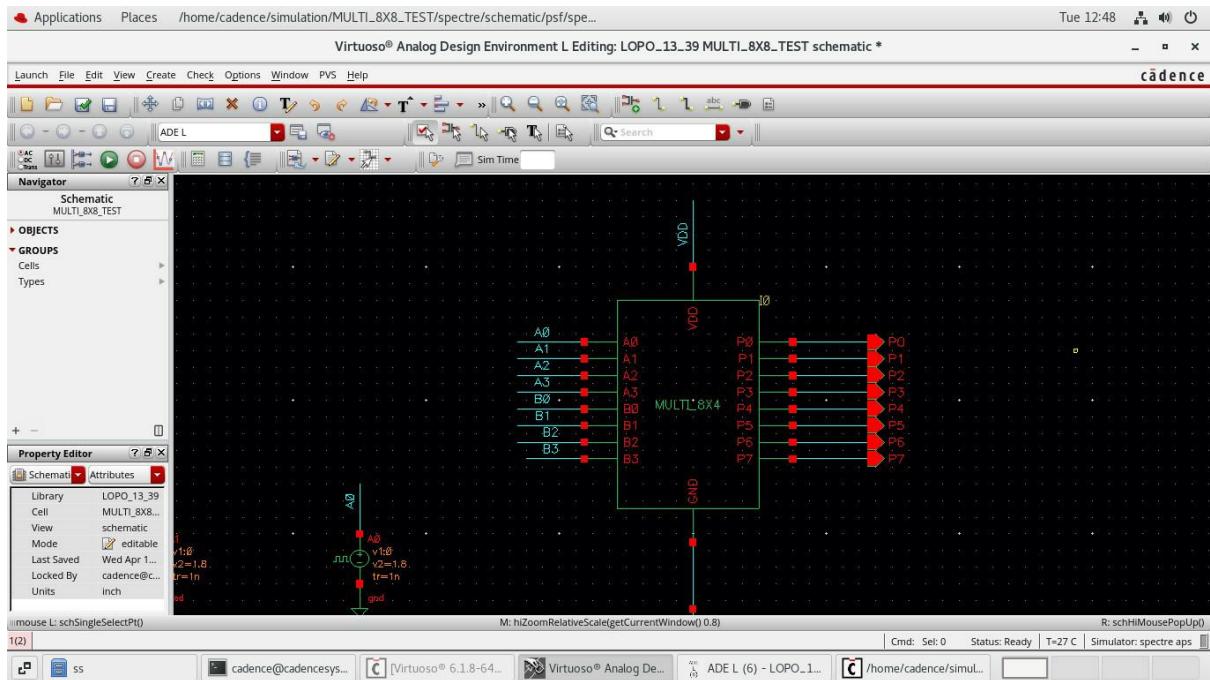
The schematic of a 4 bit multiplier uses 16 AND gates 4 half adders and 8 Full adders.





Functionality test:



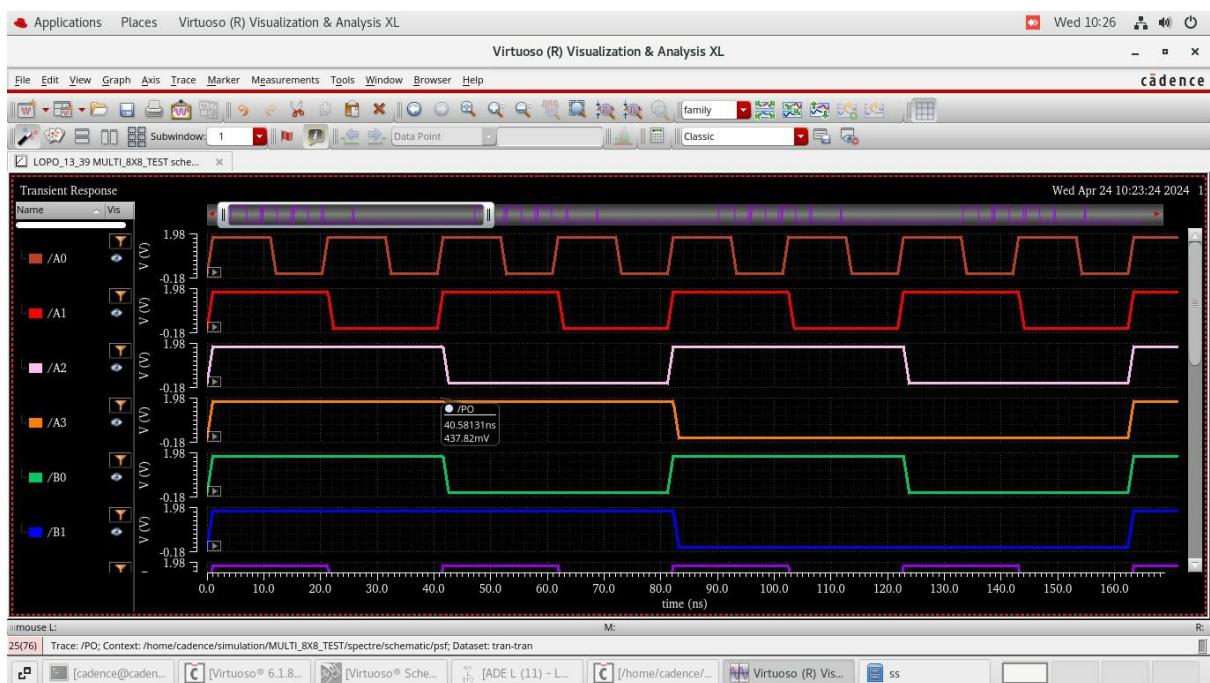


A0, A1, A2, A3 are the bits of the first input value.

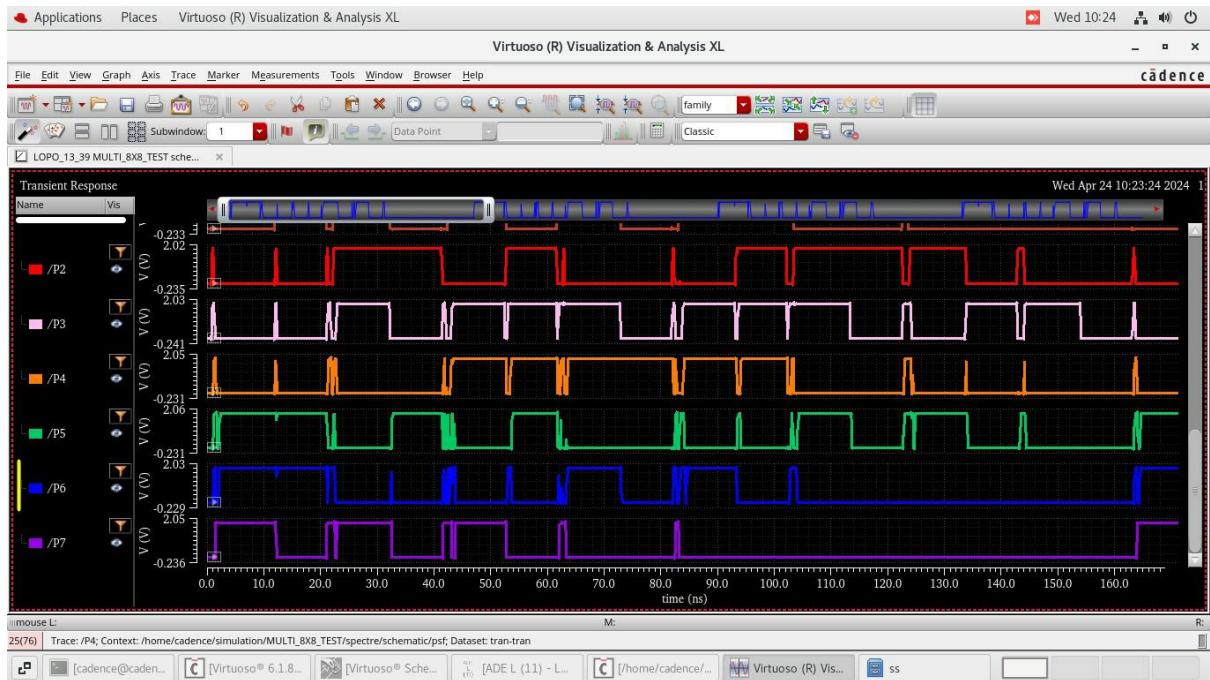
B0, B1, B2, B3 are the bits of the second input value.

P0, P1, P2, P3, P4, P5, P6, P7 are the bits of the product.

The waveforms of the 4 bit multiplier is as shown:



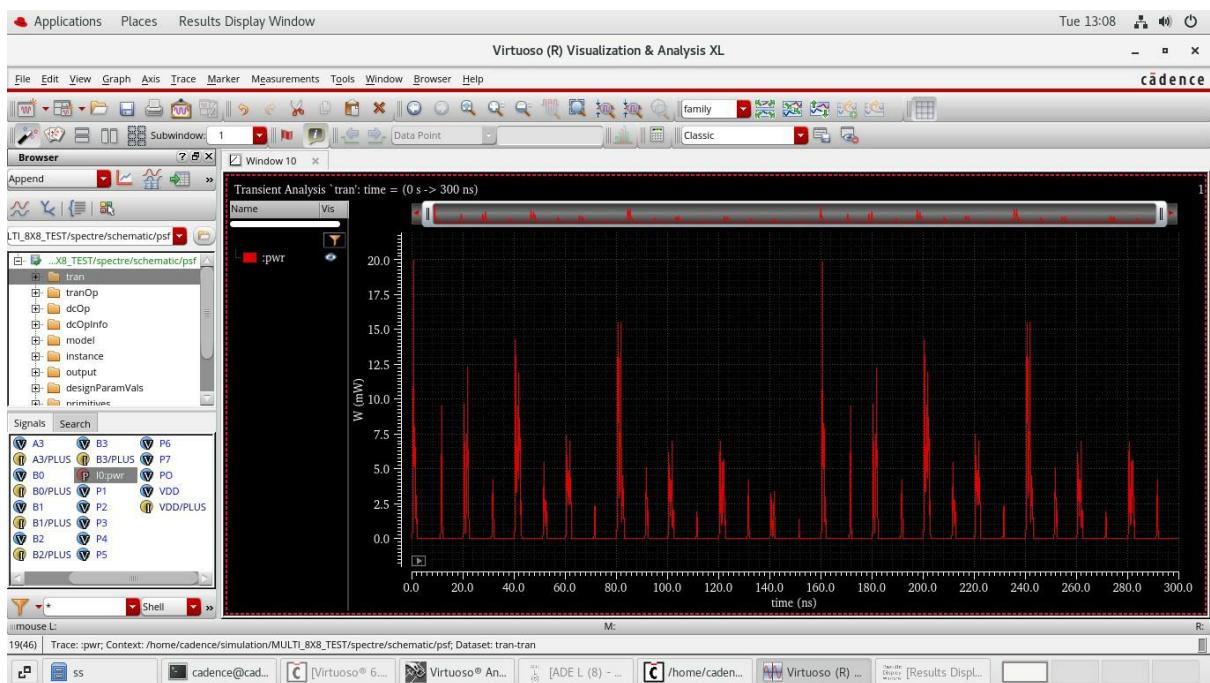




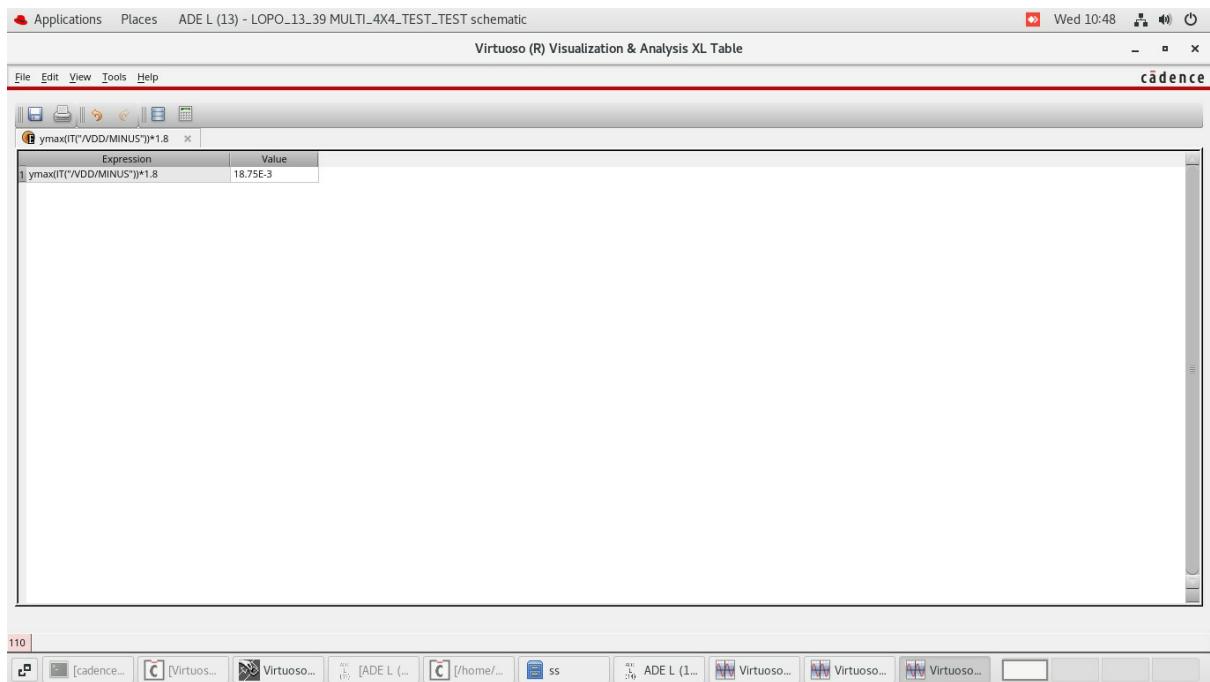
By observing the waveform and comparing it with the truth table for 4 bit multiplier, we can conclude that the results match and the 4 bit multiplier is functionally correct.

Power calculations:

The total power consumed vs time graph for the 4 bit multiplier is as shown:

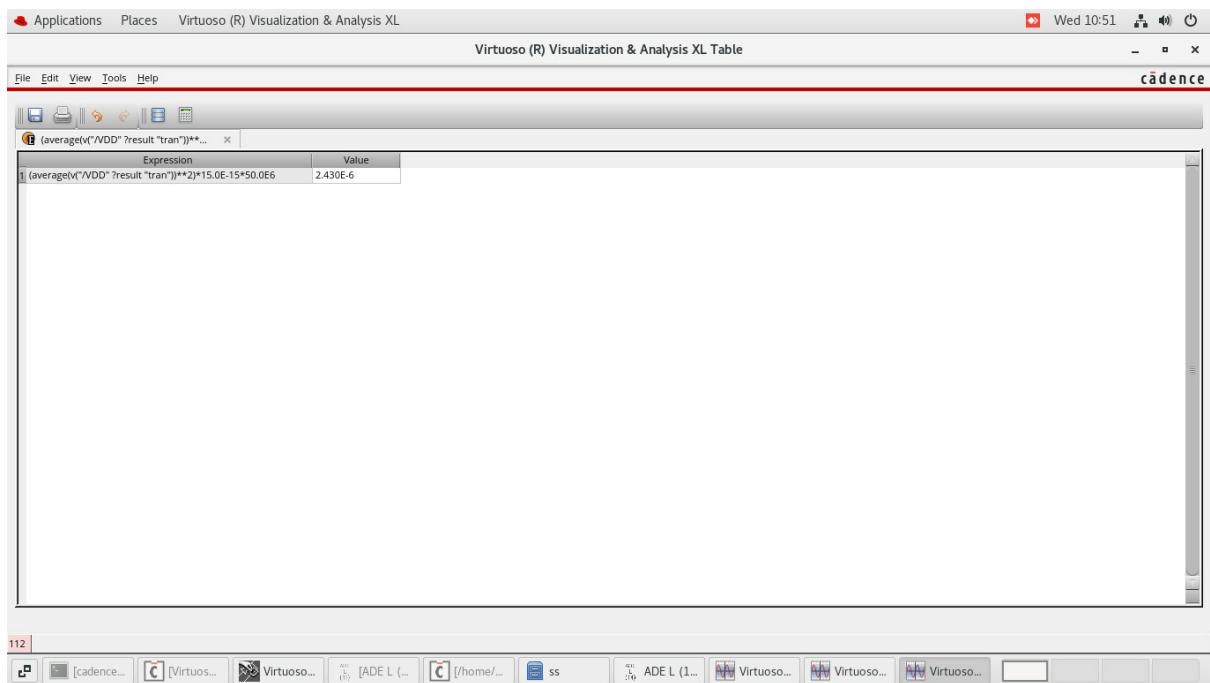


Static power is calculated as the product of Vdd and maximum Icc. Static power = 18.75 mW.

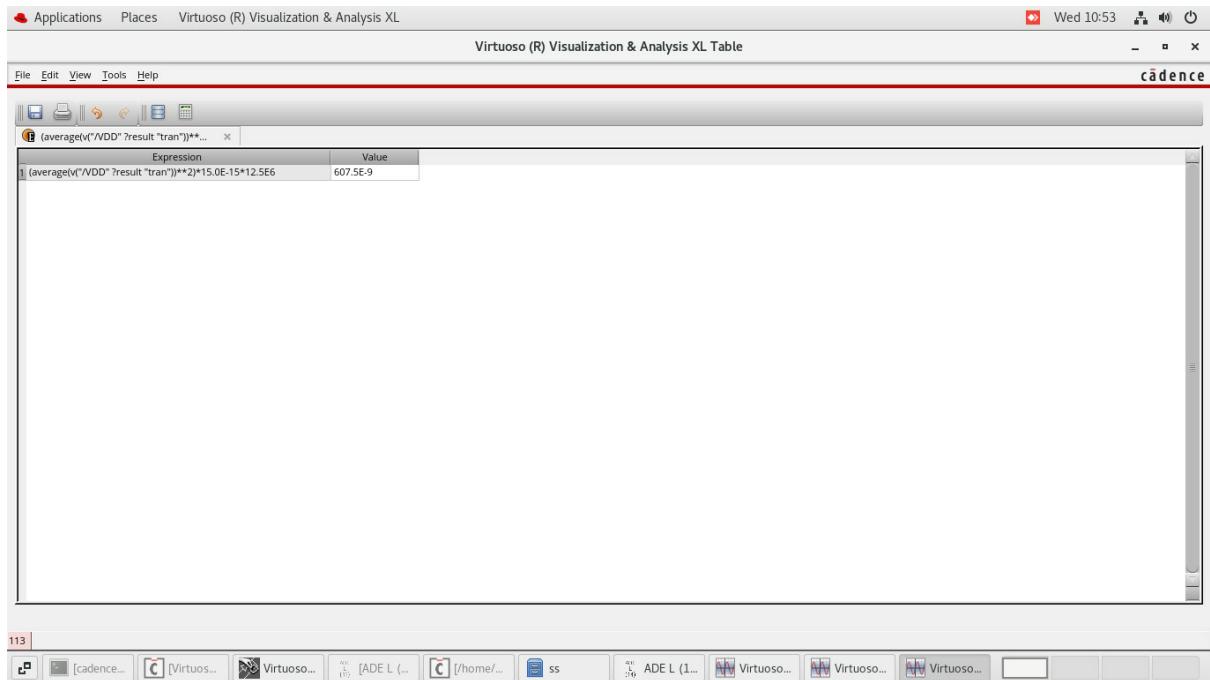


Dynamic power can be calculated for both maximum and minimum frequencies. Capacitance value is considered as 15 fF.

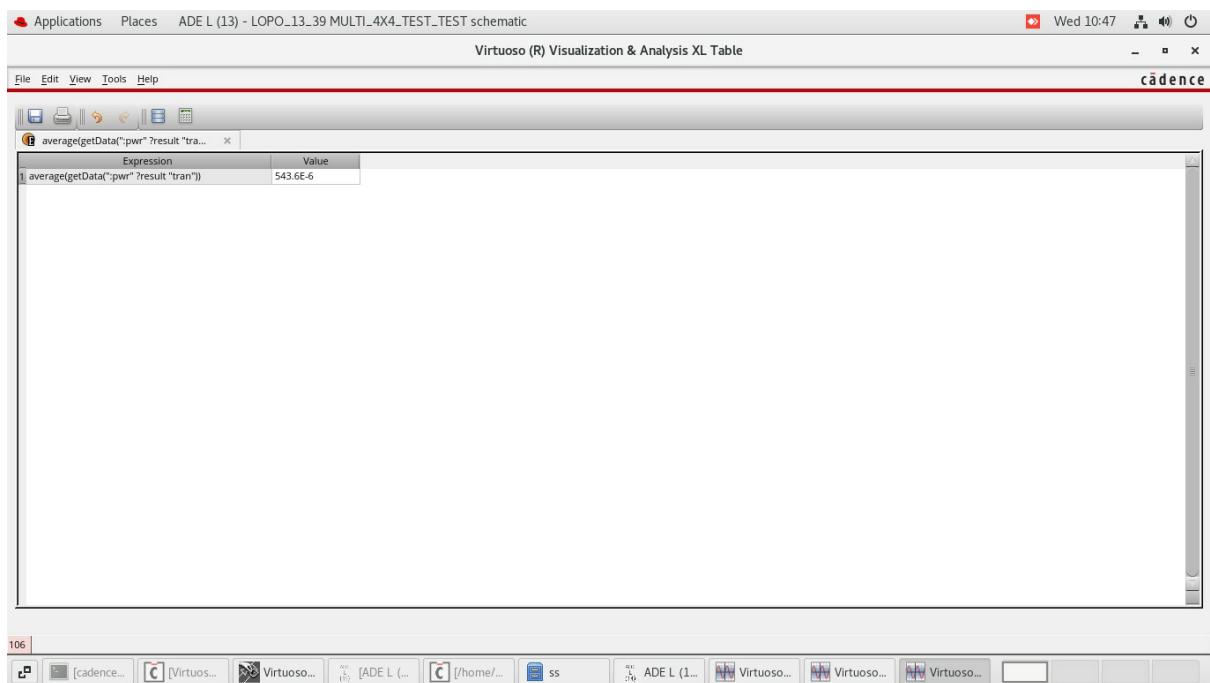
The input source with maximum frequency is $A_0 = 50 \text{ MHz}$ (time period = 20 ns). Maximum Dynamic power = 2.43 uW.



The input source with minimum frequency is $B_0 = 12.5 \text{ MHz}$ (time period = 80 ns). Minimum Dynamic power = 607.5 nW.



Average power is calculated using the total power vs time graph. Average power = 543.6 uW.



Conclusion:

In this project we analysed the different types of powers (average power, dynamic power and static power) that are encountered when designing any digital circuit from scratch using CMOS technology. We also understood the role of the different components that come to play during power analysis. The power calculations were done manually as well in order to verify the results.