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Slot: E11 + E12 + E13
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1 (b) (1)

$v = 325 \sin 314t$ L - R series circuit

$i = 14.14 \sin (314t - 60°)$

Calculate L, R and power consumed.

→

$V = 325 \sin 314t$

$v = V_m \sin \omega t$

So, $V = \frac{V_m}{\sqrt{2}}$ (RMS $= \frac{325}{1.414} = 229.8 \sim 230V$.

Now, $2\pi f = \omega = 314$

$$f = \frac{314}{2 \times 3.14} = 50 \text{ Hz}$$

Now, $i = I_m \sin(\omega t - \phi)$ is similar to $i = 14.14 \sin (314t - 60°)$

$\therefore I_m = 14.14$

now $I = \frac{I_m}{\sqrt{2}}$ (RMS value)

$\therefore I = \frac{14.14}{1.414} = 10 \text{ A}$

$\phi = 60°$

$\therefore$ Power factor $= \cos\phi = \cos 60 = \frac{1}{2}$

$P = VI \cos\phi = 230 \times 10 \times \frac{1}{2}$

$= 1150 \text{ W}$

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Impedance $= Z = \frac{V}{I} = \frac{230 \angle 0}{10 \angle -60^\circ} = 230 \angle 60^\circ \Omega$

Now, Z can be denoted as, $Z = 23(\cos 60 + j \sin 60)$

$= 23 \times \frac{1}{2} + j \times 23 \times \frac{\sqrt{3}}{2}$

$= 11.5 + 19.918\, j$

$= R + j X_L$

$\therefore R = 11.5\ \Omega$

$X_L = 19.918$

$WL = 19.918$

$L = \frac{19.918}{2\pi \times 50} = \frac{19.918}{2 \times 3.14 \times 50} = \frac{19.918}{314} = 0.063\ H$

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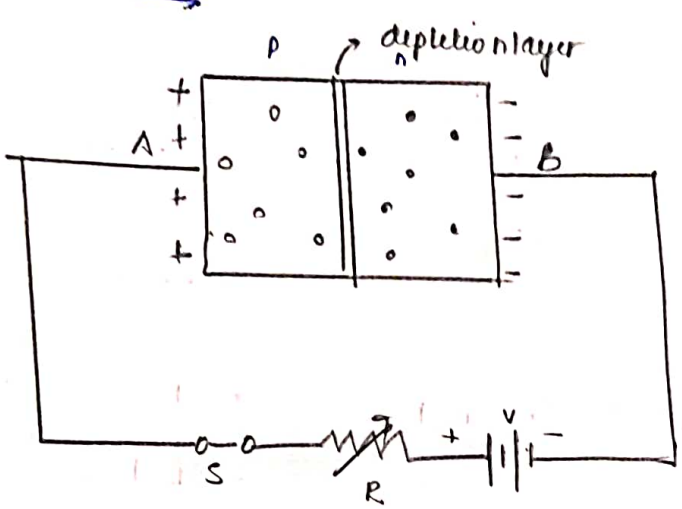
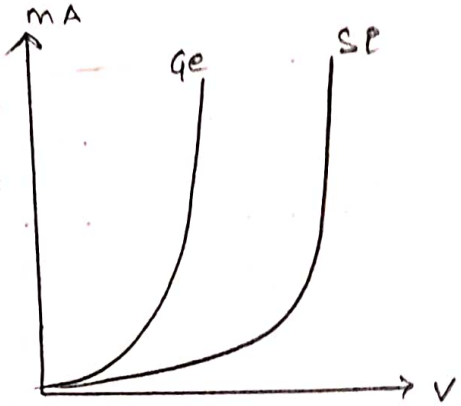
2

Biasing of p-n junction

When p side is connected to +ve to battery and n is connected to negative of battery, p-n junction is forward biased. and if it is connected opposite ⇒ then it is reverse biased.

FORWARD BIAS





The holes on p side are + and e^- on n side are negative., when current is passed, the positive terminal of battery will repel the holes from terminal. similarly electrons are repelled from negative side. As a result. the width of depletion layer will reduce. The potential barrier will also get reduced. If voltage is gradually increased, the depletion region and barrier potential will disappear

The forward voltage V, v/s I_F characteristics for germanium and silicon, the graph shows the forward current increases. Thus in forward biased p-n junction, potential barrier is neutralised allowing current flow.

⟹ **TYPES OF CURRENTS** → The current flowing due to majority carriers & minority carriers.

* Transient current: An oscillatory or aperiodic current that flows in a circuit for a short time ~~fluct~~ following an Electromagnetic disturbance
* surface leakage current: Diode reverse current that passes along the surface of semiconductor materials.

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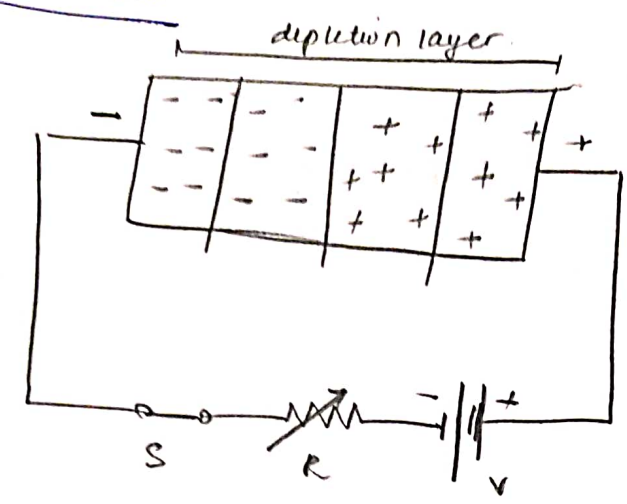
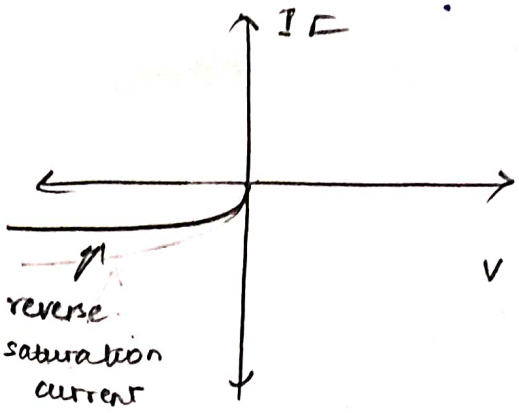
Reverse bias





Reverse V-I char

Since the holes of the p side are attracted to negative terminal and electrons on positive side, the depletion layer widens as applied voltage increases The barrier voltage also increases as such the majority charge carriers crossing the barrier is reduced to zero. As minority charges are very less, small current (mA) will flow. The number of minority charges carriers are small and very less voltage is required across the junction. Any increase in reverse voltage does not increase the small current. This is called reverse saturation current.

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3(b) 4 - 16 decoder by 2 to 4 decoder.

Quick pointer ⇒

A → MSB , D → LSB

⇒ ENABLE LOGIC

A B C D	Decoder enabled.
0 0 X X	D_1
0 1 X X	D_2
1 0 X X	D_3
1 1 X X	D_4

When A and B are zero, (and CD is irrespective) ⇒ D_1

When A = 0, B = 1 irrespective of CD ; ⇒ D_2.

When A = 1, B = 0 irrespective of CD ⇒ D_3

When A = 1 and B = 0, irrespective of CD ⇒ D_4

∴ D_1, D_2, D_3 and D_4 depends on D_5 decoder

A B C D (input)	Decoder enabled.	Output lines
0 0 0 0	D_1	Y_0
0 0 0 1	D_1	Y_1
0 0 1 0	D_1	Y_2
0 0 1 1	D_1	Y_3
0 1 0 0	D_2	Y_4
0 1 0 1	D_2	Y_5
0 1 1 0	D_2	Y_6
0 1 1 1	D_2	Y_7
1 0 0 0	D_3	Y_8
1 0 0 1	D_3	Y_9

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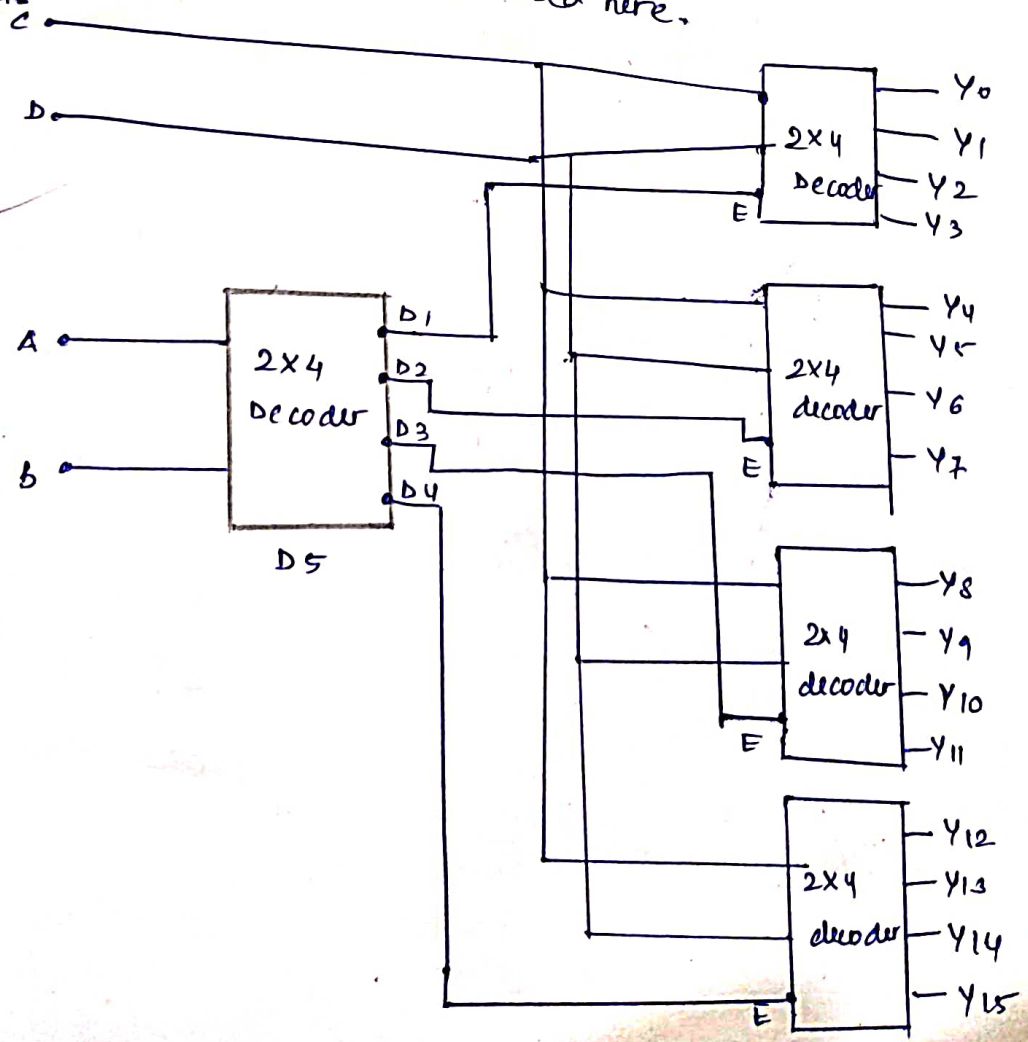
ABCD (input)	Decoder enabled	Output lines
1010	D3	Y_{10}
1011	D3	Y_{11}
1100	D4	Y_{12}
1101	D4	Y_{13}
1110	D4	Y_{14}
1111	D4	Y_{15}

Explanation → When ABCD = 0000, D1 as decoder is chosen and Y_0 as output line. & Similarly, When ABCD = 0001, D1 is decoder and Y_1 is the output line. While using the enable logic, we are choosing the decoder here. $Y_0 - Y_3$ have D1, $Y_4 - Y_7$ have D_2, $Y_8 - Y_{11}$ have D_3 and $Y_{12} - Y_{15}$ have D4.

Hence, we have successfully implemented a 4-16 decoder using 2-4 decoders. There are 5 decoders to be used here.



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4)

$L = 1.4\ H$

$R = 1\ \Omega$

$V = 12\ V$

$t = 400\ ms \rightarrow 0.4\ s$

For $i = I_0(1 - e^{-t/\tau})$; $\tau = \frac{L}{R} = \frac{1.4}{1} = 1.4$

$I_0 = \frac{V}{R} = \frac{12}{1} = 12\ A$

$\therefore i = 12\left(1 - e^{-\frac{0.4}{1.4}}\right)$

$= 12(1 - e^{-0.285})$

$= 3\ A$

For decaying current ; $i = I_0 e^{-t/\tau}$

Now, $6 = 12\ e^{-\frac{t}{1.4}}$

$= \frac{1}{2} = e^{-\frac{t}{1.4}}$

$-\frac{t}{1.4} = \log\left(\frac{1}{2}\right)$; $-t = -0.756$

$= t = 0.756\ s$

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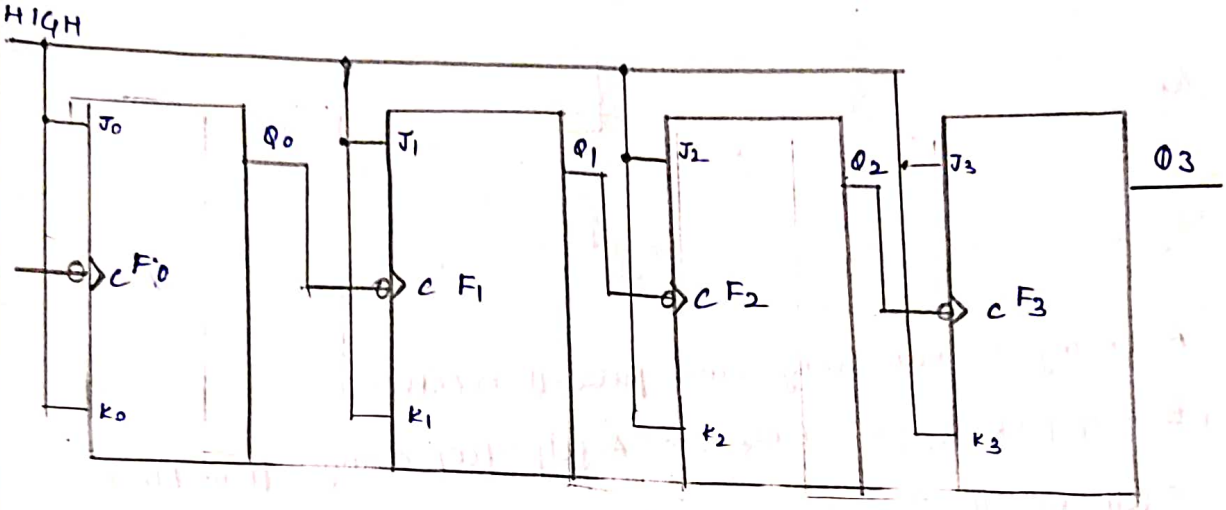
5

4-BIT RIPPLE COUNTER

This counter uses a series connection of J-K flip flops.
Each output of flip flop is connected to the clock pulse input of next higher order flip flop.
The flip flop holding the LSB receive incoming count pulses.
J K inputs are 1.



CP input has a small circle to indicate that the flip flop complements during a negative-going transition (output connected 1 → 0).
The lowest order bit Q_0 must be complemented with each count pulse.
$Q_0 \Rightarrow 1 \to 0 \longrightarrow Q_1$
$Q_1 \Longrightarrow 1 \to 0 \to Q_2$ and so on

State sequence →

MSB Q_3	Q_2	Q_1	LSB Q_0	Dec. val
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14

Q_3	Q_2	Q_1	Q_2	Dec val
1	1	1	1	15
0	0	0	0	full reset

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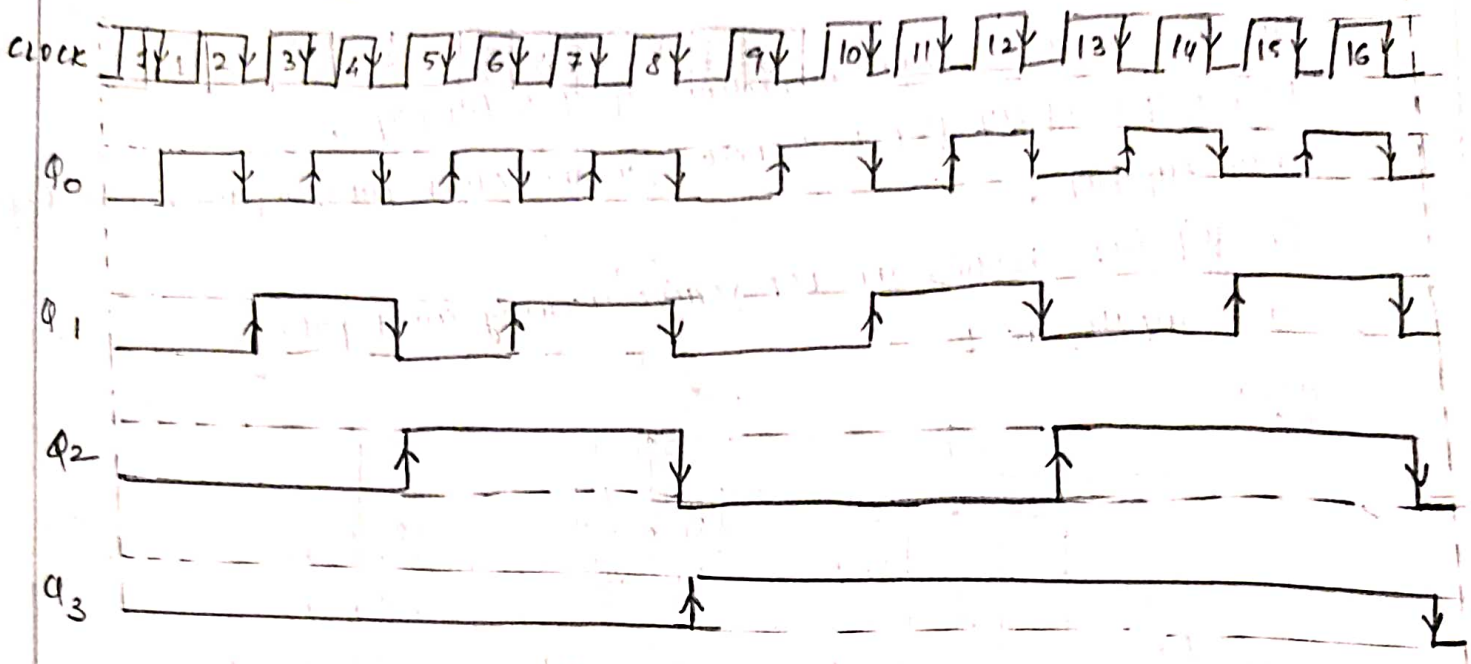
Timming diagram



A FF toggles with every clock pulse. it receives.

B flip flop toggles whenever A flip flop changes from 1 to 0.

C flip flop toggles whenever B flip flop changes from 1 to 0.

D flip flop toggles when C changes from 1 to 0.

Q_0 changes as soon as the negative edge of clock is encountered.

Q_1 is changing when negative edge of Q_0 is encountered and so on.

THANKYOU SIR!