	Reg. No.:	
	Name :	

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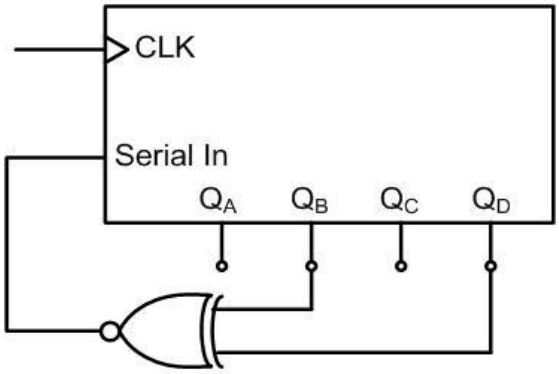
TERM END EXAMINATIONS (TEE) – May 2021

Programme	:	**B.Tech. – All Branch**	**Semester**	:	**Winter 2020-21**
Course Name	:	**Digital Logic Design**	**Course Code**	:	**ECE2002**
Faculty Name	:	**Dr. Jitendra Kumar Tandekar**	**Slot / Class No**	:	**B11+B12+B13/ 0371**
Time	:	**1½ hours**	**Max. Marks**	:	**50**

Answer ALL the Questions

Q. No.		Question Description	Marks
		PART - A (30 Marks)	
1	(a)	Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign. (i) 10011- 10010 (ii) 100010 - 100110 (iii) 1001 - 110101 (iv) 101000 - 10101	10
		OR	
	(b)	Simplify the following Boolean functions, using four-variable maps: (i) $F(w, x, y, z) = \Sigma(1, 4, 5, 6, 12, 14, 15)$ (ii) $F(A, B, C, D) = \Sigma(2, 3, 6, 7, 12, 13, 14)$ (iii) $F(w, x, y, z) = \Sigma(1, 3, 4, 5, 6, 7, 9, 11, 13, 15)$ (iv) $F(A, B, C, D) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$	10
2	(a)	For the following state table: (i) Draw the corresponding state diagram. (ii) Tabulate the reduced state table. (iii) Draw the state diagram corresponding to the reduced state table.	10

Present State	Next state		Output	
	x=0	*x=1*	*x=0*	*x=1*
a	*f*	*b*	*0*	*0*
b	*d*	*c*	*0*	*0*
c	*f*	*e*	*0*	*0*
d	*g*	*a*	*1*	*0*
e	*d*	*c*	*0*	*0*
f	*f*	*b*	*1*	*1*
g	*g*	*h*	*0*	*1*
h	*g*	*a*	*1*	*0*

		OR	
	(b)	Explain the working of clocked JK flip-flop with the help of truth table.	10
3	(a)	Design the 3-bit ripple up-counter and explain the operation in details with positive edge triggering.	10
		OR	
	(b)	Explain port Declaration with an example using Verilog code.	10
PART - B (20 Marks)			
4		Design a 4-bit adder circuit and explain the operation in details with appropriate example.	10
5		A 4-bit SIPO register is used with feedback as shown in the figure 1. the shifting sequence is $Q_A \rightarrow Q_B \rightarrow Q_C \rightarrow Q_D$. If the initial output is "0000", then in which clock cycle will the same output be repeated?  Figure 1.	10

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