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SLOT : B11 + B12 + B13
SEMESTER: II
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MIDSEM EXAMINATION

1 Reduce the following Boolean expressions to indicated number of literals:

(i) $A'C' + ABC + AC'$ (3 literals)

$A'C' + AC' + ABC$

$= C'(A' + A) + ABC$

$= C' \cdot 1 + ABC$

$= C' + ABC$

$= (C' + AB)(C' + C)$

$= AB + C'$

=

(ii) $(x'y' + z)' + z + xy + wz$ (3 literals)

$(x'y' + z)' + z + wz + xy$

$(x'y' + z') + z(1 + w) + xy$

$(x'y' + z') + z + xy$

$(x + y)z' + z + xy$

$(z + (x + y)) \cdot (z + z') + xy$

$(z + (x + y)) \cdot 1 + xy$

$x + y + z + xy$ (absorption)

$x + y + z$

(iii) $A'B(D'+C'D)+B(A+A'CD)$ (1 literal)

$= A'BD' + A'BC'D + AB + A'BCD$

$= A'BD(C+C') + A'BD' + AB$

$= A'BD + A'BD' + AB$

$= A'B(D+D') + AB$

$= A'B + AB$

$= B(A'+A)$

$= B$

$=$

(iv) $(A'+C)(A'+C')(A+B+C'D)$ (4 literals)

$(A'+C)(A'+C')(A+B+C'D)$

$(A'+CC')(A+B+C'D)$

$A'(A+B+C'D)$

$AA' + A'B + A'C'D$

$A'B + A'C'D$

$A'(B+C'D)$

$=$

(v) $ABC'D + A'BD + ABCD$ (2 literals)

$ABD(C'+C) + A'BD$

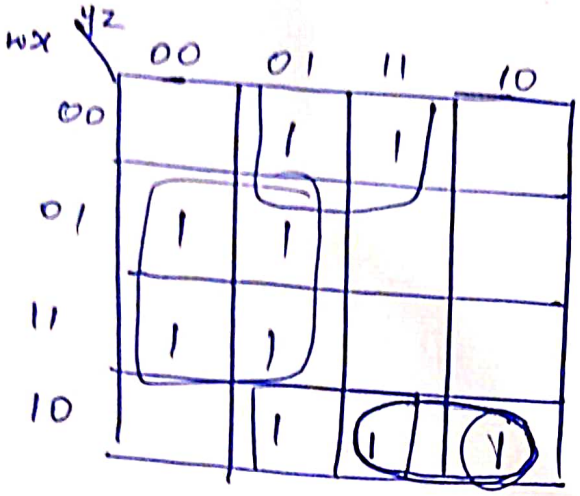
$ABD + A'BD$

$BD(A'+A)$

BD

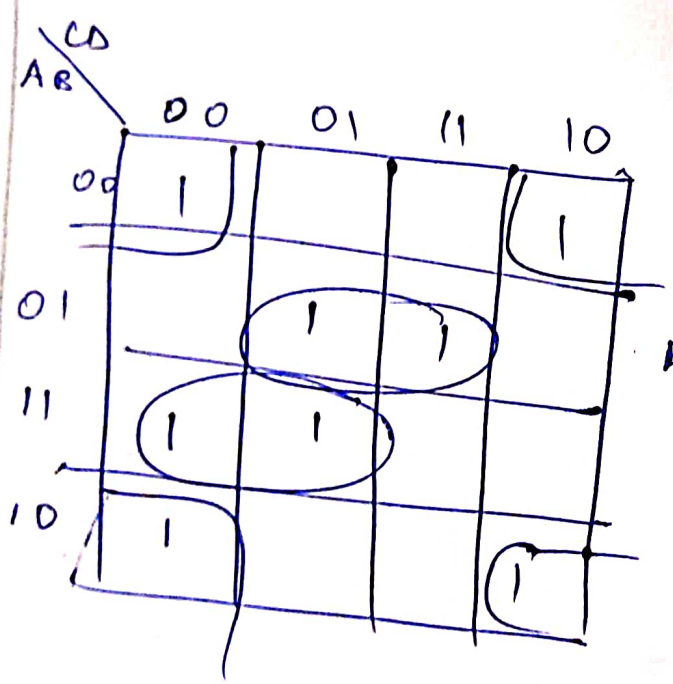
$=$

2(iv) $x'z + w'xy' + w(x'y + y'x)$



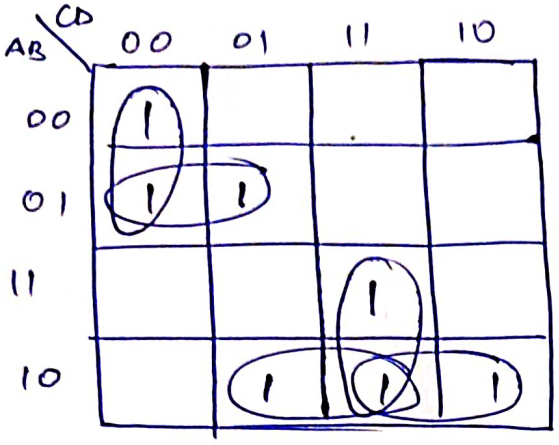
$\Rightarrow F = xy' + wx'y + x'z$

2(v)



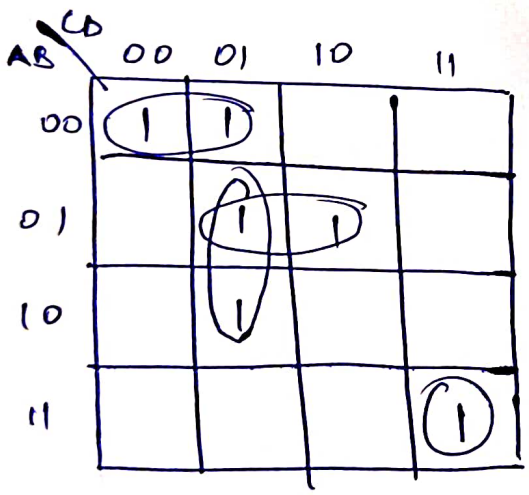
$F = ABC' + A'BD + B'D'$

(iii) $A'B'C'D' + AB'D + A'BC' + ABCD + AB'C$



$F = (A'C'D') + (AB'C) + (AB'D) + (ACD) + (A'BC')$

(iv) $A'B'C'D' + BC'D + A'C'D + A'BCD + ACD'$



$F = A'B'C' + A'BD + BC'D$

$=$

3

The 3:8 line decoder is also called binary to octal decoder. There are a total of eight outputs, i.e, $Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7$ and three inputs A_0, A_1 and A_2. This circuit has an enable E.

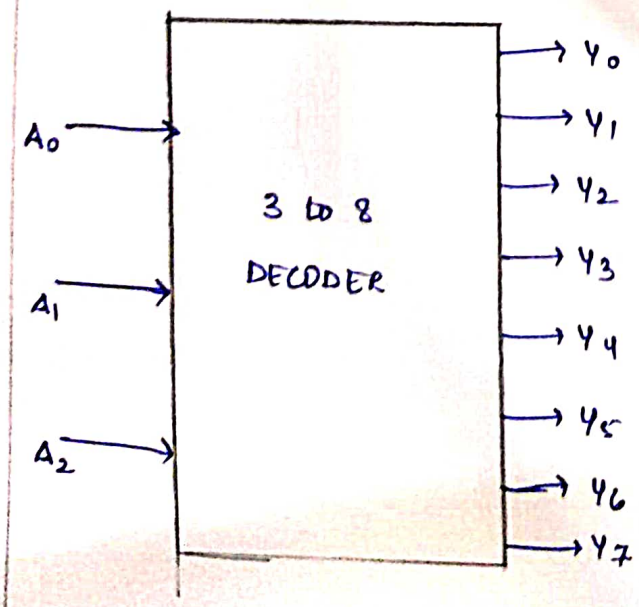
The main function of a decoder is to change a code into a set of signals because it is opposite to an encoder. It receives several inputs and gives decoded output.

When enable is set to 1, the truth table is as follows ⇒

ENABLE	A_0	A_1	A_2	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	X	X	X	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

When the E is low, all the output pins are low.

BLOCK DIAGRAM



LOGIC EXPRESSIONS:

$Y_0 = A_0' . A_1' A_2'$

$Y_1 = A_0 . A_1' A_2'$

$Y_2 = A_0' . A_1 . A_2'$

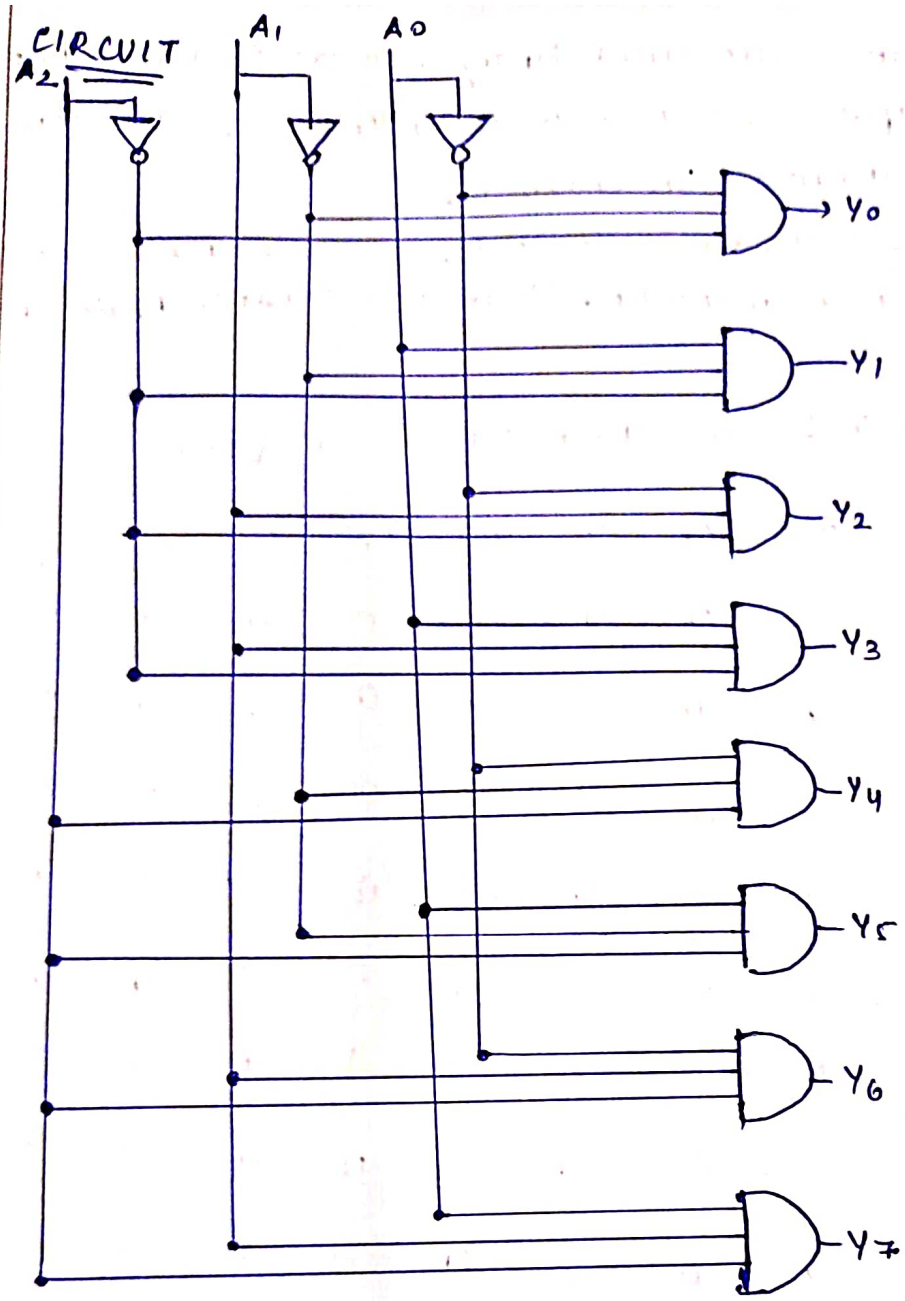
$Y_3 = A_0 . A_1 . A_2'$

$Y_4 = A_0' . A_1' . A_2$

$Y_5 = A_0 . A_1' . A_2$

$Y_6 = A_0' . A_1 . A_2$

$Y_7 = A_0 . A_1 . A_2$

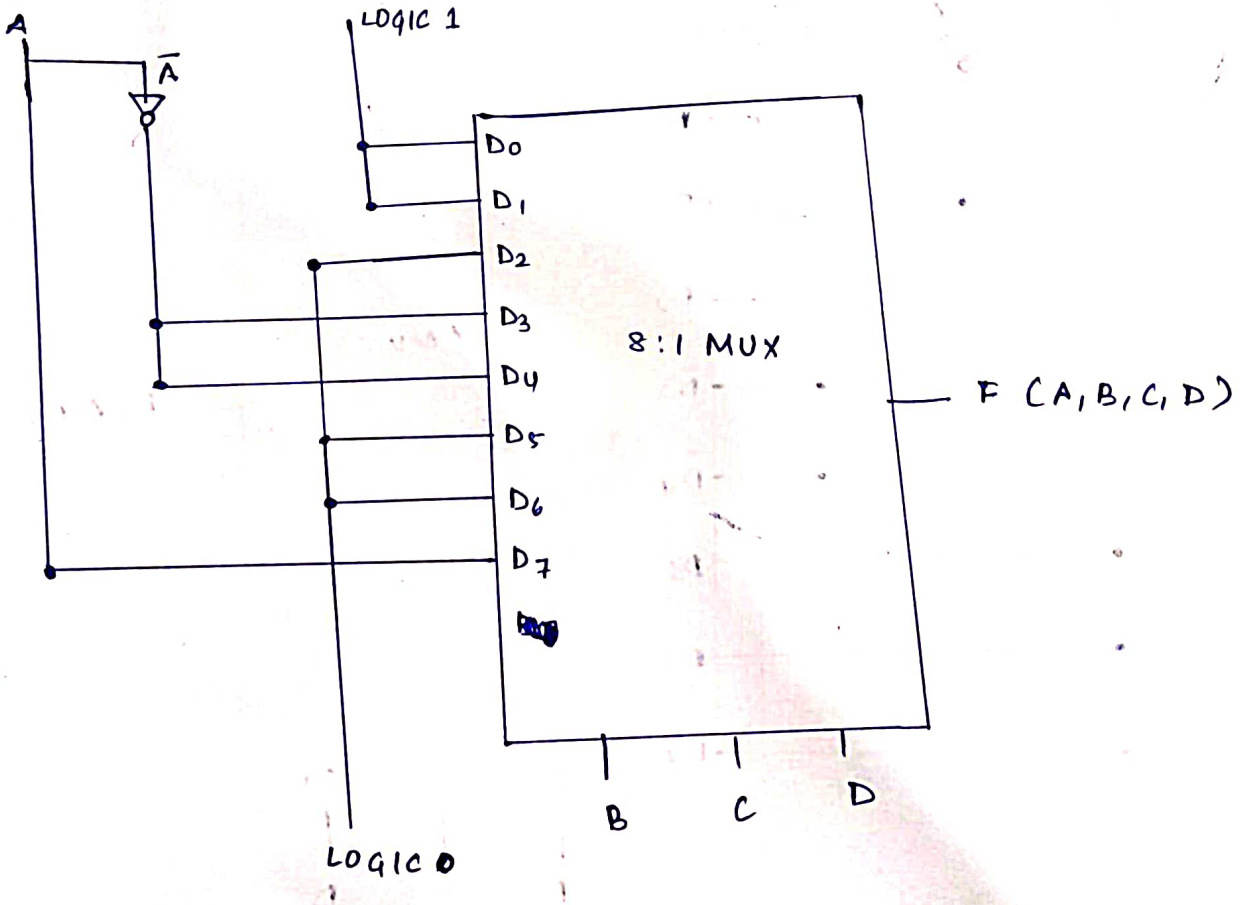


Here, there are three NOT gates and 8 three input AND gates

4 (i) Implement the following Boolean function using 8:1 MUX.

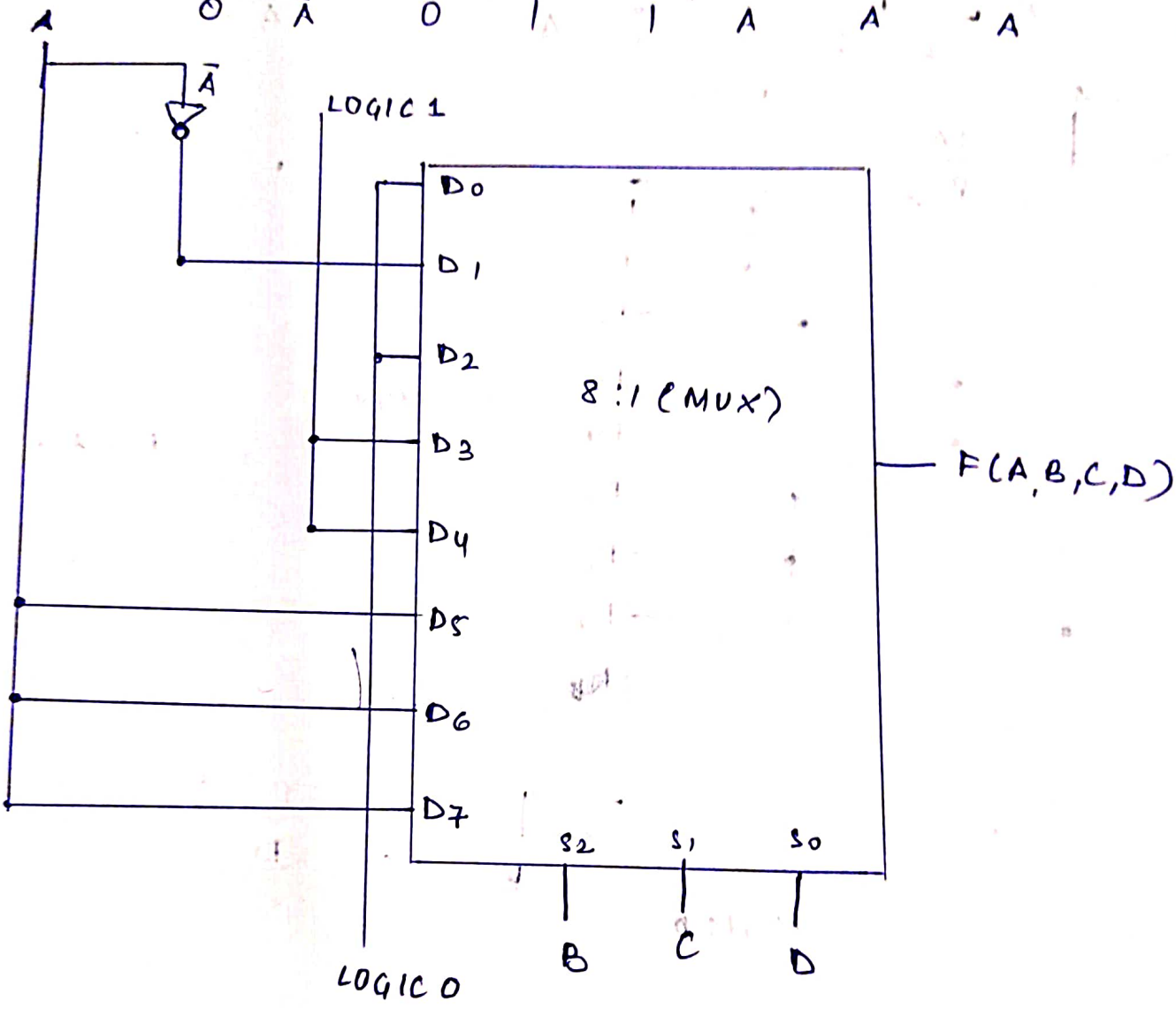
$F(A, B, C, D) = \Sigma(0, 1, 3, 4, 8, 9, 15)$

	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	(0)	(1)	2	(3)	(4)	5	6	7
A	(8)	(9)	10	11	12	13	14	(15)
	1	1	0	$\bar{A}$	$\bar{A}$	0	0	A



(ii) $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$

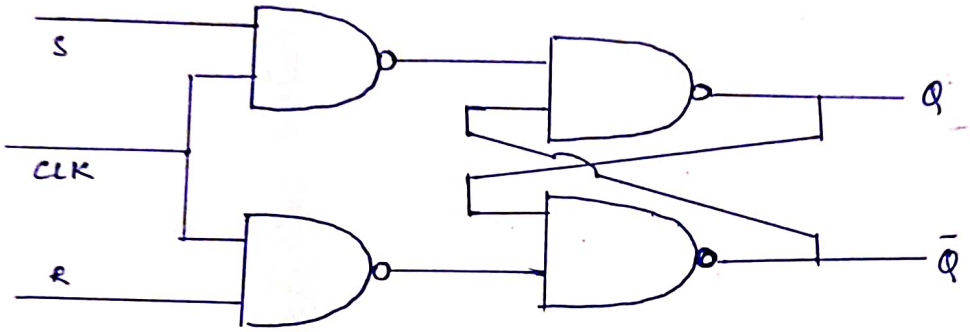
	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$\bar{A}$	0	(1)	2	(3)	(4)	5	6	7
A	8	9	10	(11)	(12)	(13)	(14)	(15)
	0	$\bar{A}$	0	1	1	A	A'	A



5

WORKING OF CLOCKED RS FLIP FLOP WITH TRUTH TABLE

* Clock is added to an RS flip flop to control the time at which the flip flop changes the state of its outputs.
* In the clocked R-S flip flop, some inputs are blocked till the receive a pulse from a source called clock. The flip flop works only when the pulse is applied according to the inputs.
* The circuit is given by two AND gates with the regular R-S flip flop.
* There is one more column in the table called as clock input (C).



CLOCKED RS FLIP FLOP

Truth table

Initial	Inputs		Output	Change shown
Q	S	R	Q(t+1)	No change
0	0	0	0	No change
0	0	1	0	Clear Q
0	1	0	1	Set Q
0	1	1	x	indeterminate
1	0	0	1	No change
1	0	1	0	Clear Q
1	1	0	1	Set Q
1	1	1	x	indeterminate