Que 1. Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign.
(i) 10111- 10110
(ii) 101010 - 101110
(iii) 1101 - 110001
(iv) 101010 – 10111

Que 2. Perform subtraction on the given unsigned numbers using the 10's complement of the subtrahend. Where the result should be negative, find its 10's complement and affix a minus sign. Verify your answers.
(i) 4,637 - 2,759
(ii) 125 - 1,700
(iii) 2,053 - 4,631
(iv) 1,431 – 735

Que 3. Simplify the following Boolean functions, using four-variable K-maps:

(i) $F(w, x, y, z) = \Sigma(1, 3, 4, 6, 11, 14, 15)$
(ii) $F(A, B, C, D) = \Sigma(2, 3, 6, 7, 11, 13, 14)$
(iii) $F(w, x, y, z) = \Sigma(0,1, 3, 4, 5, 6, 8, 9, 11, 12, 15)$
(iv) $F(A, B, C, D) = \Sigma(1, 2, 4, 5, 6, 7, 8, 9, 13, 15)$

Que 4. Simplify the following Boolean expressions, using four-variable K- maps:
(i) *A'B' C' D' + AC'D' + B'CD' + A'BCD + BC'D*
(ii) *x'z + w' xy' + w(x'y + xy')*
(iii) *A'B'C'D + AB'D + A'BC' + ABCD + AB'C*
(iv) *A'B'C'D' + BC'D + A'C'D + A'BCD + ACD'*

Que 5. Simplify the following Boolean functions, using three-variable K-maps:
(i) $F(x, y, z) = \Sigma(0, 1, 5, 7)$
(ii) $F(x, y, z) = \Sigma(1, 2, 3, 6, 7)$
(iii) $F(x, y, z) = \Sigma(2, 3, 4, 5)$
(iv) $F(x, y, z) = \Sigma(1, 2, 3, 5, 6, 7)$
(v) $F(x, y, z) = \Sigma(0, 2, 4, 6)$
(vi) $F(x, y, z) = \Sigma(3, 4, 5, 6, 7)$

Que 6. Simplify the following Boolean expressions, using three-variable K-maps:
(a) xy + x'y'z' + x'yz
(b) x'y' + yz + x'yz'
(c) F(x, y, z) = x'y + yz' + y'z'
(d) F(x, y, z) = x'yz + xy'z' + xy'z

Que 7. Simplify the following Boolean functions, using *Karnaugh* maps:
(a) $F(x, y, z) = (2, 3, 6, 7)$
(b) $F(A, B, C, D) = (4, 6, 7, 15)$
(c) $F(A, B, C, D) = (3, 7, 11, 13, 14, 15)$
(d) $F(w, x, y, z) = (2, 3, 12, 13, 14, 15)$

Que 8. For the following state table:

Present State	Next state		Output	
	x=0	*x=1*	*x=0*	*x=1*
a	*f*	*b*	*0*	*0*
b	*d*	*c*	*0*	*0*
c	*f*	*e*	*0*	*0*
d	*g*	*a*	*1*	*0*
e	*d*	*c*	*0*	*0*
f	*f*	*b*	*1*	*1*
g	*g*	*h*	*0*	*1*
h	*g*	*a*	*1*	*0*

(i) Draw the corresponding state diagram.
(ii) Tabulate the reduced state table.
(iii) Draw the state diagram corresponding to the reduced state table.

Que 9. Using partitioning minimization procedure reduce the following state table:

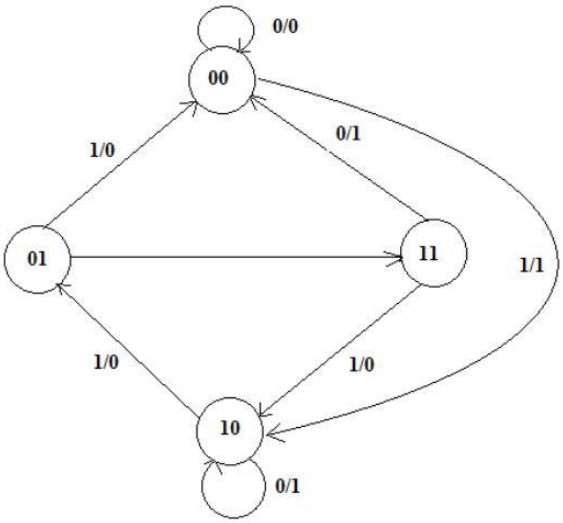
Present State	Next state		Output
	w=0	*w=1*	*z*
A	*B*	*C*	*1*
B	*D*	*F*	*1*
C	*F*	*E*	*0*
D	*B*	*G*	*1*
E	*F*	*C*	*0*
F	*E*	*D*	*0*
G	*F*	*G*	*0*

Also draw the corresponding state diagram.

Que 10. Using partitioning minimization procedure reduce the following state table:

Present State	Next state		Output
	x=0	*y=1*	*w*
a	*b*	*c*	*1*
b	*d*	*f*	*1*
c	*f*	*e*	*0*
d	*b*	*g*	*1*
e	*f*	*c*	*0*
f	*e*	*d*	*0*
g	*f*	*g*	*0*

Que 11. Construct a sequential logic circuit with single input and single output by obtaining the state and excitation table for the given state diagram using JK Flip Flop.



Que 12. With the aid of block diagram clearly distinguish between a decoder and encoder

Que 13. Design a 4-bit adder circuit and explain the operation in details with appropriate example.

Que 14. Explain the working of the following:

(i) Clocked S-R flip-flop.
(ii) Clocked D-flip-flop.
(iii) Clocked JK-flip-flop.
(iv) Clocked T-flip-flop.

Que 15. Draw the logic diagram of a four-bit binary ripple countdown counter using

a) flip-flops that trigger on the positive-edge of the clock and
b) flip-flops that trigger on the negative-edge of the clock

Que 16. How many flip-flop will be complemented in a 10-bit binary ripple counter to reach the next count after the following counts?

a) 1001100111
b) 1111000111
c) 0000001111

Que 17. Explain 4-bit ring counter with circuit diagram and waveforms.

Que 18. Using D flip-flops,

a) Design a counter with the following repeated binary sequence: 0, 2, 4, 6, 8.
b) Draw the logic diagram of the counter.

Que 19. Using JK flip-flops,

a) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6.
b) Draw the logic diagram of the counter.

Que 20. Design and implement a synchronous 3-bit up/down counter using JK flip-flops.

Que 21. Design the 3-bit parallel up-counter and explain the operation in details with positive edge clock pulse.

Que 22. Design the 3-bit ripple up-counter and explain the operation in details with positive edge triggering.

Que 23. A 4-bit SIPO register is used with feedback as shown in the figure 1. the shifting sequence is $Q_A \rightarrow Q_B \rightarrow Q_C \rightarrow Q_D$. If the output is 0010 initially the output repeats after which clock cycles?

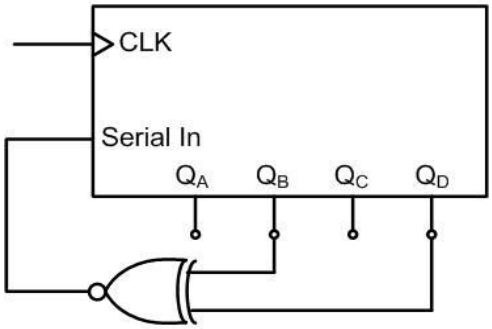


Figure 1.

Que 24. The initial counter of the 4-bit SIPO right shift register shown in figure 2. is 0110 after three clock pulses are applied the results of the shift register will be? Explain with the truth table.

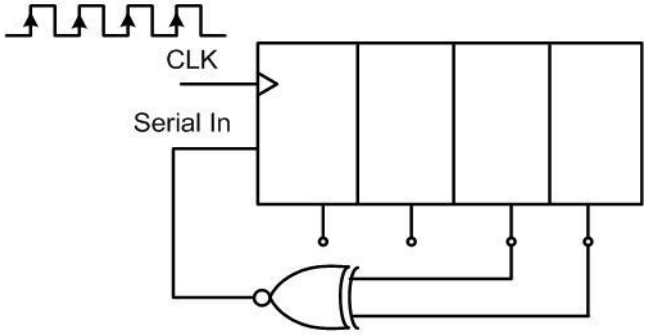


Figure 2.

Que 25. How do we know that we have not made a mistake when we manually draw a schematic and connect components to implement a function?

Que 26. Explain port Declaration with an example using Verilog code.

Que 27. Write short notes on built in operators used in VHDL programming.

Que 28. Write the verilog description of Half adder. Also write stimulus code.

Que 29. How to write comments in verilog HDL, explain with examples.

Que 30. Explain the port connection rules of Verilog HDL with examples.