

MINILAB 1 REPORT

Name: Ananya Virmani

Email: virmani2@wisc.edu

Overview

This Minilab required the implementation of a top-level module for matrix-vector multiplication. The design reads input data from the provided memory module and performs row-wise multiply-accumulate operations to generate the final output vector.

Implementation

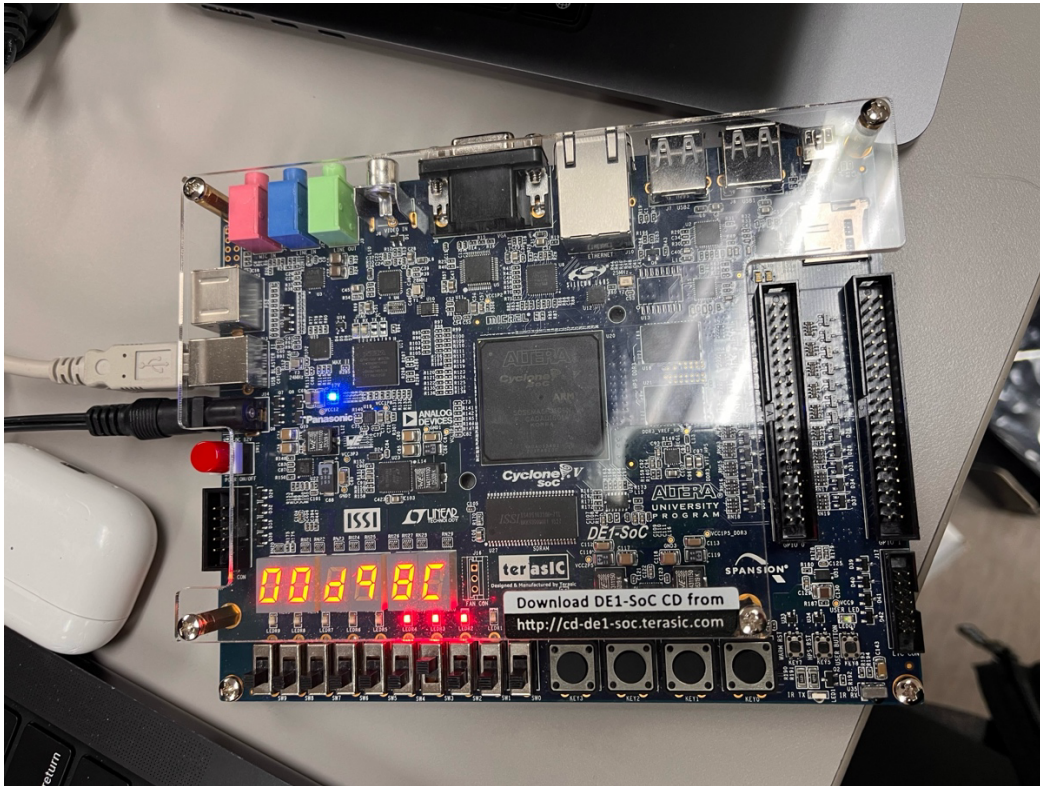
The memory structure was partitioned such that:

- Rows 0–7 functioned as eight separate FIFOs containing the rows of matrix A.
- The last memory row functioned as a FIFO storing vector B.
- The computation logic consisted of:
 - Eight parallel MAC units, each for one row of matrix A.
 - Sequential controlled logic such that MAC units activate in order.
- Existing Quartus IPs were used for both FIFO and MAC implementations to ensure reliable functionality and synthesis compatibility.

Screenshots and Images

- Waveform and Simulation Log

- Working Board at SW3



How did we fix timing?

We initially had a frequency of 127.47 with the timing constraints of 200 MHz not satisfied. To fix this:

To improve timing performance, the following structural changes were implemented:

- Flopped the outputs of the FIFO such that it breaks the long combinational path which as a result introduces one clock cycle delay that had to be accounted for by adjusting the state machine to maintain data alignment.
- The LPM_MULT module was modified to operate with two pipeline stages. Corresponding adjustments were made to the state machine to synchronize control and data paths to account for this delay.

These changes helped us achieve a final frequency of 267.09 MHz. The screenshots for these before and after the fix are also in the images folder.

