Integration Manual

for S32K1 GPT Driver

Document Number: IM2GPTASR4.4 Rev0000R1.0.1 Rev. 1.0

Chapter 1

Revision History

Revision	Date	Author	Description
1.0	24.02.2022	NXP RTD Team	Prepared for release RTD S32K1 Version 1.0.1

Chapter 2

Introduction

This integration manual describes the integration requirements for GPT Driver for S32K1xx microcontrollers.

2.1 Supported Derivatives

The software described in this document is intended to be used with the following microcontroller devices of NXP Semiconductors:

- s32k116_qfn32
- s32k116_lqfp48
- s32k118_lqfp48
- s32k118_lqfp64
- s32k142_lqfp48
- s32k142_lqfp64
- s32k142_lqfp100
- s32k142w_lqfp48
- s32k142w_lqfp64
- s32k144_lqfp48
- s32k144_lqfp64
- s32k144_lqfp100

- s32k144_mapbga100
- s32k144w_lqfp48
- s32k144w_lqfp64
- s32k146_lqfp64
- s32k146_lqfp100
- s32k146_mapbga100
- s32k146_lqfp144
- s32k148_lqfp100
- s32k148_mapbga100
- s32k148_lqfp144
- s32k148_lqfp176

All of the above microcontroller devices are collectively named as S32K1.

2.2 Overview

AUTOSAR (AUTomotive Open System ARchitecture) is an industry partnership working to establish standards for software interfaces and software modules for automobile electronic control systems.

AUTOSAR:

- paves the way for innovative electronic systems that further improve performance, safety and environmental friendliness.
- is a strong global partnership that creates one common standard: "Cooperate on standards, compete on implementation".
- is a key enabling technology to manage the growing electrics/electronics complexity. It aims to be prepared for the upcoming technologies and to improve cost-efficiency without making any compromise with respect to quality.
- facilitates the exchange and update of software and hardware over the service life of the vehicle.

2.3 About This Manual

This Technical Reference employs the following typographical conventions:

- **Boldface** style: Used for important terms, notes and warnings.
- *Italic* style: Used for code snippets in the text. Note that C language modifiers such "const" or "volatile" are sometimes omitted to improve readability of the presented code.

Notes and warnings are shown as below:

Note

This is a note.

Warning

This is a warning

2.4 Acronyms and Definitions

Term	Definition
API	Application Programming Interface
ASM	Assembler
BSMI	Basic Software Make file Interface
GPT	General Purpose Timer
C/CPP	C and C++ Source Code
CS	Chip Select
CTU	Cross Trigger Unit
DEM	Diagnostic Event Manager
DET	Development Error Tracer
DMA	Direct Memory Access
ECU	Electronic Control Unit
FIFO	First In First Out
LSB	Least Significant Bit
MCU	Micro Controller Unit
OS	Operating System
MIDE	Multi Integrated Development Environment
MSB	Most Significant Bit
N/A	Not Applicable
RAM	Random Access Memory
SIU	Systems Integration Unit
SWS	Software Specification
VLE	Variable Length Encoding
XML	Extensible Markup Language

2.5 Reference List

#	Title	Version
1	Specification of GPT Driver	AUTOSAR Release 4.↩ 4.0
2	S32K1xx Series Reference Manual	Rev. 14, 09/2021
3	S32K1xx Data Sheet	Rev. 14, 08/2021
4	Errata S32K116_0N96V	Rev. 22/OCT/2021
5	Errata S32K118_0N97V	Rev. 22/OCT/2021
6	Errata S32K142_0N33V	Rev. 22/OCT/2021
7	Errata S32K144_0N57U	Rev. 22/OCT/2021
8	Errata S32K144W_0P64A	Rev. 22/OCT/2021
9	Errata S32K146_0N73V	Rev. 22/OCT/2021
10	Errata S32K148_0N20V	Rev. 22/OCT/2021

Chapter 3

Building the driver

- Build Options
- Files required for compilation
- Setting up the plugins

This section describes the source files and various compilers, linker options used for building the driver.
It also explains the EB Tresos Studio plugin setup procedure.

3.1 Build Options

- GCC Compiler/Assembler/Linker Options
- GHS Compiler/Assembler/Linker Options
- IAR Compiler/Assembler/Linker Options

The RTD driver files are compiled using:

- NXP GCC 9.2.0 20190812 (Build 1649 Revision gaf57174)
- IAR ANSI C/C++ Compiler V8.40.3.228/W32 for ARM Functional Safety
- Green Hills Multi 7.1.6d / Compiler 2020.1.4

The compiler, assembler, and linker flags used for building the driver are explained below.
The TS_T40D2M10I1R0 part of the plugin name is composed as follows:

- T = Target_Id (e.g. T40 identifies Cortex-M architecture)
- D = Derivative_Id (e.g. D2 identifies S32K1 platform)
- M = SW_Version_Major and SW_Version_Minor
- I = SW_Version_Patch
- R = Reserved

3.1.1 GCC Compiler/Assembler/Linker Options

3.1.1.1 GCC Compiler Options

Compiler Option	Description
-mcpu=cortex-m4	Targeted ARM processor for which GCC should tune the performance of the code (for S32K14x devices)
-mcpu=cortex-m0plus	Targeted ARM processor for which GCC should tune the performance of the code (for S32K11x devices)
-mthumb	Generates code that executes in Thumb state
-mlittle-endian	Generate code for a processor running in little-endian mode
-mfpu=fpv4-sp-d16	Specifies the floating-point hardware available on the target (for S32K14x devices)
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions (for S32K14x devices)
-mfpu=auto	Specifies the floating-point hardware available on the target (for S32K11x devices)
-mfloat-abi=soft	Specifies the floating-point ABI to use. Specifying "soft" causes GCC to generate output containing library calls for floating-point operations (for S32K11x devices)
-std=c99	Specifies the ISO C99 base standard
-Os	Optimize for size. Enables all -O2 optimizations except those that often increase code size
-ggdb3	Produce debugging information for use by GDB using the most expressive format available, including GDB extensions if at all possible. Level 3 includes extra information, such as all the macro definitions present in the program
-Wall	Enables all the warnings about constructions that some users consider questionable, and that are easy to avoid (or modify to prevent the warning), even in conjunction with macros
-Wextra	This enables some extra warning flags that are not enabled by -Wall
-pedantic	Issue all the warnings demanded by strict ISO C. Reject all programs that use forbidden extensions. Follows the version of the ISO C standard specified by the aforementioend -std option
-Wstrict-prototypes	Warn if a function is declared or defined without specifying the argument types
-Wundef	Warn if an undefined identifier is evaluated in an #if directive. Such identifiers are replaced with zero
-Wunused	Warn whenever a function, variable, label, value, macro is unused
-Werror=implicit-function-declaration	Make the specified warning into an error. This option throws an error when a function is used before being declared
-Wsign-compare	Warn when a comparison between signed and unsigned values could produce an incorrect result when the signed value is converted to unsigned.
-Wdouble-promotion	Give a warning when a value of type float is implicitly promoted to double
-fno-short-enums	Specifies that the size of an enumeration type is at least 32 bits regardless of the size of the enumerator values.

Compiler Option	Description
-funsigned-char	Let the type char be unsigned by default, when the declaration does not use either signed or unsigned
-funsigned-bitfields	Let a bit-field be unsigned by default, when the declaration does not use either signed or unsigned
-fomit-frame-pointer	Omit the frame pointer in functions that dont need one. This avoids the instructions to save, set up and restore the frame pointer; on many targets it also makes an extra register available.
-fno-common	Makes the compiler place uninitialized global variables in the BSS section of the object file. This inhibits the merging of tentative definitions by the linker so you get a multiple-definition error if the same variable is accidentally defined in more than one compilation unit
-fstack-usage	Makes the compiler output stack usage information for the program, on a per-function basis
-fdump-ipa-all	Enables all inter-procedural analysis dumps
-c	Stop after assembly and produce an object file for each source file
-DS32K1XX	Predefine S32K1XX as a macro, with definition 1
-DS32K148	Predefine S32K148 as a macro, with definition 1
-DGCC	Predefine GCC as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver (for S32K14x devices)
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver (for S32K14x devices)
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPO↩ RT as a macro, with definition 1. Allows drivers to be configured in user mode.

3.1.1.2 GCC Assembler Options

Assembler Option	Description
-Xassembler-with-cpp	Specifies the language for the following input files (rather than letting the compiler choose a default based on the file name suffix)
-mcpu=cortex-m4	Targeted ARM processor for which GCC should tune the performance of the code (for S32K14x devices)
-mcpu=cortex-m0plus	Targeted ARM processor for which GCC should tune the performance of the code (for S32K11x devices)
-mthumb	Generates code that executes in Thumb state
-c	Stop after assembly and produce an object file for each source file

3.1.1.3 GCC Linker Options

Linker Option	Description
-Wl,-Map,filename	Produces a map file
-T linkerfile	Use linkerfile as the linker script. This script replaces the default linker script (rather than adding to it)
–entry=Reset_Handler	Specifies that the program entry point is Reset_Handler
-nostartfiles	Do not use the standard system startup files when linking
-mcpu=cortex-m4	Targeted ARM processor for which GCC should tune the performance of the code (for S32K14x devices)
-mcpu=cortex-m0plus	Targeted ARM processor for which GCC should tune the performance of the code (for S32K11x devices)
-mthumb	Generates code that executes in Thumb state
-mfpu=fpv4-sp-d16	Specifies the floating-point hardware available on the target (for S32K14x devices)
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions (for S32K14x devices)
-mfpu=auto	Specifies the floating-point hardware available on the target (for S32K11x devices)
-mfloat-abi=soft	Specifies the floating-point ABI to use. Specifying "soft" causes GCC to generate output containing library calls for floating-point operations (for S32K11x devices)
-mlittle-endian	Generate code for a processor running in little-endian mode
-ggdb3	Produce debugging information for use by GDB using the most expressive format available, including GDB extensions if at all possible. Level 3 includes extra information, such as all the macro definitions present in the program
-lc	Link with the C library
-lm	Link with the Math library
-lgcc	Link with the GCC library
-n	Turn off page alignment of sections, and disable linking against shared libraries

3.1.2 GHS Compiler/Assembler/Linker Options

3.1.2.1 GHS Compiler Options

Compiler Option	Description
-cpu=cortexm4	Selects target processor: Arm Cortex M4 (for S32K14x devices)
-cpu=cortexm0plus	Selects target processor: Arm Cortex M0+ (for S32K11x devices)
-thumb	Selects generating code that executes in Thumb state
-fpu=vfpv4_d16	Specifies hardware floating-point using the v4 version of the VFP instruction set, with 16 double-precision floating-point registers (for S32K14x devices)
-fsingle	Use hardware single-precision, software double-precision FP instructions (for S32K14x devices)

Compiler Option	Description
-fsoft	Specifies software floating-point (SFP) mode. This setting causes your target to use integer registers to hold floating-point data and use library subroutine calls to emulate floating-point operations (for S32K11x devices)
-C99	Use (strict ISO) C99 standard (without extensions)
–ghstd=last	Use the most recent version of Green Hills Standard mode (which enables warnings and errors that enforce a stricter coding standard than regular C and C++)
-Osize	Optimize for size
–gnu_asm	Enables GNU extended asm syntax support
-dual_debug	Generate DWARF 2.0 debug information
-G	Generate debug information
-keeptempfiles	Prevents the deletion of temporary files after they are used. If an assembly language file is created by the compiler, this option will place it in the current directory instead of the temporary directory
-Wimplicit-int	Produce warnings if functions are assumed to return int
-Wshadow	Produce warnings if variables are shadowed
-Wtrigraphs	Produce warnings if trigraphs are detected
-Wundef	Produce a warning if undefined identifiers are used in #if preprocessor statements
–unsigned_chars	Let the type char be unsigned, like unsigned char
–unsigned_fields	Bitfelds declared with an integer type are unsigned
–no_commons	Allocates uninitialized global variables to a section and initializes them to zero at program startup
–no_exceptions	Disables C++ support for exception handling
–no_slash_comment	C++ style // comments are not accepted andgenerate errors
–prototype_errors	Controls the treatment of functions referenced or called when no prototype has been provided
–incorrect_pragma_warnings	Controls the treatment of valid #pragma directives that use the wrong syntax
-c	Stop after assembly and produce an object file for each source file
-DS32K1XX	Predefine S32K1XX as a macro, with definition 1
-DS32K148	Predefine S32K148 as a macro, with definition 1
-DGHS	Predefine GHS as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver (for S32K14x devices)
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver (for S32K14x devices)

Compiler Option	Description
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPO↩ RT as a macro, with definition 1. Allows drivers to be configured in user mode

3.1.2.2 GHS Assembler Options

Assembler Option	Description
-cpu=cortexm4	Selects target processor: Arm Cortex M4 (for S32K14x devices)
-cpu=cortexm0plus	Selects target processor: Arm Cortex M0+ (for S32K11x devices)
-preprocess_assembly_files	Controls whether assembly files with standard extensions such as .s and .asm are preprocessed
-list	Creates a listing by using the name and directory of the object file with the .lst extension
-c	Stop after assembly and produce an object file for each source file

3.1.2.3 GHS Linker Options

Linker Option	Description
-e Reset_Handler	Make the symbol Reset_Handler be treated as a root symbol and the start label of the application
-T linker_script_file.ld	Use linker_script_file.ld as the linker script. This script replaces the default linker script (rather than adding to it)
-map	Produce a map file
-keepmap	Controls the retention of the map file in the event of a link error
-Mn	Generates a listing of symbols sorted alphabetically/numerically by address
-delete	Instructs the linker to remove functions that are not referenced in the final executable. The linker iterates to find functions that do not have relocations pointing to them and eliminates them
-ignore_debug_references	Ignores relocations from DWARF debug sections when using -delete. DWA↩ RF debug information will contain references to deleted functions that may break some third-party debuggers
-Llibrary_path	Points to library_path (the libraries location) for thumb2 to be used for linking
-larch	Link architecture specific library
-lstartup	Link run-time environment startup routines. The source code for themodules in this library is provided in the src/libstartup directory
-lind_sd	Link language-independent library, containing support routines for features such as software floating point, run-time error checking, C99 complex numbers, and some general purpose routines of the ANSI C library (for S32K14x devices)
-lind_sf	Link language-independent library, containing support routines for features such as software floating point, run-time error checking, C99 complex numbers, and some general purpose routines of the ANSI C library (for S32K11x devices)
-v	Prints verbose information about the activities of the linker, including the libraries it searches to resolve undefined symbols
-keep=C40_Ip_AccessCode	Avoid linker remove function C40_Ip_AccessCode from Fls module because it is not referenced explicitly

Linker Option	Description
-nostartfiles	Controls the start files to be linked into the executable

3.1.3 IAR Compiler/Assembler/Linker Options

3.1.3.1 IAR Compiler Options

Compiler Option	Description
–cpu=Cortex-M4	Targeted ARM processor for which IAR should tune the performance of the code (for S32K14x devices)
–cpu=Cortex-M0+	Targeted ARM processor for which IAR should tune the performance of the code (for S32K11x devices)
–cpu_mode=thumb	Generates code that executes in Thumb state
–endian=little	Generate code for a processor running in little-endian mode
–fpu=FPv4-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant. (for S32K14x devices)
–fpu=none	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). No FPU. (for S32K11x devices)
-e	Enables all IAR C language extensions
-Ohz	Optimize for size. the compiler will emit AEABI attributes indicating the requested optimization goal. This information can be used by the linker to select smaller or faster variants of DLIB library functions
–debug	Makes the compiler include debugging information in the object modules. Including debug information will make the object files larger
–no_clustering	Disables static clustering optimizations. Static and global variables defined within the same module will not be arranged so that variables that are accessed in the same function are close to each other
–no_mem_idioms	Makes the compiler not optimize certain memory access patterns
–no_explicit_zero_opt	Do not treat explicit initializations to zero of static variables as zero initializations
–require_prototypes	Force the compiler to verify that all functions have proper prototypes. Generates an error otherwise
–no_wrap_diagnostics	Does not wrap long lines in diagnostic messages
–diag_suppress=Pa050	Suppresses diagnostic message Pa050
-DS32K1XX	Predefine S32K1XX as a macro, with definition 1
-DS32K148	Predefine S32K148 as a macro, with definition 1
-DIAR	Predefine IAR as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.

Compiler Option	Description
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver (for S32K14x devices)
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver (for S32K14x devices)
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPO↩ RT as a macro, with definition 1. Allows drivers to be configured in user mode.

3.1.3.2 IAR Assembler Options

Assembler Option	Description
–cpu=Cortex-M4	Targeted ARM processor for which IAR should tune the performance of the code (for S32K14x devices)
–cpu=Cortex-M0+	Targeted ARM processor for which IAR should tune the performance of the code (for S32K11x devices)
–cpu_mode thumb	Selects the thumb mode for the assembler directive CODE
-g	Disables the automatic search for system include files
-r	Generates debug information

3.1.3.3 IAR Linker Options

Linker Option	Description
–map filename	Produces a map file
–config linkerfile	Use linkerfile as the linker script. This script replaces the default linker script (rather than adding to it)
–cpu=Cortex-M4	Targeted ARM processor for which IAR should tune the performance of the code (for S32K14x devices)
–cpu=Cortex-M0+	Targeted ARM processor for which IAR should tune the performance of the code (for S32K11x devices)
–fpu=FPv4-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant. (for S32K14x devices)
–fpu=none	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). No FPU. (for S32K11x devices)
–entry __start	Treats __start as a root symbol and start label
–enable_stack_usage	Enables stack usage analysis. If a linker map file is produced, a stack usage chapter is included in the map file
–skip_dynamic_initialization	Dynamic initialization (typically initialization of C++ objects with static storage duration) will not be performed automatically during application startup
–no_wrap_diagnostics	Does not wrap long lines in diagnostic messages

3.2 Files required for compilation

This section describes the include files required to compile, assemble (if assembler code) and link the GPT driver for S32K1xx micro-controllers. To avoid integration of incompatible files, all the include files from other modules shall have the same AR_MAJOR_VERSION and AR_MINOR_VERSION, i.e. only files with the same AUTOSAR major and minor versions can be compiled.

GPT files:

- ..\Gpt_TS_T40D2M10I1R0\include\Gpt.h
- ..\Gpt_TS_T40D2M10I1R0\include\Gpt_EnvCfg.h
- ..\Gpt_TS_T40D2M10I1R0\include\Gpt_Ipw.h
- ..\Gpt_TS_T40D2M10I1R0\include\Gpt_Ipw_Irq.h
- ..\Gpt_TS_T40D2M10I1R0\include\Gpt_Ipw_Types.h
- ..\Gpt_TS_T40D2M10I1R0\include\Gpt_Irq.h
- ..\Gpt_TS_T40D2M10I1R0\include\LPit_Gpt_Ip.h
- ..\Gpt_TS_T40D2M10I1R0\include\LPit_Gpt_Ip_Types.h
- ..\Gpt_TS_T40D2M10I1R0\include\SRtc_Ip.h
- ..\Gpt_TS_T40D2M10I1R0\include\SRtc_Ip_Types.h
- ..\Gpt_TS_T40D2M10I1R0\include\Lptmr_Gpt_Ip.h
- ..\Gpt_TS_T40D2M10I1R0\include\Lptmr_Gpt_Ip_Types.h
- ..\Gpt_TS_T40D2M10I1R0\include\Ftm_Gpt_Ip.h
- ..\Gpt_TS_T40D2M10I1R0\include\Ftm_Gpt_Ip_Types.h

- ..\Gpt_TS_T40D2M10I1R0\src\Gpt.c
- ..\Gpt_TS_T40D2M10I1R0\src\Gpt_Ipw.c
- ..\Gpt_TS_T40D2M10I1R0\src\LPit_Gpt_Ip.c
- ..\Gpt_TS_T40D2M10I1R0\src\Lptmr_Gpt_Ip.c
- ..\Gpt_TS_T40D2M10I1R0\src\SRtc_Ip.c
- ..\Gpt_TS_T40D2M10I1R0\src\Ftm_Gpt_Ip.c

GPT generated files (these files should be generated by the user using a configuration tool):

- **<Filename>_Cfg.c (For PC Variant) - For driver compilation, this file should be generated by the user using a configuration tool**
- **<Filename>_PBcfg.c (For PB Variant) - For driver compilation, this file should be generated by the user using a configuration tool**

- **<Filename>_Cfg.h - For driver compilation, this file should be generated by the user using a configuration tool**
  - Gpt_Cfg.h
  - LPit_Gpt_Ip_Cfg.h
  - LPit_Gpt_Ip_Cfg_Defines.h
  - SRtc_Ip_Cfg.h
  - SRtc_Ip_Cfg_Defines.h
  - Lptmr_Gpt_Ip_Cfg.h
  - Lptmr_Gpt_Ip_Cfg_Defines.h
  - Ftm_Gpt_Ip_Cfg.h
  - Ftm_Gpt_Ip_Cfg_Defines.h
  - Gpt_Ipw_PBcfg.h
  - Gpt_PBcfg.h
  - LPit_Gpt_Ip_PBcfg.h
  - SRtc_Ip_PBcfg.h
  - Lptmr_Gpt_Ip_PBcfg.h
  - Ftm_Gpt_Ip_PBcfg.h
  - Gpt_Cfg.c
  - Gpt_PBcfg.c
  - LPit_Gpt_Ip_PBcfg.c
  - SRtc_Ip_PBcfg.c
  - Lptmr_Gpt_Ip_PBcfg.c
  - Ftm_Gpt_Ip_PBcfg.c

Files from Base common folder:

- ..\Base_TS_T40D2M10I1R0\include\BasicTypes.h
- ..\Base_TS_T40D2M10I1R0\include\Compiler.h
- ..\Base_TS_T40D2M10I1R0\include\CompilerDefinition.h
- ..\Base_TS_T40D2M10I1R0\include\Compiler_Cfg.h
- ..\Base_TS_T40D2M10I1R0\include\Devassert.h
- ..\Base_TS_T40D2M10I1R0\include\Gpt_MemMap.h
- ..\Base_TS_T40D2M10I1R0\include\StandardTypes.h
- ..\Base_TS_T40D2M10I1R0\generate_PC.h
- ..\Base_TS_T40D2M10I1R0\header\S32K116_FTM.h
- ..\Base_TS_T40D2M10I1R0\header\S32K118_FTM.h
- ..\Base_TS_T40D2M10I1R0\header\S32K142_FTM.h
- ..\Base_TS_T40D2M10I1R0\header\S32K142W_FTM.h

- ..\Base_TS_T40D2M10I1R0\header\S32K144_FTM.h
- ..\Base_TS_T40D2M10I1R0\header\S32K144W_FTM.h
- ..\Base_TS_T40D2M10I1R0\header\S32K146_FTM.h
- ..\Base_TS_T40D2M10I1R0\header\S32K148_FTM.h
- ..\Base_TS_T40D2M10I1R0\header\S32K116_LPIT.h
- ..\Base_TS_T40D2M10I1R0\header\S32K118_LPIT.h
- ..\Base_TS_T40D2M10I1R0\header\S32K142_LPIT.h
- ..\Base_TS_T40D2M10I1R0\header\S32K142W_LPIT.h
- ..\Base_TS_T40D2M10I1R0\header\S32K144_LPIT.h
- ..\Base_TS_T40D2M10I1R0\header\S32K144W_LPIT.h
- ..\Base_TS_T40D2M10I1R0\header\S32K146_LPIT.h
- ..\Base_TS_T40D2M10I1R0\header\S32K148_LPIT.h
- ..\Base_TS_T40D2M10I1R0\header\S32K116_LPTMR.h
- ..\Base_TS_T40D2M10I1R0\header\S32K118_LPTMR.h
- ..\Base_TS_T40D2M10I1R0\header\S32K142_LPTMR.h
- ..\Base_TS_T40D2M10I1R0\header\S32K142W_LPTMR.h
- ..\Base_TS_T40D2M10I1R0\header\S32K144_LPTMR.h
- ..\Base_TS_T40D2M10I1R0\header\S32K144W_LPTMR.h
- ..\Base_TS_T40D2M10I1R0\header\S32K146_LPTMR.h
- ..\Base_TS_T40D2M10I1R0\header\S32K148_LPTMR.h
- ..\Base_TS_T40D2M10I1R0\header\S32K116_RTC.h
- ..\Base_TS_T40D2M10I1R0\header\S32K118_RTC.h
- ..\Base_TS_T40D2M10I1R0\header\S32K142_RTC.h
- ..\Base_TS_T40D2M10I1R0\header\S32K142W_RTC.h
- ..\Base_TS_T40D2M10I1R0\header\S32K144_RTC.h
- ..\Base_TS_T40D2M10I1R0\header\S32K144W_RTC.h
- ..\Base_TS_T40D2M10I1R0\header\S32K146_RTC.h
- ..\Base_TS_T40D2M10I1R0\header\S32K148_RTC.h

Files from Det folder:

- ..\Det_TS_T40D2M10I1R0\include\Det.h

3.3 Setting up the plugins

The GPT driver was designed to be configured by using the EB Tresos Studio (version EB tresos Studio 27.1.0 or later).

3.3.1 Location of various files inside the Gpt module folder

VSMD (Vendor Specific Module Definition) file in EB tresos Studio XDM format:

- ..\Gpt_TS_T40D2M10I1R0\config\Gpt.xdm
- ..\Base_TS_T40D2M10I1R0\config\Base.xdm
- ..\Resource_TS_T40D2M10I1R0\config\Resource.xdm VSMD (Vendor Specific Module Definition) file(s) in AUTOSAR compliant EPD format:
- ..\Gpt_TS_T40D2M10I1R0\autosar\Gpt.epd
- ..\Base_TS_T40D2M10I1R0\autosar\Base.epd
- ..\Resource_TS_T40D2M10I1R0\autosar\Resource.epd Code Generation Templates for Pre-Compile time configuration parameters:
- ..\Gpt_TS_T40D2M10I1R0\include\Gpt_Cfg.h
- ..\Gpt_TS_T40D2M10I1R0\include\LPit_Gpt_Ip_Cfg.h
- ..\Gpt_TS_T40D2M10I1R0\include\LPit_Gpt_Ip_Cfg_Defines.h
- ..\Gpt_TS_T40D2M10I1R0\include\SRtc_Gpt_Ip_Cfg.h
- ..\Gpt_TS_T40D2M10I1R0\include\SRtc_Gpt_Ip_Cfg_Defines.h
- ..\Gpt_TS_T40D2M10I1R0\include\Lptmr_Gpt_Ip_Cfg.h
- ..\Gpt_TS_T40D2M10I1R0\include\Lptmr_Gpt_Ip_Cfg_Defines.h
- ..\Gpt_TS_T40D2M10I1R0\include\Ftm_Gpt_Ip_Cfg.h
- ..\Gpt_TS_T40D2M10I1R0\include\Ftm_Gpt_Ip_Cfg_Defines.h
- ..\Gpt_TS_T40D2M10I1R0\src\Gpt_Cfg.c

3.3.2 Dependencies

- RESOURCE is required to select processor derivative. Current Gpt driver has support for the following derivatives, each one having attached a Resource file: s32k116_qfn32,s32k116_lqfp48,s32k118↩ _lqfp48,s32k118_lqfp64,s32k142_lqfp48,s32k142_lqfp64,s32k142_lqfp100,s32k142w_lqfp48,s32k142w_↩ lqfp64,s32k144_lqfp48,s32k144_lqfp64,s32k144_lqfp100,s32k144_mapbga100,s32k144w_lqfp48,s32k144w↩ _lqfp64,s32k146_lqfp64,s32k146_lqfp100,s32k146_mapbga100,s32k146_lqfp144,s32k148_lqfp100,s32k148↩ _mapbga100,s32k148_lqfp144,s32k148_lqfp176
- DET is required for signalling the development error detection (parameters out of range, null pointers, etc).
- BASE is required for Gpt specific header files and other header definitions.

Chapter 4

Function calls to module

4.1 Function Calls during Start-up

GPT shall be initialized during STARTUP1 phase of EcuM initialization. The API to be called for this is Gpt_Init() MCU module shall be initialized before GPT is initialized.

4.2 Function Calls during Shutdown

If GptWakeupFunctionalityApi and GptWakeupSourceRef are enabled, Gpt_SetMode(GPT_MODE_SLEEP) API shall be called during GO SLEEP phase of EcuM to configure the hardware for Sleep mode.

4.3 Function Calls during Wake-up

For the platforms where the GPT driver controls wakeup hw sources, if the GptWakeupFunctionalityApi and Gpt↩ WakeupSourceRef are enabled, the driver shall report the wakeup event to EcuM through EcuM_SetWakeup↩ Event(Source) upon the hw source event.

Chapter 5

Module requirements

- Exclusive areas to be defined in BSW scheduler
- Exclusive areas not available on this platform
- Peripheral Hardware Requirements
- ISR to configure within AutosarOS - dependencies
- ISR Macro
- Other AUTOSAR modules - dependencies
- Data Cache Restrictions
- User Mode support
- Multicore support

5.1 Exclusive areas to be defined in BSW scheduler

In the current implementation, GPT is using the services of Schedule Manager (SchM) for entering and exiting the exclusive areas. The following critical regions are used in the GPT driver:

GPT_EXCLUSIVE_AREA_50 is used in function Gpt_Init to protect the LPIT_MCR register from read/modify/write.

GPT_EXCLUSIVE_AREA_51 is used in function Gpt_Init to protect the LPIT_TMR_TCTRL register from read/modify/write.

GPT_EXCLUSIVE_AREA_52 is used in function Gpt_Init to protect the LPIT_TMR_TCTRL register from read/modify/write.

GPT_EXCLUSIVE_AREA_52 is used in function Gpt_DeInit to protect the LPIT_TMR_TCTRL register from read/modify/write.

GPT_EXCLUSIVE_AREA_53 is used in function Gpt_Init to protect the LPIT_MCR register from read/modify/write.

GPT_EXCLUSIVE_AREA_53 is used in function Gpt_DeInit to protect the LPIT_MCR register from read/modify/write.

GPT_EXCLUSIVE_AREA_54 is used in function Gpt_Init to protect the LPIT_MCR register from read/modify/write.

GPT_EXCLUSIVE_AREA_54 is used in function Gpt_DeInit to protect the LPIT_MCR register from read/modify/write.

GPT_EXCLUSIVE_AREA_55 is used in function Gpt_Init to protect the LPIT_MIER register from read/modify/write.

GPT_EXCLUSIVE_AREA_55 is used in function Gpt_DeInit to protect the LPIT_MIER register from read/modify/write.

GPT_EXCLUSIVE_AREA_55 is used in function Gpt_EnableNotification to protect the LPIT_MIER register from read/modify/write.

GPT_EXCLUSIVE_AREA_55 is used in function Gpt_DisableNotification to protect the LPIT_MIER register from read/modify/write.

GPT_EXCLUSIVE_AREA_56 is used in function Gpt_Channel_EnableChainMode to protect the LPIT_↩ TMR_TCTRL register from read/modify/write.

GPT_EXCLUSIVE_AREA_56 is used in function Gpt_Channel_DisableChainMode to protect the LPIT↩ _TMR_TCTRL register from read/modify/write.

GPT_EXCLUSIVE_AREA_60 is used in function Gpt_Init to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_60 is used in function Gpt_EnableNotification to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_60 is used in function Gpt_DisableNotification to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_61 is used in function Gpt_Init to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_61 is used in function Gpt_EnableNotification to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_61 is used in function Gpt_DisableNotification to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_62 is used in function Gpt_Init to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_62 is used in function Gpt_EnableNotification to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_62 is used in function Gpt_DisableNotification to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_63 is used in function Gpt_Init to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_63 is used in function Gpt_EnableNotification to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_63 is used in function Gpt_DisableNotification to protect the RTC_IER register from read/modify/write.

GPT_EXCLUSIVE_AREA_64 is used in function Gpt_DeInit to protect the RTC_CR register from read/modify/write.

GPT_EXCLUSIVE_AREA_65 is used in function Gpt_Init to protect the RTC_CR register from read/modify/write.

GPT_EXCLUSIVE_AREA_65 is used in function Gpt_StartTimer to protect the RTC_CR register from read/modify/write.

GPT_EXCLUSIVE_AREA_66 is used in function Gpt_Init to protect the RTC_SR register from read/modify/write.

GPT_EXCLUSIVE_AREA_67 is used in function Gpt_Init to protect the RTC_SR register from read/modify/write.

GPT_EXCLUSIVE_AREA_17 is used in function Gpt_Init to protect the CONF register from read/modify/write.

GPT_EXCLUSIVE_AREA_17 is used in function Gpt_DeInit to protect the CONF register from read/modify/write.

GPT_EXCLUSIVE_AREA_17 is used in function Gpt_Init to protect the CONF register from read/modify/write.

GPT_EXCLUSIVE_AREA_18 is used in function Gpt_Init to protect the SC and CONF register from read/modify/write.

GPT_EXCLUSIVE_AREA_20 is used in function Gpt_Init to protect the SC register from read/modify/write.

GPT_EXCLUSIVE_AREA_21 is used in function Gpt_Init to protect the SC register from read/modify/write.

GPT_EXCLUSIVE_AREA_22 is used in function Gpt_Init to protect the CSC register from read/modify/write.

GPT_EXCLUSIVE_AREA_22 is used in function Gpt_DeInit to protect the CSC register from read/modify/write.

GPT_EXCLUSIVE_AREA_22 is used in function Gpt_StartTimer to protect the CSC register from read/modify/write.

GPT_EXCLUSIVE_AREA_22 is used in function Gpt_StopTimer to protect the CSC register from read/modify/write.

GPT_EXCLUSIVE_AREA_23 is used in function Gpt_Init to protect the CSC register from read/modify/write.

GPT_EXCLUSIVE_AREA_23 is used in function Gpt_DeInit to protect the CSC register from read/modify/write.

GPT_EXCLUSIVE_AREA_23 is used in function Gpt_StartTimer to protect the CSC register from read/modify/write.

GPT_EXCLUSIVE_AREA_23 is used in function Gpt_StopTimer to protect the CSC register from read/modify/write.

GPT_EXCLUSIVE_AREA_24 is used in function Gpt_Init to protect the SC register from read/modify/write.

GPT_EXCLUSIVE_AREA_24 is used in function Gpt_DeInit to protect the SC register from read/modify/write.

GPT_EXCLUSIVE_AREA_24 is used in function Gpt_StartTimer to protect the SC register from read/modify/write.

GPT_EXCLUSIVE_AREA_24 is used in function Gpt_StopTimer to protect the SC register from read/modify/write.

GPT_EXCLUSIVE_AREA_25 is used in function Gpt_Init to protect the MODE register from read/modify/write.

GPT_EXCLUSIVE_AREA_25 is used in function Gpt_DeInit to protect the MODE register from read/modify/write.

GPT_EXCLUSIVE_AREA_25 is used in function Gpt_StartTimer to protect the MODE register from read/modify/write.

GPT_EXCLUSIVE_AREA_25 is used in function Gpt_StopTimer to protect the MODE register from read/modify/write.

GPT_EXCLUSIVE_AREA_26 is used in function Gpt_Init to protect the CSC register from read/modify/write.

GPT_EXCLUSIVE_AREA_27 is used in function Gpt_SetClockMode to protect the SC register from read/modify/write.

GPT_EXCLUSIVE_AREA_28 is used in function Gpt_Init to protect the QDCTRL and SC register from read/modify/write.

GPT_EXCLUSIVE_AREA_40 is used in function Gpt_Init to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_40 is used in function Gpt_DeInit to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_40 is used in function Gpt_StartTimer to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_40 is used in function Gpt_StopTimer to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_41 is used in function Gpt_Init to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_41 is used in function Gpt_DeInit to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_41 is used in function Gpt_EnableNotification to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_41 is used in function Gpt_DisableNotification to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_42 is used in function Gpt_Init to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_42 is used in function Gpt_StopTimer to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_42 is used in function Gpt_DisableNotification to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_42 is used in function Gpt_DeInit to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_43 is used in function Gpt_Init to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_44 is used in function Gpt_Init to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_44 is used in function Gpt_DeInit to protect the LPTMR_CSR register from read/modify/write.

GPT_EXCLUSIVE_AREA_45 is used in function Gpt_Init to protect the LPTMR_CMR register from read/modify/write.

Exclusive Areas implemented in Low level driver layer (IPL)

GPT_EXCLUSIVE_AREA_46 is used in function Lptmr_Gpt_Ip_SetCompareValue to protect the updates for:

- CMR

GPT_EXCLUSIVE_AREA_50 is used in function Lpit_Gpt_Ip_EnableMdlClk to protect the updates for:

- LPIT_MCR

GPT_EXCLUSIVE_AREA_51 is used in function Lpit_Gpt_Ip_TimerEnable to protect the updates for:

- LPIT_TMR_TCTRL

GPT_EXCLUSIVE_AREA_52 is used in function Lpit_Gpt_Ip_SetMode to protect the updates for:

- LPIT_TMR_TCTRL

GPT_EXCLUSIVE_AREA_53 is used in function Lpit_Gpt_Ip_SetDebugMode to protect the updates for:

- LPIT_MCR

GPT_EXCLUSIVE_AREA_54 is used in function Lpit_Gpt_Ip_SetDozeMode to protect the updates for:

- LPIT_MCR

GPT_EXCLUSIVE_AREA_55 is used in function Lpit_Gpt_Ip_InterruptTimerChannels to protect the updates for:

- LPIT_MIER

GPT_EXCLUSIVE_AREA_56 is used in function Lpit_Gpt_Ip_SetChainMode to protect the updates for:

- LPIT_TMR_TCTRL

GPT_EXCLUSIVE_AREA_60 is used in function Srtc_Ip_SetTimeInvalidInterrupt to protect the updates for:

- RTC_IER

GPT_EXCLUSIVE_AREA_61 is used in function Srtc_Ip_SetTimeOverflowInterrupt to protect the variables for:

- RTC_IER

GPT_EXCLUSIVE_AREA_62 is used in function Srtc_Ip_SetTimeOverflowInterrupt to protect the variables for:

- RTC_IER

GPT_EXCLUSIVE_AREA_63 is used in function Srtc_Ip_SetTimeAlarmInterrupt to protect the variables for:

- RTC_IER

GPT_EXCLUSIVE_AREA_64 is used in function Srtc_Ip_SoftwareReset to protect the variables for:

- RTC_CR

GPT_EXCLUSIVE_AREA_65 is used in function Srtc_Ip_CounterEnable to protect the variables for:

- RTC_SR

GPT_EXCLUSIVE_AREA_66 is used in function Srtc_Ip_SelectClock to protect the variables for:

- RTC_CR

GPT_EXCLUSIVE_AREA_67 is used in function Srtc_Ip_SelectClockOut to protect the variables for:

- RTC_CR

GPT_EXCLUSIVE_AREA_17 is used in function Ftm_Gpt_Ip_SetFreezebit to protect the updates for:

- FTM_CONF

GPT_EXCLUSIVE_AREA_18 is used in function Ftm_Gpt_Ip_PredefConfigure to protect the updates for:

- FTM_SC
- FTM_CONF

GPT_EXCLUSIVE_AREA_20 is used in function Ftm_Gpt_Ip_EnableTOIEflag to protect the updates for:

- FTM_SC

GPT_EXCLUSIVE_AREA_21 is used in function Ftm_Gpt_Ip_Configure to protect the updates for:

- FTM_SC

GPT_EXCLUSIVE_AREA_22 is used in function Ftm_Gpt_Ip_ClearInterruptFlag to protect the updates for:

- FTM_CSC

GPT_EXCLUSIVE_AREA_23 is used in function Ftm_Gpt_Ip_EnableInterrupt to protect the updates for:

- FTM_CSC

GPT_EXCLUSIVE_AREA_24 is used in function Ftm_Gpt_Ip_SetClockSource to protect the updates for:

- FTM_SC

GPT_EXCLUSIVE_AREA_25 is used in function Ftm_Gpt_Ip_FTMEnable to protect the updates for:

- FTM_MODE

GPT_EXCLUSIVE_AREA_26 is used in function Ftm_Gpt_Ip_ModeSelectA to protect the updates for:

- FTM_CSC

GPT_EXCLUSIVE_AREA_27 is used in function Ftm_Gpt_Ip_SetPrescaler to protect the updates for:

- FTM_SC

GPT_EXCLUSIVE_AREA_28 is used in function Ftm_Gpt_Ip_EnableQUADENbit and Ftm_Gpt_Ip_↩ EnableCPWMS to protect the updates for:

- FTM_QDCTRL
- FTM_SC

GPT_EXCLUSIVE_AREA_46 is used in function Lptmr_Gpt_Ip_SetCompareValue to protect the updates for:

- LPTMR_CMR

Global Variable /Function name	Lpit_Gpt_Ip_EnableMdlClk	Lpit_Gpt_Ip_TimerEnable	Lpit_Gpt_Ip_SetTrigger	Lpit_Gpt_Ip_SetMode	Lpit_Gpt_Ip_SetDebugMode	Lpit_Gpt_Ip_SetDozeMode	Lpit_Gpt_Ip_InterruptTimerChannels	Lpit_Gpt_Ip_SetChainMode
GPT_EXCLUSIVE_AREA_50	x							
GPT_EXCLUSIVE_AREA_51		x						
GPT_EXCLUSIVE_AREA_52				x				
GPT_EXCLUSIVE_AREA_53					x			
GPT_EXCLUSIVE_AREA_54						x		
GPT_EXCLUSIVE_AREA_55							x	
GPT_EXCLUSIVE_AREA_56								x

Figure 5.1 Extracted table from RTD_GPT_EXCLUSIVE_AREAS.xlsx

Global Variable /Function name	Srtc_Ip_SetTimeInvalidInterrupt	Srtc_Ip_SetTimeOverflowInterrupt	Srtc_Ip_SetTimeAlarmInterrupt	Srtc_Ip_SetTimeSecondsInterrupt	Srtc_Ip_SoftwareReset	Srtc_Ip_CounterEnable	Srtc_Ip_IsCounterEnable	Srtc_Ip_SelectClock	Srtc_Ip_SelectClockOut
GPT_EXCLUSIVE_AREA_60	x								
GPT_EXCLUSIVE_AREA_61		x							
GPT_EXCLUSIVE_AREA_62			x						
GPT_EXCLUSIVE_AREA_63				x					
GPT_EXCLUSIVE_AREA_64					x				
GPT_EXCLUSIVE_AREA_65						x			
GPT_EXCLUSIVE_AREA_66								x	
GPT_EXCLUSIVE_AREA_67									x

Figure 5.2 Extracted table from RTD_GPT_EXCLUSIVE_AREAS.xlsx

Global Variable /Function name	Ftm_Gpt_Ip_StartPredefTimer	Ftm_Gpt_Ip_StopPredefTimer	Ftm_Gpt_Ip_SetFreezebit	Ftm_Gpt_Ip_Configure	Ftm_Gpt_Ip_SetCounterInitVal	Ftm_Gpt_Ip_SetCounter	Ftm_Gpt_Ip_ClearInterruptFlag	Ftm_Gpt_Ip_EnableInterrupt	Ftm_Gpt_Ip_SetClockSource	Ftm_Gpt_Ip_FTMEnable	Ftm_Gpt_Ip_SetCompareValue	Ftm_Gpt_Ip_WriteModulo	Ftm_Gpt_Ip_GetCounter	Ftm_Gpt_Ip_GetCntValue	Ftm_Gpt_Ip_ModeSelectA	Ftm_Gpt_Ip_SetHalfCycleValue	Ftm_Gpt_Ip_SetPrescaler
GPT_EXCLUSIVE_AREA_17			x														
GPT_EXCLUSIVE_AREA_20																	
GPT_EXCLUSIVE_AREA_21				x													
GPT_EXCLUSIVE_AREA_22							x										
GPT_EXCLUSIVE_AREA_23								x									
GPT_EXCLUSIVE_AREA_24									x								
GPT_EXCLUSIVE_AREA_25										x							
GPT_EXCLUSIVE_AREA_26															x		
GPT_EXCLUSIVE_AREA_27																	x
GPT_EXCLUSIVE_AREA_28	x																

Figure 5.3 Extracted table from RTD_GPT_EXCLUSIVE_AREAS.xlsx

Global Variable /Function name	Lptmr_Gpt_Ip_TimerEnable	Lptmr_Gpt_Ip_InterruptEnable	Lptmr_Gpt_Ip_ClearCompareFlag	Lptmr_Gpt_Ip_TimerModeSelect	Lptmr_Gpt_Ip_SetPrescaler	Lptmr_Gpt_Ip_Configure	Lptmr_Gpt_Ip_WriteCompareValue	Lptmr_Gpt_Ip_WriteCounterValue	Lptmr_Gpt_Ip_CompareValue
GPT_EXCLUSIVE_AREA_40	x								
GPT_EXCLUSIVE_AREA_41		x							
GPT_EXCLUSIVE_AREA_42			x						
GPT_EXCLUSIVE_AREA_43				x					
GPT_EXCLUSIVE_AREA_44						x			
GPT_EXCLUSIVE_AREA_45									x

Figure 5.4 Extracted table from RTD__GPT__EXCLUSIVE__AREAS.xlsx

The critical regions from interrupts are grouped in “Interrupt Service Routines Critical Regions (composed diagram)”. If an exclusive area is “exclusive” with the composed “Interrupt Service Routines Critical Regions (composed diagram)” group, it means that it is exclusive with each one of the ISR critical regions.

5.2 Exclusive areas not available on this platform

List of exclusive areas which are not available on this platform (or blank if they're all available).

None.

5.3 Peripheral Hardware Requirements

Driver implements channels on S32K1xx peripherals :

- Low Power Timer (LPTMR) : 1 instances $*$ 1 channels => 1 channels are implemented.
- Low Power Interrupt Timer (LPIT) : 1 instance $*$ 4 channels => 4 channels are implemented.
- Real Time Clock (SRTC) : 1 instance $*$ 1 channel => 1 channel is implemented.
- FlexTimer (FTM) : 8 instances $*$ 8 channels => 64 channels are implemented.

5.4 ISR to configure within AutosarOS - dependencies

isr to configure within AutosarOS dependencies template.

Flextrimer interrupts

FlexTimer Module Interrupts	HW INT Vector	Observations
FTM_0_CH_0_CH_1_ISR	115	None
FTM_0_CH_2_CH_3_ISR	116	None
FTM_0_CH_4_CH_5_ISR	117	None
FTM_0_CH_6_CH_7_ISR	118	None
FTM_0_OVF_ISR	120	None
FTM_1_CH_0_CH_1_ISR	121	None
FTM_1_CH_2_CH_3_ISR	122	None
FTM_1_CH_4_CH_5_ISR	123	None
FTM_1_CH_6_CH_7_ISR	124	None
FTM_1_OVF_ISR	126	None
FTM_2_CH_0_CH_1_ISR	127	None
FTM_2_CH_2_CH_3_ISR	128	None
FTM_2_CH_4_CH_5_ISR	129	None
FTM_2_CH_6_CH_7_ISR	130	None
FTM_2_OVF_ISR	132	None
FTM_3_CH_0_CH_1_ISR	133	None
FTM_3_CH_2_CH_3_ISR	134	None
FTM_3_CH_4_CH_5_ISR	135	None
FTM_3_CH_6_CH_7_ISR	136	None
FTM_3_OVF_ISR	138	None
FTM_4_CH_0_CH_1_ISR	139	None
FTM_4_CH_2_CH_3_ISR	140	None
FTM_4_CH_4_CH_5_ISR	141	None
FTM_4_CH_6_CH_7_ISR	142	None
FTM_4_OVF_ISR	144	None
FTM_5_CH_0_CH_1_ISR	145	None
FTM_5_CH_2_CH_3_ISR	146	None
FTM_5_CH_4_CH_5_ISR	147	None
FTM_5_CH_6_CH_7_ISR	148	None
FTM_5_OVF_ISR	150	None
FTM_6_CH_0_CH_1_ISR	151	None
FTM_6_CH_2_CH_3_ISR	152	None
FTM_6_CH_4_CH_5_ISR	153	None
FTM_6_CH_6_CH_7_ISR	154	None
FTM_6_OVF_ISR	156	None
FTM_7_CH_0_CH_1_ISR	157	None
FTM_7_CH_2_CH_3_ISR	158	None
FTM_7_CH_4_CH_5_ISR	159	None
FTM_7_CH_6_CH_7_ISR	160	None

External LPTMR (Low power timer) Interrupts

LPTMR Module Interrupts	HW INT Vector	Observations
LPTMR_0_CH_0_ISR	74	None

LPIT Interrupts

LPIT Interrupts	HW INT Vector	Observations
LPIT_0_CH_0_ISR	64	None
LPIT_0_CH_1_ISR	65	None
LPIT_0_CH_2_ISR	66	None
LPIT_0_CH_3_ISR	67	None

External SRTC (Real Time Clock) Interrupts

SRTC Module Interrupts	HW INT Vector	Observations
SRTC_0_Ch_0_ISR	46	None

5.5 ISR Macro

RTD drivers use the ISR macro to define the functions that will process hardware interrupts. Depending on whether the OS is used or not, this macro can have different definitions.

5.5.1 Without an Operating System

The macro *USING_OS_AUTOSAROS* must not be defined.

5.5.1.1 Using Software Vector Mode

The macro *USE_SW_VECTOR_MODE* must be defined and the ISR macro is defined as:

```
#define ISR(IsrName) void IsrName(void)
```

In this case, the drivers' interrupt handlers are normal C functions and their prologue/epilogue will handle the context save and restore.

5.5.1.2 Using Hardware Vector Mode

The macro *USE_SW_VECTOR_MODE* must not defined and the ISR macro is defined as:

```
#define ISR(IsrName) INTERRUPT_FUNC void IsrName(void)
```

In this case, the drivers' interrupt handlers must also handle the context save and restore.

5.5.2 With an Operating System

Please refer to your OS documentation for description of the ISR macro.

5.6 Other AUTOSAR modules - dependencies

- BASE - The BASE module contains the common files/definitions needed by all MCAL modules.
- DET - Development Error Tracer: This module is necessary for enabling Development error detection. The API function used is Det_ReportError(). Activation of Development error detection is configurable using 'GptDevErrorDetect' configuration parameter.
- DEM - Diagnostic Event Manager: This module is necessary for enabling reporting of production relevant error status. It is not used with current GPT implementation as the production relevant error codes are not present.
- EcuC - This module is necessary for handling PostBuild Variant. It allows users to configure multiple configuration.
- RESOURCE - The RESOURCE module is used to select microcontroller's derivatives.

5.7 Data Cache Restrictions

None.

5.8 User Mode support

- User Mode configuration in the module
- User Mode configuration in AutosarOS

5.8.1 User Mode configuration in the module

5.8.2 User Mode configuration in AutosarOS

When User mode is enabled, the driver may has the functions that need to be called as trusted functions in AutosarOS context. Those functions are already defined in driver and declared in the header `<IpName>_Ip↩ _TrustedFunctions.h`. This header also included all headers files that contains all types definition used by parameters or return types of those functions. Refer the chapter User Mode configuration in the module for more detail about those functions and the name of header files they are declared inside. Those functions will be called indirectly with the naming convention below in order to AutosarOS can call them as trusted functions.

```
Call_<Function_Name>_TRUSTED(parameter1,parameter2,...)
```

That is the result of macro expansion `OsIf_Trusted_Call` in driver code:

`#define` OsIf_Trusted_Call[1-6params](name,param1,...,param6) Call_##name##_TRUSTED(param1,...,param6)

So, the following steps need to be done in AutosarOS:

- Ensure `MCAL_ENABLE_USER_MODE_SUPPORT` macro is defined in the build system or somewhere global.
- Define and declare all functions that need to call as trusted functions follow the naming convention above in Integration/User code. They need to visible in `Os.h` for the driver to call them. They will do the marshalling of the parameters and call `CallTrustedFunction()` in OS specific manner.
- `CallTrustedFunction()` will switch to privileged mode and call `TRUSTED_<Function_Name>()`.
- `TRUSTED_<Function_Name>()` function is also defined and declared in Integration/User code. It will unmarshalling of the parameters to call `<Function_Name>()` of driver. The `<Function_Name>()` functions are already defined in driver and declared in `<IpName>_Ip_TrustedFunctions.h`. This header should be included in OS for OS call and indexing these functions.

See the sequence chart below for an example calling `Linflexd_Uart_Ip_Init_Privileged()` as a trusted function.

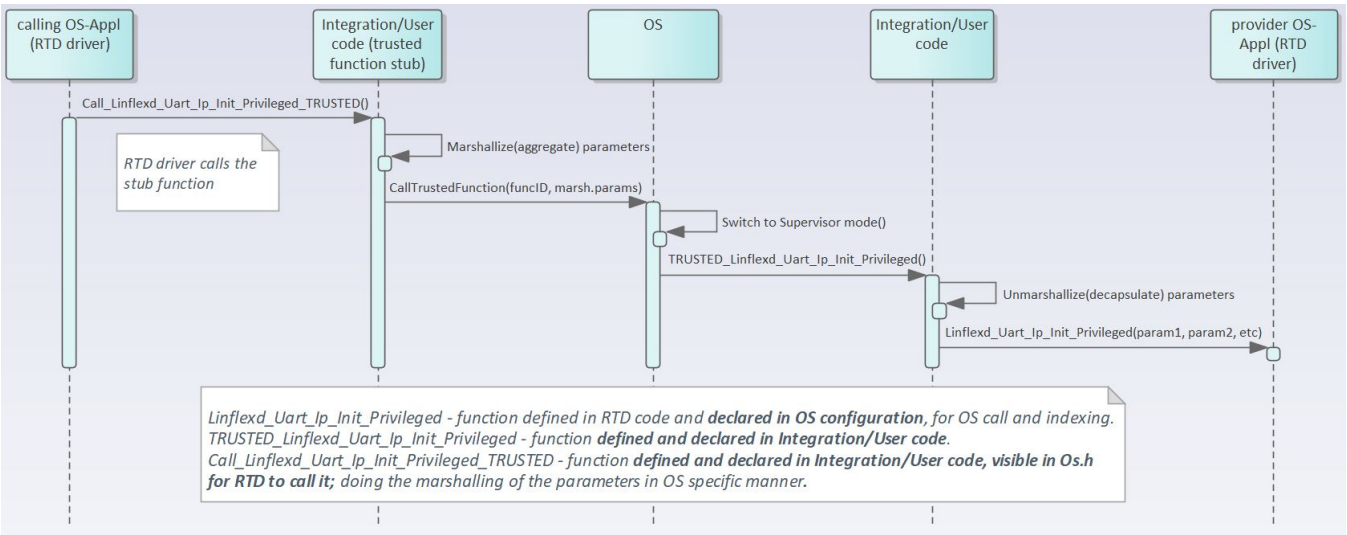

Figure 5.5 Example sequence chart for calling `Linflexd_Uart_Ip_Init_Privileged` as trusted function

5.9 Multicore support

1.** The Gpt implements the "Autosar 4.4 MCAL Multicore Distribution" according to type II, in which the mappable element is set to Hw_Unit for FTM Ip , LPIT Ip, RTC Ip and LPTMR Ip. For additional details, please refer to AUTOSAR_EXP_BSWDistributionGuide.

2.** The Gpt and the mappable elements can be allocated to zero, one or several ECUC partitions, by means of "GptEcucPartionRef". If the Gpt is mapped to zero ECUC partitions, the Gpt behavior reverts to single-core implementation, similar to previous Autosar versions. If the Gpt is mapped to one or more ECUC partitions, the Gpt enforces the following multi-core assumptions:

The Gpt assumes there is a single EcucPartition allocated per core. Internally, the module will use the Core ID returned by GetCoreID API to reference the appropriate global data and configuration elements. The Gpt assumes the EcucCoreIDs are defined in a compact/consecutive order, starting from zero. The rationale is that the number of

EcucPartitions is used for dimensioning the Gpt internal variables and the EcucCoreIDs are used for indexing those variables. The Gpt assumes that initialization is performed on each core, Gpt_Init() is called separately for each core, using a different configguration structure. (Type II) The Gpt initialization expects the upper layer will pass the correct initialization pointer, specific to the partition in which the driver is to be used. For example: EcucPartition_1 is assigned to CoreID 1; Gpt_Init function will be called with Gpt_Config_EcucPartition_1 configuration structure, on Core 1. The Gpt will check upon each API call if the requested resource is configured to be available on the current core, if DET error reporting is enabled. The Gpt requires that all variables in NonCacheable MemMap sections be allocated accordingly, to avoid data corruption in multicore context. The Gpt assumes that RTE module implements the EXCLUSIVE AREAS to be core-aware only. The rationale is that the module implementation ensures data integrity by separating the mappable elements for different cores already, thus implementing the EX↩ CLUSIVE AREAS in a blocking manner (ex: spin-lock) on a multicore scope, might affect the performance of the drivers on the two cores, although they might access separate HW elements. For single-core scope, the EXCLUSIVE AREAS keep the same purpose as on previous AUTOSAR implementations. The Gpt assumes that each interrupt is routed by the system only to the core on which is supposed to be serviced. The configuration structure name shall be available in the caller scope of Gpt_Init function by being declared with EXTERN, according to its generated name.

Module specific limitation:∗∗

For current implementation, Gpt driver does not support channel mapping with zero ECUC partition in configuration. Therefore the driver will force user to map each channel with one partition only.

Current implementation of GPT driver does not allow for a partition with no allocated channels to access the predefined timer info – if any of the predefined timers are defined. The GPT driver issues a DET for this access if the API call is present in user code

Chapter 6

Main API Requirements

6.1 Main function calls within BSW scheduler

None.

6.2 API Requirements

None.

6.3 Calls to Notification Functions, Callbacks, Callouts

Call-back Notifications:

- There are no call-back notifications defined inside the GPT driver.

User Notification:

- The GPT Driver provides a notification per channel that is called whenever the defined time period is over.
- The notifications can be configured as pointers to user defined functions. If notification is not desired,

'NULL_PTR' shall be configured.

An example of the syntax of this function is as follows:

- void Gpt_Notification_<channel>(void)
- An extern declaration of this function is available in Gpt_PBcfg.c. The function has to be implemented by the user.

Chapter 7

Memory allocation

7.1 Sections to be defined in Gpt_MemMap.h

Section name	Type of section	Description
GPT_START_SEC_CONFIG_DATA↩ _UNSPECIFIED	Configuration Data	Start of Memory Section for Config Data
GPT_STOP_SEC_CONFIG_DATA_↩ UNSPECIFIED	Configuration Data	End of memory Section for Config Data
GPT_START_SEC_CODE	Code	Start of memory Section for Code
GPT_STOP_SEC_CODE	Code	End of memory Section for Code
GPT_START_SEC_VAR_INIT_UNS↩ PECIFIED	Variables	Start of memory Section for Variables
GPT_STOP_SEC_VAR_INIT_UNSP↩ ECIFIED	Variables	End of memory Section for Variables
GPT_START_SEC_VAR_CLEARED↩ _UNSPECIFIED	Variables	Start of memory Section for Variables. Used for variables, constants, structure, array and unions when SIZE (alignment) does not fit the criteria of 8,16 or 32 bit. For instance used for variables of unknown size
GPT_STOP_SEC_VAR_CLEARED_↩ UNSPECIFIED	Variables	End of memory Section for Variables. Used for variables, constants, structure, array and unions when SIZE (alignment) does not fit the criteria of 8,16 or 32 bit. For instance used for variables of unknown size

7.2 Linker command file

Memory shall be allocated for every section defined in the driver's "<Module>"_MemMap.h.

Chapter 8

Integration Steps

This section gives a brief overview of the steps needed for integrating this module:

1. Generate the required module configuration(s). For more details refer to section Files Required for Compilation
2. Allocate the proper memory sections in the driver's memory map header file ("<Module>"_MemMap.h) and linker command file. For more details refer to section Sections to be defined in <Module>_MemMap.h
3. Compile & build the module with all the dependent modules. For more details refer to section Building the Driver

Chapter 9

External assumptions for driver

The section presents requirements that must be complied with when integrating the GPT driver into the application.

External Assumption Req ID	External Assumption Text
SWS_Gpt_00353	If the register can affect several hardware modules and if it is an I/O register it shall be initialized by the PORT driver. Note: The GPT driver manages hardware which does not include input/output configurable pins.
SWS_Gpt_00354	If the register can affect several hardware modules and if it is not an I/O register it shall be initialized by the MCU driver. Note: The requirement is implicitly fulfilled at MCU level, as the MCU shall initialize the clock tree used also by the GPT driver.
SWS_Gpt_00355	One-time writable registers that require initialization directly after reset shall be initialized by the startup code. Note: to be traced at the sMCAL generic level; no verification done on driver level.The Interrupt Controller shall be initialized by the integrating application before to start using the GPTdriver.
SWS_Gpt_00356	All other registers shall be initialized by the startup code. Note: to be traced at the sMCAL generic level; no verification done on driver level.The Interrupt Controller shall be initialized by the integrating application before to start using the GPTdriver.
EA_RTD_00032	The application shall not preempt a channel related function (like starting/stoping a timer) by calling Gpt_SetMode() or Gpt_DeInit().
EA_RTD_00033	The application shall not preempt a GPT function working on a GPT channel by calling another GPT function targeting the same channel.
EA_RTD_00034	The application must not concurrently call Gpt functions with one exception: GetVersionInfo only can get interrupted or may interrupt. Note: A transversal GPT functions are those functions addressing the entire set of channels, like Gpt_Init(), Gpt_DeInit(), Gpt_SetMode(), Gpt_Periodic↩ Check(), ...
EA_RTD_00035	The application shall not call any function of the GPT module before having called Gpt_Init.
EA_RTD_00036	Wakeup enabled timers shall be started or stopped only when GPT driver is in GPT_MODE_NORMAL mode.The external application shall invoke Gpt_EnableWakeup() and Gpt_DisableWakeup() only when GPT driver is in GPT_MODE_NORMAL mode. Note: If Gpt_EnableWakeup(), Gpt↩ _DisableWakeup(), Gpt_StartTimer() and Gpt_StopTimer() are called while GPT is already in SLEEP mode, the GPT driver behavior is not guaranteed. Therefore any wakeup channel configuration shall be done before entering in sleep mode.

External Assumption Req ID	External Assumption Text
EA_RTD_00071	If interrupts are locked, a centralized function pair to lock and unlock interrupts shall be used.
EA_RTD_00081	The integrator shall assure that <MSN>_Init() and <MSN>_DeInit() functions do not interrupt each other.
EA_RTD_00082	When caches are enabled and data buffers are allocated in cacheable memory regions the buffers involved in DMA transfer shall be aligned with both start and end to cache line size. Note: **Rationale**: This ensures that no other buffers/variables compete for the same cache lines.
EA_RTD_00092	The integrator shall allocate a single EcucPartition per core or the partition in which the Gpt is allocated shall be exclusively mapped to a core. Note↩ : Internally, the Gpt will use the Core ID returned by GetCoreID API to reference the appropriate global data and configuration elements, that is why a core should reference only one configured partition.
EA_RTD_00093	The application shall define EcucCoreIDs in a compact/consecutive order, starting from zero.
EA_RTD_00094	When multicore support is enabled, the application shall call Gpt_Init() for each core, using the dedicated configuration pointer for that core.
EA_RTD_00096	The application shall pass the correct initialization pointer, specific to the partition in which the driver is to be used.
EA_RTD_00106	Standalone IP configuration and HL configuration of the same driver shall be done in the same project
EA_RTD_00107	The integrator shall use the IP interface only for hardware resources that were configured for standalone IP usage. Note:The integrator shall not directly use the IP interface for hardware resources that were allocated to be used in HL context.
EA_RTD_00108	The integrator shall use the IP interface to a build a CDD, therefore the BSWMD will not contain reference to the IP interface

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