IAM-20685

Automotive 6-axis MotionTracking® MEMS Device for ADAS and Autonomous Driving Applications

GENERAL DESCRIPTION

The IAM-20685 is a 6-axis MotionTracking device that combines a 3-axis gyroscope and a 3-axis accelerometer in a small plastic package with wettable flanks option. By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, TDK InvenSense has driven the package size down to a footprint and thickness of 4.5x4.5x1.1 mm^3 (24-pin DQFN), to offer fully integrated, high performance component in a compact form factor.

The IAM-20685 features:

- Six independent mechanical structures
- Gyroscope with programmable full scale range from ±41 dps to ±1966 dps
- Accelerometer with programmable full-scale range from ±2g, to ±65g
- Minimal cross-axis sensitivity between the accelerometer and gyroscope axes
- 10,000 g shock tolerant structure
- Two temperature sensors
- 10 MHz, 32-bits Serial Peripheral Interface (SPI) with CRC-based error-detecting code algorithm
- ISO26262 ASIL B
- Automotive-qualified
- Reliability testing performed according to Automotive Electronics Council AEC – Q100 grade 2 (-40°C to 105°C) qualification requirements
- Final test at three temperatures: -40°C, 25°C, 105°C

IAM-20685 includes on-chip 16-bit ADCs, programmable digital filters, and embedded seft-test. The device features a VDD operating range of 3.0V to 5.5V, a separate digital IO supply, VDDIO, from 3.0V to 5.5V, and a current consumption below 10 mA in all the operating conditions.

The IAM-20685 has been developed according to ISO-26262 to address systems with automotive safety integrity level ASIL-B. Fault detection over lifetime is achieved by a set of embedded safety mechanisms (SMs) executed either in at startup, upon command, or in a continuous manner.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE	PACKAGE	MSL*
IAM-20685†	–40°C to +105°C	24-Pin DQFN	3

†Denotes RoHS and Green-compliant package

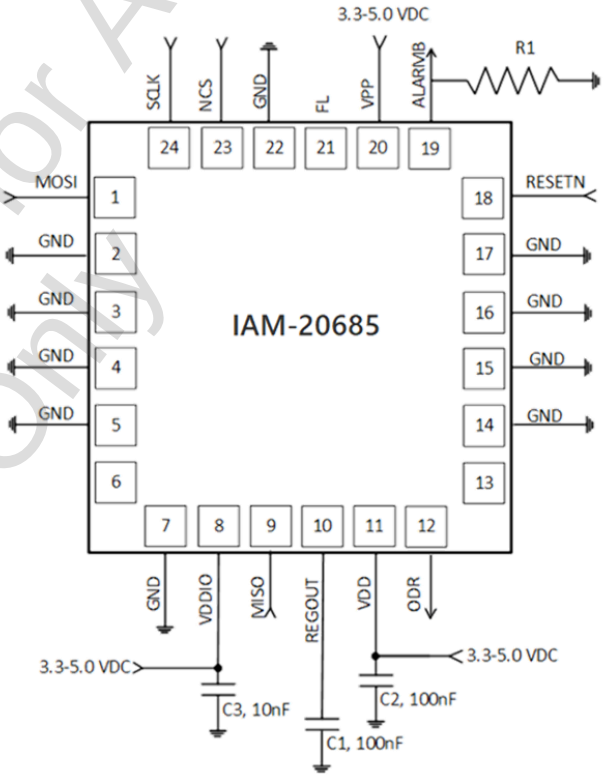
* Moisture sensitivity level of the package

APPLICATIONS

IAM-20685 addresses a wide range of Automotive applications, including but not limited to:

- Navigation
- Telematics and V2X
- Autonomous Driving
- Automated parking
- ADAS
- Dead Reckoning
- High precise positioning
- Vision system image stabilization

TYPICAL OPERATING CIRCUIT



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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing description, specifications, and design-related information on the IAM-20685 MotionTracking® device. The device is housed in a small 4.5x4.5x1.1 mm 24-pin DQFN package.

For what is concerned Functional Safety, this datasheet is intended to be used in conjunction with safety manual DS-000342.

1.2 PRODUCT OVERVIEW

The IAM-20685 is a 6-axis MotionTracking device that combines a 3-axis gyroscope and a 3-axis accelerometer in a small 4.5x4.5x1.1 mm (24-pin DQFN) package. The IAM-20685, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance.

The gyroscope has user-programmable full-scale range with a guaranteed accuracy up to ±300 dps. The accelerometer has a user-programmable accelerometer full-scale range of ±2*g*, to ±65*g* with accuracy guaranteed to up to ±36*g*. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, and embedded temperature sensors. The device features an SPI serial interface, a VDD operating range of 3.0V to 5.5V, and a separate digital IO supply, VDDIO, from 3.0V to 5.5V. Communication with all registers of the device is performed by using the SPI at 10 MHz

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates Micro Electro-Mechanical Systems (MEMS) wafers with companion CMOS electronics through wafer-level bonding, TDK has driven the package size down to a footprint and thickness of 4.5x4.5x1.1 mm (24-pin DQFN), to provide a very small yet high-performance low-cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.3 APPLICATIONS

- Autonomous Driving
- Advanced Driver Assistance Systems (ADAS)
- Navigation
- Telematics
- Dead Reckoning

1.4 FEATURES

- Low accelerometer and gyroscope offset
- On-Chip 16-bit ADCs and Programmable Filters
- Output Data-ready for synchronous sensor data readings
- Digital-output temperature sensors
- VDD operating range of 3.0 V to 5.5 V
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant
- Automotive-qualified
- Reliability testing performed according AEC – Q100 grade 2 (-40°C to 105°C) qualification requirements
- ISO-26262 ASIL level B

2 FEATURES

2.1 GYROSCOPE FEATURES

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a programmable full-scale range from ±41 dps to ±1966 dps and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full-scale range from ±2*g* to ±65*g* and integrated 16-bit ADCs
- Self-test

2.3 ADDITIONAL FEATURES

- Smallest and thinnest package in the industry: 24-pin DQFN 4.5x4.5x1.1 mm
- Minimal cross-axis sensitivity between the accelerometer and gyroscope axes
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope and accelerometer
- 10,000*g* shock tolerant
- 10 MHz SPI interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level

3 TARGET ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 3.3V, VDDIO = 3.3V, T_A=25°C, Gyroscope Full scale = ±655.36 dps, all specifications include board soldering effect unless otherwise noted.

NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	GUARANTEED[1,2,3,4]
02-002	Guaranteed measurement range		±300			dps	Design
02-003	Mechanical headroom		±2000			dps	Design
02-004	Electrical headroom		±2000			dps	Design
	Full Scale	See Table 22					
02-005	Sensitivity	gyro_fs_sel=0001		50		LSB/dps	Design
02-006	Resolution			0.02		dps	Design
02-008	Sensitivity error RT	25 ˚C	-1.0		1.0	%	Final test and characterization
02-009	Sensitivity variation over temperature	-40˚C to 105°C	-1.0		1.0	%	Final test and characterization
02-010	Sensitivity variation over life	Lifetime	-1.0		1.0	%	Qualification
02-014	Offset output RT	25˚C	-1.5		1.5	dps	Final test and characterization
02-015	Offset output variation over Temperature	-40˚C to 105°C	-1.0		1.0	dps	Final test and characterization
02-016	Offset output variation over life	Lifetime	-1.5		1.5	dps	Qualification
02-023	Output RMS noise	60 Hz Filter		0.045	0.1	dps rms	Characterization
02-023A	Noise Density[5]			5		mdps/√Hz	Characterization
02-024	Cross-axis sensitivity		-1.7		1.7	%	Characterization
02-025	Linearity	Maximum deviation from the straight line	-0.33		0.33	%FS	Characterization
02-030	Hysteresis	Maximum difference between two measurements for one temperature value: 25°C→ 105°C→25°C→-40°C→ 25°C			±0.5	dps	Characterization
02-031	g-sensitivity				±0.2	dps	Characterization
02-032	Device element resonant frequency		20.3			kHz	Final test
02-033	Mechanical gain due to resonance effects	Above 1.2 kHz at frequencies other than the element driven frequency, in any axis			3	dB	Design
02-036	Vibration Sensitivity	±8g, X and Y axes at drive frequency f_d[6]			±10	dps	Characterization
02-037		±8g, Z axis at drive frequency f_d[7]			±20		
02-038		±8g, all axes, all other frequencies between 50 Hz and 50 kHz[8]			±2		

Table 1. Gyroscope Specifications

Note:

1. Characterization means derived from validation or characterization of parts, not guaranteed in production.
2. Final test and characterization means tested in production at socket level, board soldering effect estimated from characterization of parts
3. Design means guaranteed by design, not tested in production.
4. Qualification means guaranteed by the qualification process, not tested in production. Lifetime effect estimated from qualification (HTOL)
5. Derived from RMS noise, 60 Hz filter
6. Nominal Gyroscope X f_d is 28 kHz, Nominal Gyroscope Y f_d is 26 kHz
7. Nominal Gyroscope Z f_d is 30 kHz
8. Vibrations at ±8g applied from 46 kHz to 50 kHz generates gyroscope saturation on Z axis

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 3.3V, VDDIO = 3.3V, T_A=25°C, accelerometer full scale = ±16.384g, all specifications include board soldering effect unless otherwise noted.

NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	GUARANTEED[1,2,3,4]
03-002	Guaranteed Measurement Range		±36			g	Design
03-003	Mechanical headroom	All axes	±115			g	Design
03-004	Electrical headroom	All axes	±115			g	Design
	Full Scale	See Table 23					
03-006	Sensitivity	Full scale ± 16.384*g*		2000		LSB/g	Design
03-007	Sensitivity	Full scale ±32.768*g*		1000		LSB/g	Design
03-007A	Sensitivity	Full Scale ±64.536*g*		500		LSB/g	Design
03-008	Resolution	Full scale ± 16.384*g*		0.5		mg	Design
03-009	Resolution	Full scale ±32.768*g*		1.0		mg	Design
03-009A	Resolution	Full Scale ±64.536*g*		2.0		mg	Design
03-011	Sensitivity error RT	25˚C, X and Y axes	-0.5		0.5	%	Final test and characterization
		25˚C, Z axis	-1.5		1.5		
03-012	Sensitivity variation over temperature	-40˚C to 105°C	-1.5		1.5	%	Final test and characterization
03-013	Sensitivity variation over life	lifetime, X and Y axes	-1.0		1.0	%	Characterization/qualification
		lifetime, Z axis	-2.0		2.0		
03-017	Zero offset code	0G		0000h		-	Design
03-019	Offset error at RT	25˚C, X and Y axes	-40		40	mg	Final test and characterization
		25˚C, Z axis	-86		86		
03-020	Offset variation over temperature	-40˚C to 105°C, X and Y axes	-30		30	mg	Final test and characterization
		-40˚C to 105°C, Z axis	-68		68		
03-021	Offset variation over life	Lifetime, X and Y axes	-35		35	mg	Characterization/qualification
		Lifetime, Z axis	-70		70		
03-029	Output noise	60 Hz filter			4.0	mg rms	Final test
03-031	Cross-axis sensitivity		-1.7		1.7	%	Characterization
03-032	Linearity	Maximum deviation from the straight line	-1.7		1.7	%FS	Characterization
03-036	Hysteresis	Maximum difference between two measurements for one temperature value: 25°C→ 105°C→25°C→-40°C→ 25°C			±15	mg	Characterization

Table 2. Accelerometer Specifications

Notes:

1. Characterization means derived from validation or characterization of parts, not guaranteed in production.
2. Final test and characterization mean tested in production at socket level, board soldering effect estimated from characterization of parts
3. Design means guaranteed by design, not tested in production.
4. Qualification means guaranteed by the qualification process, not tested in production. Lifetime effect estimated from qualification (HTOL)

3.3 TEMPERATURE SENSOR 1 SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 3.3V, VDDIO = 3.3V, T_A=25°C, unless otherwise noted.

NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT	GUARANTEED[1,2]
04-004	Total offset error	Including all variations (over life, temperature, supply, etc.)	-10		10	°C	Final test and qualification
04-005	Sensitivity			20		LSB/°C	Characterization
04-006	Total Sensitivity error	Including all variations (over life, temperature, supply, etc.)	-5.0		5.0	%	Characterization
04-007	Linearity	-40˚C to 105°C	-2.0		2.0	%	Characterization
04-009	Hysteresis	25°C(60°C)→+105°C→25°C(60°C)→ -40°C→25°C(60°C)			±5	°C	Characterization

Table 3. Temperature sensor 1 specifications

Notes:

1. Characterization means derived from validation or characterization of parts, not guaranteed in production
2. Final test and qualification mean tested in production at socket level, lifetime effect estimated from qualification (HTOL)

3.4 ELECTRICAL SPECIFICATIONS

3.4.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 3.3V, VDDIO = 3.3V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD	3.3V supply range	3.0	3.3	3.6	V	1
	5.0V supply range	4.5	5.0	5.5	V	1
VDDIO	3.3V supply range	3.0	3.3	3.6	V	1
	5.0V supply range	4.5	5.0	5.5	V	1
VPP	Connect to VDDIO	VDDIO-0.3		VDDIO+0.3	V	1
SUPPLY CURRENTS & BOOT TIME						
Normal Mode	6-axis Gyroscope + Accelerometer			10	mA	1
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+105	°C	1

Table 4. D.C. Electrical Characteristics

Notes:

1. Based on simulation and characterization of parts.

3.4.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 3.3V, VDDIO = 3.3V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time (T_{RAMP})	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		100	ms	1
POWER-ON RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01		100	ms	1
Start-up time for register read/write	From power-up			200	ms	1
DIGITAL INPUTS (MOSI, NCS, SCLK, RESETN)						
V_{IH}, High-Level Input Voltage		0.55*VDDIO		VDDIO+0.3	V	1

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
V_{IL}, Low-Level Input Voltage		-0.3		0.3*VDDIO	V	
C_I, Input Capacitance				15	pF	
DIGITAL OUTPUT (MISO)						
V_{OH}, High- Level Output Voltage	Iout=-1 mA	DVDD-0.5		VDD+0.3	V	1
V_{OL1}, Low-Level Output Voltage	Iout=1 mA			0.5	V	
OUTPUT DATA-READY (ODR)						
VOH, High- Level Output Voltage	Iout=-1 mA	DVDD-0.5		VDD+0.3	V	1
VOL1, Low-Level Output Voltage	Iout=1 mA			0.5	V	

Table 5. A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

3.4.3 Other Electrical Specifications

Typical Operating Circuit of section 4.2, VDD = 3.3V, VDDIO = 3.3V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SPI Operating Frequency, All Registers Read/Write			10000		kHz	1
Internal sampling rate		8,000			Samples/s	1, 2

Table 6. Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. If output data are acquired at a frequency different than the effective actual data rate, a suitable sampling rate conversion processing should be applied by the receiver to prevent data corruption by aliasing/images

3.5 SPI TIMING CHARACTERIZATION

NO.	PARAMETER	MIN	MAX	DESCRIPTION
	f_{SPI}		10 MHz	SCLK Frequency
1	t_{high}	35 ns		Time high: duration of SCLK logical high level
2	t_{low}	35 ns		Time low: duration of SCLK logical low level
3	t_{SUCS}	35 ns		CSB setup time: time between the CSB falling edge and SCLK rising edge
4	t_{d1}		52 ns	Time between CSB falling edge to valid data on MISO with 100 pF capacitance at MISO
5	t_{susi}	12 ns		MOSI setup time (with respect to an SCLK rising edge)
6	t_{d2}	0 ns	52 ns	Time between SCLK falling edge to valid data on MISO with 100 pF capacitance at MISO
7	t_{ncs}	20 ns		CSB hold time (SCLK falling edge to CSB rising edge)
8	t_{ri}		44 ns	Time between CSB rising edge to MISO tri-state with 200 pF capacitance at MISO
9	t_{ihics}	35 ns		Minimum time that CSB must stay high between two consecutive transfers
10	t_{ckrh}	10 ns		SCLK hold time after CSB becomes high
11	t_{ckfh}	5 ns		SCLK hold time after CSB becomes low
12	t_{cks}		4 ns	SCLK rise time
13	t_{ckf}		4 ns	SCLK fall time
14	t_{hsi}	12 ns		MOSI hold time before an SCLK falling edge

Table 7. SPI timing definitions

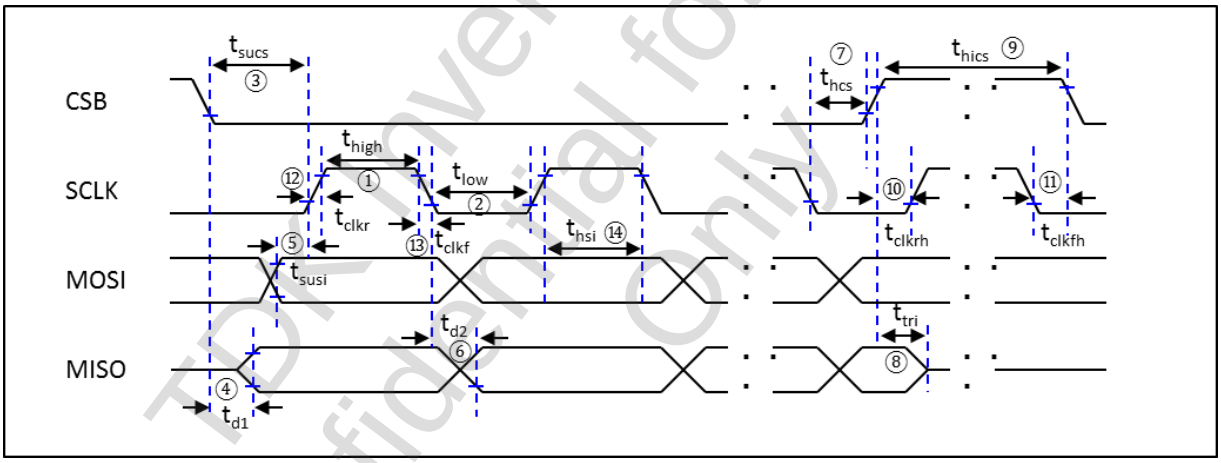

Figure 1. SPI bus timing diagram

3.6 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING
Supply Voltage, VDD	-0.3V to 6.5V
Supply Voltage, VDDIO	-0.3V to 6.5V
Input Voltage Level (MOSI, CSB, SCLK)	-0.5V to VDDIO + 0.5V
Acceleration (Any Axis, unpowered)	10,000*g* for 0.2 ms
Constant vibration (amplitude and frequency)	200 g, 43kHz[1]
Operating Temperature Range	-40°C to 105°C
Storage Temperature Range	-40°C to 155°C
Electrostatic Discharge (ESD) Protection Human Body Model (HBM)	2 kV
ESD Protection HBM (GND/Power Pins)	4 kV
ESD Protection Charged Device Model (CDM)	500V
ESD Protection CDM (Corner Pins)	750V
Latch-up at 105°C	±200 mA
Ultrasonic excitation (cleaning/welding/…)	Not allowed

Table 8. Absolute Maximum Ratings

Note:

1. Details for frequency higher than 43 kHz provided upon request.

4 APPLICATIONS INFORMATION

4.1 PINOUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	MOSI	Connect to host SPI MOSI pin
7	GND	Ground pin
8	VDDIO	VDDIO rail (3.3V or 5V)
9	MISO	Connect to host SPI MISO pin
10	REGOUT	Connect to ground through a 100 nF capacitor
11	VDD	Connect to 5V or 3.3V supply voltage and decouple with a 100 nF capacitor
12	ODR	Output Data-ready for synchronous sensor data readings (optional), leave floating when not used
18	RESETN	Connect to host reset signal (active low) or to VDDIO
19	ALARMB	Connect to host alarm monitoring pin
20	VPP	Connect to VDDIO
23	NCS	Connect to host CS pin
24	SCLK	Connect to host SPI SCLK pin
6, 13, 21	FL	Leave floating
2, 3, 4, 5, 14, 15, 16, 17, 22	GND	Connect to ground

Table 9. Pin Descriptions

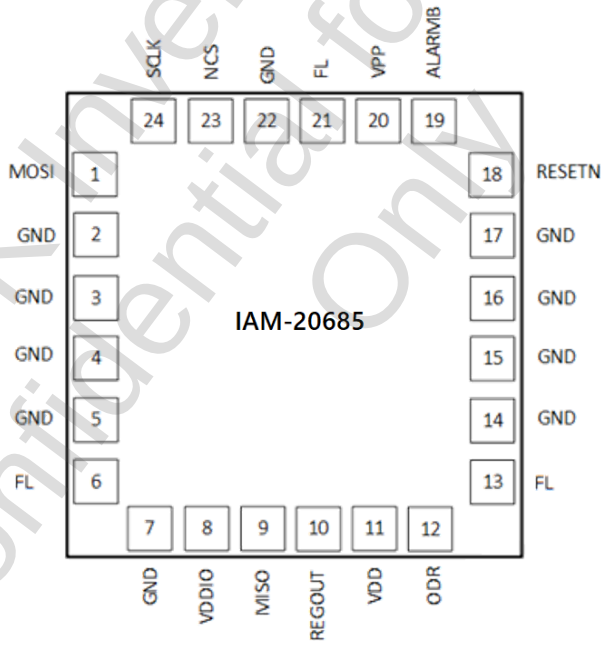

Figure 2. Top View – DQFN package 24-pin 4.5 mm x 4.5 mm

4.2 TYPICAL OPERATING CIRCUIT

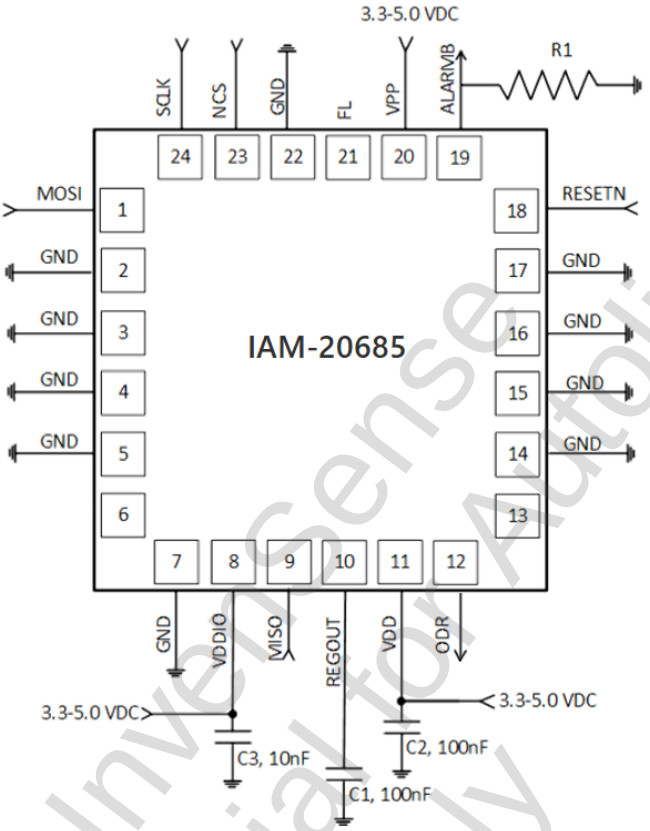

Figure 3. Application Schematic

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
REGOUT Capacitor	C1	X7R, 100 nF ±10%	1
VDD Bypass Capacitors	C2	X7R, 100 nF ±10%	1
VDDIO Bypass Capacitor	C3	X7R, 10 nF ±10%	1
ALARMB Pull-down Resistor	R1	47 kΩ ± 10%	1

Table 10. Bill of Materials

4.4 BLOCK DIAGRAM

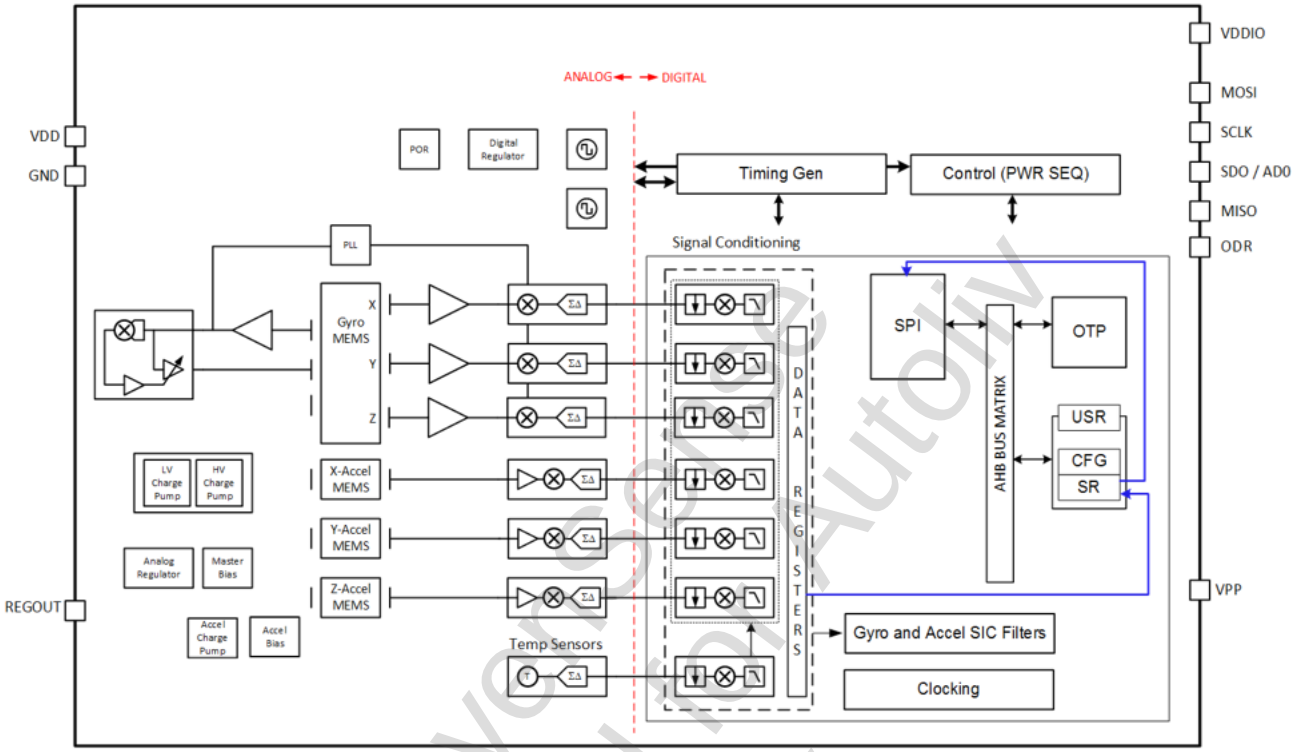

Figure 4. IAM-20685 Block Diagram

4.5 OVERVIEW

The IAM-20685 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Digital-output temperature sensors
- SPI serial communications interface
- Self-test
- Clocking
- Sensor Data Registers
- Bias circuit, regulators, charge pumps, and supplies
- Startup circuitry
- Signal conditioning and digital low-pass filters

4.6 SIGNAL CONDITIONING AND FILTERING

The capacitive output of the MEMS gyroscopes and accelerometers is converted into a digital representation by six sigma-delta analog-to-digital converters (ADCs – one converter per MEMS structure). Also, the output of each temperature sensor is converted into a digital value by a sigma-delta ADC. A bandgap structure provides the reference voltage to each ADC. The output of the ADCs is then fed to a gain offset settings (GOS) block that applies all the compensations and calibrations. The output of the GOS block is fed to digital low-pass filters (see sections 7.7 and 7.8). The output of the filters is available in the output registers (see sections 7.1 to Low Resolution Accelerometer 7.5).

4.7 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The IAM-20685 consists of three independent vibratory MEMS rate one-axis gyroscopes which detect the rotation around the X, Y, and Z axes. When the gyroscopes are rotated around any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit ADCs to sample each axis. A digital signal processor (DSP) processes the ADC output signals and reports the result into the gyroscope output registers. The gyroscopes are driven by dedicated drive circuits. The ADC sample rate is 8,000 samples per second (gyroscope, accelerometer, and temperature data will all be sampled within a sample period). User-selectable filters enable a wide range of cut-off frequencies.

4.7.1 Gyroscope Output

The registers gyro_x_data[15:0], gyro_y_data[15:0], and gyro_z_data[15:0] contain the gyroscope data for the x, y, and z axis respectively. The registers are encoded in 2's complement and the equation to convert the digital output into the corresponding angular rotation rate is:

$$\omega_x = \frac{gyro\_x\_data}{2^{15}} * FS, \omega_y = \frac{gyro\_y\_data}{2^{15}} * FS, \omega_z = \frac{gyro\_z\_data}{2^{15}} * FS,$$

Where $\omega_x, \omega_y, \omega_z$ are the angular rates of rotation (expressed in dps) of the axes x, y, and z, respectively and FS is the full-scale value of the axis. For instance, if gyro_x_data[15:0] contains 0x0A17 (Decimal 2583) and gyro_fs_sel[3:0]=1 (±655dps), the angular rate of the x axis is 2583*$(655.36\ dps)/2^{15}$= 51.63 dps.

4.8 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The IAM-20685's 3-axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass and capacitive sensors detect the displacement differentially. The IAM-20685's architecture reduces the accelerometers' susceptibility to manufacturing variations as well as to thermal drift. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. A DSP processes the signals at the output of the ADCs and reports the result into the accelerometer output registers. The IAM-20685 provides two accelerometer outputs per axis: a high-resolution output and a low-resolution output. The two outputs only differ for the full-scale setting (and, hence, for the resolution). The full-scale range of the high-resolution output is always smaller than the full-scale range of the low-resolution output.

Vrefshield is a voltage used to bias fixed shield structures surrounding accelerometer movable structures and protect them from electrical disturbances that may affect stability. VrefShieldXY is used for x-axis and y-axis accelerometers, while VrefShieldZ is used for z-axis accelerometer.

The full-scale range of the digital outputs can be adjusted setting the register accel_fs_sel[2:0] (see sections 7.3 and 7.5).

4.8.1 Accelerometers Output

The registers accel_x_data[15:0], accel_y_data[15:0], and accel_z_data[15:0] contain the accelerometer data for the axes x, y, and z respectively. The registers accel_x_data_lr[15:0], accel_y_data_lr[15:0], and accel_z_data[15:0] contain the low-resolution accelerometer data for the axes x, y, and z respectively. The low-resolution registers are designated with the suffix "lr". The registers are encoded in 2's complement and the equation to convert the digital output into the corresponding acceleration is:

$$a_x = \frac{accel\_x\_data}{2^{15}} * FS, a_y = \frac{accel\_y\_data}{2^{15}} * FS\ a_z = \frac{accel\_z\_data}{2^{15}} * FS,$$

$$a_{lrx} = \frac{accel\_x\_data\_lr}{2^{15}} * FS_{lr}, a_{lry} = \frac{accel\_y\_data\_lr}{2^{15}} * FS_{lr}, a_{lrz} = \frac{accel\_z\_data\_lr}{2^{15}} * FS_{lr},$$

Where a_x, a_y, a_z, a_{lrx}, a_{lry}, and a_{lrz} are the high-resolution and low-resolution accelerations of the axes x, y, and z, respectively and FS and FS_{lr} the full-scale range of the accelerometers high-resolution and low-resolution output. Table 23 shows the relationship between accel_fs_sel and the full-scale ranges.

For instance, if accel_x_data[15:0] contains 0x0A17 (Decimal 2583) and accel_fs_sel[2:0] is 001 (±16.384 g), the acceleration of the x axis is 2583*$(16.384\ g)/2^{15}$= 1.291g.

4.9 TEMPERATURE SENSORS

The IAM-20685 contains two temperature sensors called temp1 and temp2. Temperature sensor temp1 is used by all temperature-related calculations, while temp2 is used to check the correct operation of temp1. The output of the two temperature sensors is available in the registers temp1_data[15:0] and temp2_data[15:0], respectively. The equation to convert the digital output into the corresponding temperature (expressed in degrees Celsius) is:

$$TEMPERATURE\ (°C) = 25\ + \frac{\text{temp\_data}}{20}$$

where temp_data indicates either temp1_data[15:0] or temp2_data[15:0].

4.10 SERIAL COMMUNICATIONS INTERFACE

The IAM-20685 communicates with a system processor using a SPI interface. The IAM-20685 always acts as a slave when communicating to the system processor.

The system processor is an SPI master to the IAM-20685. Pins 1, 9, 23, 24 are used to support the MOSI, MISO, NCS, and SCLK signals for SPI communications. See section 5 for more information on the communication interface.

SPI readings are driven by SCLK that is asynchronous respect to internal sensor data rate (8kHz). When required it's possible to synchronize SPI readings with internal ODR clock.

4.11 SPI READINGS SYNCHRONOUS WITH INTERNAL ODR

Pin 12 (ODR) can be programmed to generate a copy of internal output data rate, allowing the synchronization of SPI readings respect to internal sensor data generation. Once programmed the ODR clock on pin 12, SPI readings shall be executed following timing shown in the following diagram:

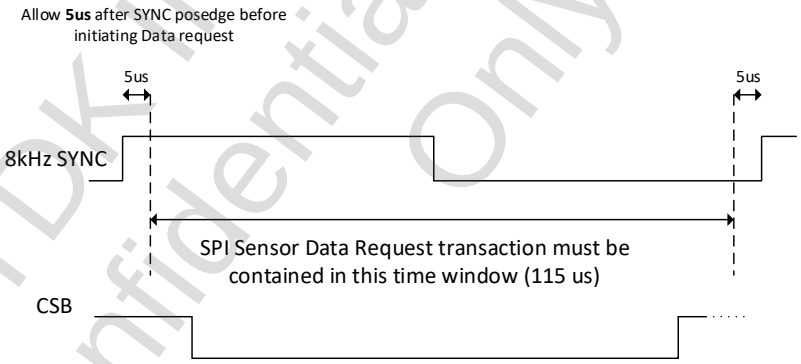

Figure 5: SPI synchronization with ODR

IAM-20685 implements a security feature to prevent unwanted register change, below procedure must be applied in order to unlock the ODR feature:

- 32-bit HEX word command must be sent over SPI: 0xE4000288
- 32-bit HEX word command must be sent over SPI: 0xE400018B
- 32-bit HEX word command must be sent over SPI: 0xE400048E
- 32-bit HEX word command must be sent over SPI: 0xE40300AD
- 32-bit HEX word command must be sent over SPI: 0xE4018017
- 32-bit HEX word command must be sent over SPI: 0xE4028030

Once the procedure above has been completed the ODR clock can be routed on Pin 12 following below procedure:

- Set BANK3, register address 0x14, bit 9 to 1b
- Set BANK3, register address 0x17, bit 12 to 1b
- Set BANK3, register address 0x11, bits 13:8 to 0x21
- Set BANK3, register address 0x13, bits 7:4 to 0x08
- Set BANK3, register address 0x14, bit 5 to 1b
- Set BANK3, register address 0x16, bit 0 to 1b

Please note that all the other bits that are contained into the same registers must be considered reserved and changing them might cause unwanted effects. To avoid unwanted behavior of the chip, before writing into a 16 -bit register, read the whole 16-bit register first and compute the new register value by changing the desired bits only.

4.12 SELF-TEST

The IAM-20685 includes a number of self-tests that help ISO-26262 compliance. Please see section 6 for more information. The self-tests are controlled by a safety controller.

4.13 CLOCKING

The IAM-20685 system is normally clocked by a phase locked loop (PLL). At start-up, until the PLL is stable, the IAM-20685 is clocked by an internal RC relaxation oscillator (RCOSC1). The IAM-20685 also has a second redundant RC oscillator (RCOSC2) that is used to check the operation of RCOSC1.

Each accelerometer and gyroscope has its own separate PLL.

4.14 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers and are accessed via the serial interface. Data from these registers may be read at any time. See sections 7.1 to 7.5 for details.

4.15 BIAS, REGULATORS, REFERENCES, CHARGE PUMPS, AND SUPPLIES

The bias and LDO block generates the internal supply and the reference voltages and currents required by the IAM-20685. The IAM-20685 is powered externally by two 3.3V to 5V (nominal) supplies, VDD and VPP, and by an input/output supply VDDIO that powers the communications output driver and determines the voltage levels of the SPI interface.

The IAM-20685 contains a number of regulators that, along with the charge pump, generate the required internal voltages, including the 2.4V master regulator, the 1.8V analog supply, AVDD, and the 1.8V digital supply, DVDD. The regulators and charge pumps contain a series of voltage references, each of which includes one or more bandgaps.

On-chip charge pumps generate the voltages required for the MEMS element.

4.16 INTERNAL BUSES

The IAM-20685 has internal direct memory access (DMA) and Advanced Microcontroller Bus Architecture (AMBA) High Performance (AHB) buses that route the signals between the registers and other internal blocks.

5 DIGITAL INTERFACE

The IAM-20685 uses a Serial Peripheral Interface to communicate with the host processor.

5.1 SERIAL INTERFACE PIN DESCRIPTIONS

The internal registers and memory of the IAM-20685 can be accessed using a SPI interface at 10 MHz. SPI operates in four-wire mode.

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	MOSI	Master Output Slave Input
9	MISO	Master Input Slave Output
23	NCS	Chip Select
24	SCLK	Serial Clock

Table 11. Serial Interface Pins Description

5.1.1 SPI Interface Operation

SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines. The IAM-20685 always operates as a slave device during standard master-slave SPI operation.

With respect to the master, MOSI, MISO, and SCLK are shared among the slave devices. Each SPI slave device requires its own Chip Select (NCS) line from the master.

NCS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one chip select line is active at any given time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their MISO lines to remain in a high-impedance (high-Z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data are delivered MSB first and LSB last
2. Data are latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 10 MHz

SPI read and write operations are completed in 32 clock cycles.

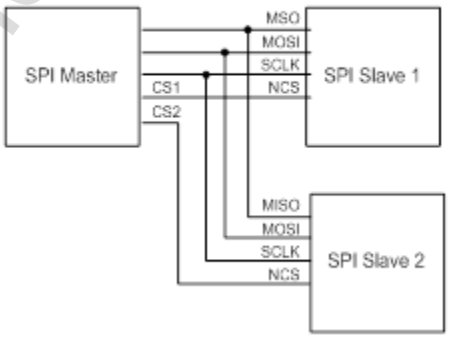

Figure 6. Typical SPI Master/Slave Configuration

5.2 PROTOCOL

The protocol is a 32-bit communication protocol. The bits are arranged according to the order shown in Figure 7.

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	···	b8	b7	···	b0
	Offset						Return status		Data				CRC		
MOSI	RW	A4	A3	A2	A1	A0	0	0	D15	D14	···	D0	CR7	···	CR0
MISO	RW	A4	A3	A2	A1	A0	RS1	RS0	D15	D14	···	D0	CR7	···	CR0

Figure 7. Protocol syntax

Each SPI command allows to read or write a register in the currently selected bank. Bank 0 is selected by default. To change bank, the host controller must first unlock bank_select (see section 7.18) using the tcode_status sequence shown in section 7.16.

Bit 31 determines whether the command is a register read (0) or a register write (1). Bits [30:26] represent the offset with respect to the bank that is currently selected. Please note that offsets 0x00 to 0x07 contain gyroscope, accelerometer, and sensors output data in all banks (see sections 7.1, 7.2, 7.3, and 7.4).

The meaning of the status bits is shown in Figure 8.

RS1	RS0	Definition
0	0	Reserved
0	1	Successful Register & OTP read/write
1	0	Register & OTP read/write in progress (data not prepared). Sensor output reading while Self test running
1	1	Error

Figure 8. Status bits

When communicating through SPI, data integrity is checked using an error-detecting code algorithm similar to the classic CRC, with 0xFF seed value. Please note that the resulting code is inverted before being appended to the command. For instance, when sending 0xD07A65, the inverted code is 0x88 and the host controller should send 0xD07A6588.
Input_data is the 24-bit word to be encoded, shifted serially, most significant bit first.

```
# encoding algorithm
CRC=0xFF
CRC_New=0x00
For i=23 to 0 {
 CRC_New[7]=CRC[6]
 CRC_New[6]=CRC[5]
 CRC_New[5]=CRC[4]
 CRC_New[4]=CRC[3] ^CRC[7]
 CRC_New[3]=CRC[2] ^CRC[7]
 CRC_New[2]=CRC[1] ^CRC[7]
 CRC_New[1]=CRC[0]
 CRC_New[0]=Input_data[i]^CRC[7]
 CRC=CRC_New
}

# final invertion before appending
For i=0 to 7 {
 CRC[i] = CRC[i]^1
}
```

The symbol ^ indicates the XOR operator.

For example, the CRC of 0xA0CA85 is 2F and the CRC of 0x3B007C is C2.

6 FUNCTIONAL SAFETY (ISO26262) FEATURES

The IAM-20685 has been developed according to ISO-26262 with an automotive safety integrity level ASIL-B.

Refer to safety manual DS-000342 for the further necessary details regarding Fault handling time detection and IAM-20685 integration into final system.

Fault detection over lifetime is achieved by a set of safety mechanisms (SMs) executed either in at startup, upon command, or in a continuous manner. The typical target detection time is <=0.75 ms.

The safety mechanisms are listed in Table 12.

SM #	SM NAME
3	SM03 – Clocks Check
4	SM04 – Gyroscopes Quadrature Check
7	SM07 – Gyroscopes Drive Signal Integrity Check
8	SM08 – Temperature Check
9	SM09 – Reset Check
10	SM10 – Master Regulator Check
11	SM11 – Analog VDD Regulator Check
12	SM12 – Digital VDD Regulator Check
13	SM13 – External Regulators Check
14	SM14 – Voltage References Check
16	SM16 – Accelerometers Self Test
17	SM17 – Shield Voltage Reference Check
18	SM18 – Accelerometer Drive Voltage Check
22	SM22 – Data Integrity Check
26	SM26 – Correct Register Loading From OTP Check
29	SM29 – AHB Matrix Check
30	SM30 – SPI Integrity Check
33	SM33 – Continuous Register Check
34	SM34 – Bandgaps Check
36	SM36 – Gyroscope DC Self Test
101	SM101 – Host SPI Check

Table 12. List of Safety Mechanisms

Each safety mechanism can trigger one or more alarms. An alarm is a bit in the register space (see sections 7.10, 0, and 7.12). Each alarm will in turn trigger the pin ALARMB, unless it is masked by its corresponding mask bit (see section 7.20). The pin ALARMB can also be masked by using msk_alarmpin (see section 7.20). Many alarms can be latched by their corresponding latch enable bits (see section 0). When an alarm is latched, the corresponding alarm register will only clear when read, even if the alarm signal ceases to be active.

Some safety mechanisms run all the time, while others run only at startup and/or upon command by the host. HostSPICheck is executed by the host micro-controller. Safety mechanisms can be enabled and disabled by their corresponding enable bits (see section 7.19).

Please note that when enabling/disabling and masking/unmasking safety mechanisms, before writing a bit into the enable and mask registers (sections 7.19 and 7.20), to preserve the chip configuration, the register must be read and only the desired bits must be changed, while all other bits must be left at the existing value.

6.1 SM03 – CLOCKS CHECK

SM03 checks that the frequencies of the following clock signals are within a certain tolerance of each other: system clock, x-axis PLL drive, y-axis PLL drive, z-axis PLL drive, RC oscillator 1, and RC oscillator 2. All clocks whose frequency is deemed incorrect will raise an alarm:

- sys_clk_alarm will be raised if the system clock is too slow or too fast with respect to the fastest clock

- gyro_x_drfreqmeas_alarm will be raised if the PLL driving the x-axis gyroscope is too slow or too fast with respect to the fastest clock
- gyro_y_drfreqmeas_alarm will be raised if the PLL driving the y axis gyroscope is too slow or too fast with respect to the fastest clock
- gyro_z_drfreqmeas_alarm will be raised if the PLL driving the z axis gyroscope is too slow or too fast with respect to the fastest clock
- rcosc1_freqmeas_alarm if the RC oscillator 1 is too slow or too fast with respect to the fastest clock
- rcosc2_freqmeas_alarm if the RC oscillator 2 is too slow or too fast with respect to the fastest clock

See section 7.10 for more details on the six alarms. The mask, enable, and latch bits are described in Table 13.

ALARM	MASK BIT	LATCH	ENABLE
sys_clk_alarm	msk_sys_clk_alarm	le_gyro_drfreqmeas_alarm	en_drivefreq_meas_sm
gyro_x_drfreqmeas_alarm	msk_gyro_x_drfreqmeas_alarm		
gyro_y_drfreqmeas_alarm	msk_gyro_y_drfreqmeas_alarm		
gyro_z_drfreqmeas_alarm	msk_gyro_z_drfreqmeas_alarm		
rcosc1_freqmeas_alarm	msk_rcosc1_freqmeas_alarm		
rcosc2_freqmeas_alarm	msk_rcosc2_freqmeas_alarm		

Table 13. SM03 Alarm Configuration Bits

The alarms can be masked by writing a 1 in the respective mask registers. The alarms can be latched by writing a 1 in the corresponding latch enable registers. This safety mechanism is enabled by default and can be disabled by writing a 0 into the enable register.

6.2 SM04 – GYROSCOPES QUADRATURE CHECK

SM04 ensures that the quadrature signals of the gyroscopes are within certain limits.

See section 7.10 for more information on the alarms. The mask, enable, and latch bits are described in Table 14.

ALARM	MASK BIT	LATCH	ENABLE
gyro_x_quadadc_alarm	msk_gyro_x_quadadc_alarm	le_gyro_quadadc_alarm	en_gyro_quad_adc_sm
gyro_y_quadadc_alarm	msk_gyro_y_quadadc_alarm		
gyro_z_quadadc_alarm	msk_gyro_z_quadadc_alarm		

Table 14. SM04 Alarm Configuration Bits

The alarms can be masked by writing a 1 in the respective mask registers. The alarms can be latched by writing a 1 in the corresponding latch enable registers. The safety mechanism is enabled by default and can be disabled by writing a 0 into the enable register.

Before enabling the safety mechanism, please mask its alarm bits by setting their corresponding mask bits. Unmask only after 5 ms to avoid false alarms.

6.3 SM07 – GYROSCOPES DRIVE SIGNAL INTEGRITY CHECK

The gyroscope drive clock is compared with the PLL feedback clock for phase alignment. The two clocks must be in phase. If any of the clocks of the x, y, and/or z gyroscopes are out of phase by more than 180 degrees with respect to the PLL feedback clock for two or more clock cycles gyro_x_drclk_alarm, gyro_y_drclk_alarm, and/or gyro_z_drclk_alarm will be issued.

The safety mechanism alarms, latch, enable, and mask configuration bits are described in Table 15.

AXIS	ALARM	ENABLE	MASK	LATCH
X gyroscope	gyro_x_drclk_alarm	Always enabled	msk_gyro_x_drclk_alarm	le_gyro_drclk_alarm
Y gyroscope	gyro_y_drclk_alarm		msk_gyro_y_drclk_alarm	
Z gyroscope	gyro_z_drclk_alarm		msk_gyro_z_drclk_alarm	

Table 15. SM07 Configuration Bits

6.4 SM08 – TEMPERATURE CHECK

SM08 checks temperature sensor 1. SM08 triggers temp_dsp_alarm if the temperature is too high or too low.

SM08 also triggers temp12_alarm if the difference in temperature reported by the two sensors is too high.

The alarms temp_dsp_alarm and temp12_alarm can be disabled by setting en_temp_sensecheck_sm to 0.

The alarms temp_dsp_alarm and temp12_alarm can be masked by setting msk_temp_dsp_alarm and msk_temp12_alarm to 1.

The alarms temp_dsp_alarm and temp12_alarm can be latched by setting le_temp_dsp_alarm to 1.

6.5 SM09 – RESET CHECK

When the IAM-20685 is in soft reset, hard reset, or power-on-reset the pin ALARMB raises an alarm. This safety mechanism cannot be latched or disabled, nor can it be masked.

6.6 SM10 – MASTER REGULATOR CHECK

SM10 checks that the 2.4V master regulator still outputs the correct voltage. If the voltage of the regulator is incorrect vddmaster_alarm is set to 1.

SM10 can be masked by msk_vddmaster_alarm, enabled by en_vddmaster_sm, and latched by le_vddmaster_alarm.

6.7 SM11 – ANALOG VDD REGULATOR CHECK

SM11 checks that the 1.8V analog regulator still outputs the correct voltage. If the voltage of the regulator is incorrect avddreg_alarm is set to 1.

SM11 can be masked by msk_avddreg_alarm, enabled by en_avdd_sm, and latched by le_avddreg_alarm.

6.8 SM12 – DIGITAL VDD REGULATOR CHECK

SM12 checks that the 1.8V digital regulator still outputs the correct voltage. If the voltage of the regulator is incorrect dvddreg_alarm is set to 1.

SM12 can be masked by msk_dvddreg_alarm, enabled by en_dvdd_sm, and latched by le_dvddreg_alarm.

6.9 SM13 – EXTERNAL REGULATORS CHECK

SM13 checks that the external digital regulator and the external power supply still supply the correct voltage at pins VDD and VDDIO.

If the external regulator voltage is incorrect vdd_alarm is set to 1.

If the VDDIO power supply voltage is incorrect vddio_alarm is set to 1.

SM 13 is enabled by setting en_vdd_sm to 1. The alarm vdd_alarm is masked by msk_vdd_alarm and is latched by le_vdd_alarm. The alarm vddio_alarm is masked by msk_vddio_alarm and is latched by le_vddio_alarm.

6.10 SM14 – VOLTAGE REFERENCES CHECK

SM14 ensures that the gyroscope, temperature sensors, accelerometer, and charge pump voltage references are within an acceptable range. Specifically:

- If the gyroscope voltage reference is incorrect gyro_vref_alarm is set to 1
- If the accelerometer voltage reference is incorrect accel_vref_alarm is set to 1
- If the temperature sensor 1 voltage reference is incorrect temp_vref_alarm is set to 1
- If the charge pump voltage reference is incorrect cp_vref_alarm is set to 1

BLOCK	ALARM	ENABLE	MASK	LATCH
Gyroscopes	gyro_vref_alarm	en_vref_sm	msk_gyro_vref_alarm	le_vref_alarm
Accelerometers	accel_vref_alarm		msk_accel_vref_alarm	
Temperature Sensor	temp_vref_alarm		msk_temp_vref_alarm	
Charge Pump	cp_vref_alarm		msk_cp_vref_alarm	

Table 16. SM14 Configuration Bits

SM14's alarm, mask, enable, and latch bits are reported in Table 16.

6.11 SM16 – ACCELEROMETERS SELF TEST

SM16 checks the proper operation of the accelerometers by applying a set of electrostatic forces to movable structures through dedicated electrodes.

The safety mechanism alarms, enable, and mask configuration bits are described in the table below.

AXIS	ALARM	ENABLE	MASK
X accelerometer	accel_x_dcst_alarm	en_accel_dcst_sm	msk_accel_x_dcst_alarm
Y accelerometer	accel_y_dcst_alarm		msk_accel_y_dcst_alarm
Z accelerometer	accel_z_dcst_alarm		msk_accel_z_dcst_alarm

Table 17. SM16 Alarms and Configuration Registers

The self-test can also be activated manually by setting the register accel_dc_trigger. In this case, the self-test will be executed with a stimulus equivalent to a variation of -3g or +3g, depending upon the setting of accel_dc_trigger. A response to ±4g (±0.5g for accel_fs_sel[2:0]>3) can also be simulated through the "dummy" self-test by setting the register accel_dummy_dc_trigger. In this case, the alarms are not activated. The dummy self-test can be used to generate a known signal at the output of the IAM-20685 to test the rest of the system.

6.12 SM17 – SHIELD VOLTAGE REFERENCE CHECK

SM17 ensures that the shield voltage references are within an acceptable range. Specifically:

- If the shieldxy voltage reference is incorrect vrefshieldxy_alarm is set to 1
- If the shieldz voltage reference is incorrect vrefshieldz_alarm is set to 1

SM17 is enabled by setting en_vrefshield_sm to 1. The alarm vrefshieldxy_alarm is masked by msk_vrefshieldxy_alarm and latched by le_vrefshieldxy_alarm. The alarm vrefshieldz_alarm is masked by msk_vrefshieldz_alarm and latched by le_vrefshieldz_alarm.

6.13 SM18 – ACCELEROMETER DRIVE VOLTAGE CHECK

SM18 ensures that the drive voltage of the accelerometer is within an acceptable range. If the voltage is incorrect accel_cp_alarm is set to 1.

SM18 is enabled by setting en_accel_cp_sm. The alarm accel_cp_alarm is masked by msk_accel_cp_alarm and latched by le_accel_cp_alarm.

6.14 SM22 – DATA INTEGRITY CHECK

SPI, AHB transfers, and all the register banks are protected by a single error correction and double error detection error correcting code (SECDED ECC). SM22 checks the data integrity each time a register is accessed or an AHB transfer takes place.

When the AHB is used, its SECDED bits are examined. If there is a single bit correction, ahb_eccdone_warn is set to 1. If two or more errors are detected, ahb_eccerr_alarm is set to 1.

6.15 SM26 – CORRECT REGISTER LOADING FROM OTP CHECK

SM26 ensures that the registers are correctly loaded from the internal one time programmable memory (OTP) by comparing the CRC stored in the OTP to the CRC computed when reading the registers and by comparing the value of the registers after loading to the value stored in the OTP.

If the CRC check fails otp_crc_alarm is set to 1. The alarm is masked by msk_otp_crc_alarm.

If the loading takes too long otp_cpy_alarm is set to 1. The alarm is masked by msk_otp_cpy_alarm.

If the check after loading fails, otp_reg_alarm is set to 1. The alarm is masked by msk_otp_reg_alarm.

The test can be started at any given time by setting otpreg_check_trigger to 1. However, if otpreg_check_trigger is already 1, it must first be set to 0.

Please note that register read/write access through SPI is not possible during this test (maximum execution time is 1 ms). It is advised to wait for the completion of the self-test startup sequence (200 ms) before performing register read/writes.

SM26 is not executed when monitor_st bit is set to 1 in RESET CONTROL register.

6.16 SM29 – AHB MATRIX CHECK

SM29 ensures that address and data are correctly transferred across the AHB matrix. If data and address at the input and output of the AHB matrix do not match, ahb_bus_alarm is set to 1. The alarm is masked by msk_ahb_bus_alarm.

SM29 is enabled by setting en_ahbbus_sm to 1.

Please note that register read/write access through SPI is not possible during this test (maximum execution time is 1 ms). It is advised to wait for the completion of the self-test startup sequence (200 ms) before performing register read/writes.

6.17 SM30 – SPI INTEGRITY CHECK

SM30 checks the integrity of the SPI logic by counting the number of transitions in the commands and by checking each frame with a redundant encoding and decoding logic.

Within each SPI frame, if the number of transitions in a SPI command is incorrect, spi_clkcnt_alarm is set to 1. The alarm is masked by msk_spi_clkcnt_alarm and latched by le_spi_clkcnt_alarm.

If the number of transitions is correct but the command CRC bits do not match the command, the spi_crc_alarm is set to 1. This alarm is masked by msk_spi_crc_alarm and latched by le_spi_crc_alarm.

Otherwise, if an error is detected in the decoded frame (compared to redundant encode/decode logic), spi_cmddecod_alarm is set to 1. The alarm is masked by msk_spi_cmddecod_alarm and latched by le_spi_cmddecod_alarm.

6.18 SM33 – CONTINUOUS REGISTER CHECK

SM33 checks the integrity of the registers content by examining their SECDED ECC bits periodically. If there is a single bit correction, reg_eccdone_warn is set to 1. If there are two or more errors, reg_eccerr_alarm is set to 1. Regcheck_alarm is masked by msk_regcheck_alarm.

SM33 is enabled by setting en_regcheck_sm to 1.

6.19 SM34 – BANDGAPS CHECK

SM34 checks whether or not the main bandgap, the analog/digital regulator bandgap, or the master regulator bandgap fall below predetermined voltages. If any of the bandgaps outputs a voltage that is lower than expected, bg_alarm is set to 1; bg_alarm is masked by msk_bg_alarm and latched by le_bg_alarm.

SM34 is enabled by setting en_bg_sm to 1.

6.20 SM36 – GYROSCOPE DC SELF TEST

SM36 checks the proper operation of the gyroscopes by applying a set of electrostatic forces to movable structures through dedicated electrodes.

The safety mechanism alarms, enable, and mask configuration bits are described in Table 18.

AXIS	ALARM	ENABLE	MASK
X gyroscope	gyro_x_dcst_alarm	en_gyro_dcst_sm	msk_gyro_x_dcst_alarm
Y gyroscope	gyro_y_dcst_alarm		msk_gyro_y_dcst_alarm
Z gyroscope	gyro_z_dcst_alarm		msk_gyro_z_dcst_alarm

Table 18. SM36 Alarms and Configuration Registers

The self-test can also be activated manually by setting the register gyro_dc_trigger. In this case, the self-test will be executed with a stimulus equivalent to -110dps or +110dps), depending upon the setting of gyro_dc_trigger. The dummy self-test injects ±50 LSB (±12.5 dps for gyro_fs_sel [3:0]>7) in front of the digital low pass filters. In this case, the alarms are not activated. The dummy self-test can be used to generate a known signal at the output of the IAM-20685 to test the rest of the system.

6.21 SM101 – HOST SPI CHECK

The Host System has an active role to fully achieve Functional Safety, it's expected to implement some specific tasks.

Register_Write_Lock bit (BANK0 Addr=0x16 bit 19) shall be set as last action of sensor initialization, after start-up. As consequence of this action register bank switch is no more effective, therefore only BANK 0 is accessible afterwards. That means that Alarms shall be checked by reading registers:

- SUMMARY STATUS, BANK0, Addr 0Eh (i_s_ok_c , i_s_ok_a , i_s_ok_r)
- GYRO_ST_STATUS_1, BANK0, Addr 10h
- GYRO_ST_STATUS_2, BANK0, Addr 11h
- ACCEL_ST_STATUS_1, BANK0, Addr 12h
- ACCEL_ST_STATUS_2, BANK0, Addr 13h
- COMMON_ST_STATUS_1, BANK0, Addr 14h
- COMMON_ST_STATUS_2, BANK0, Addr 15h

For further details please refer to safety manual DS-000342.

7 REGISTER DESCRIPTIONS

This section describes the function and contents of each register within the IAM-20685. The registers are described in order of bank and, within each bank, in order of offset.

Please note that all register bits that are not documented are considered reserved and changing them might cause unwanted effects. To avoid unwanted behavior of the chip, before writing into a 16 -bit register, read the whole 16-bit register first and compute the new register value by changing the desired bits.

7.1 GYROSCOPE DATA

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	All	0x00	15:0	N/A	gyro_x_data[15:0]	Contains the gyroscope x axis data
R	All	0x01	15:0	N/A	gyro_y_data[15:0]	Contains the gyroscope y axis data
R	All	0x02	15:0	N/A	gyro_z_data[15:0]	Contains the gyroscope z axis data

The registers gyro_x_data[15:0], gyro_y_data[15:0], and gyro_z_data[15:0] contain the gyroscope data for the axes x, y, and z respectively. The registers are encoded in 2's complement. Refer to section 4.7.1 for details on how to convert the register output in degrees per second.

7.2 TEMPERATURE 1 DATA

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	All	0x03	15:0	N/A	temp1_data[15:0]	Contains the temperature sensor 1 data

The register temp1_data[15:0] contains the IC temperature data. The register is encoded in 2's complement. See section 4.9 for the equation to convert the digital output into the corresponding temperature (expressed in degrees Celsius).

7.3 ACCELEROMETER DATA

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	All	0x04	15:0	N/A	accel_x_data[15:0]	Contains the accelerometer x axis data
R	All	0x05	15:0	N/A	accel_y_data[15:0]	Contains the accelerometer y axis data
R	All	0x06	15:0	N/A	accel_z_data[15:0]	Contains the accelerometer z axis data

The registers accel_x_data, accel_y_data, and accel_z_data contain the accelerometer data for the axes x, y, and z respectively. The registers are encoded in 2's. Refer to section 4.8.1 for details on how to convert the register output in g.

7.4 TEMPERATURE 2 DATA

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	All	0x07	15:0	N/A	temp2_data[15:0]	Contains the temperature sensor 2 data

The register temp2_data[15:0] contains the temperature data for the redundant temperature. The register encoding and behavior matches that of temp1_data[15:0].

7.5 LOW RESOLUTION ACCELEROMETER DATA

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	0	0x08	15:0	N/A	accel_x_data_lr[15:0]	Contains the low-resolution accelerometer x axis data
R	0	0x09	15:0	N/A	accel_y_data_lr[15:0]	Contains the low-resolution accelerometer y axis data
R	0	0x0A	15:0	N/A	accel_z_data_lr[15:0]	Contains the low-resolution accelerometer z axis data

The registers accel_x_data_lr, accel_y_data_lr, and accel_z_data_lr contain the accelerometer data for the axes x, y, and z respectively. The register suffix LR stands for "low resolution" as its full scale is always equal or greater than that of the accelerometer data registers of section 7.3. The registers are encoded in 2's. Refer to section 4.8.1 for details on how to convert the register output in g.

7.6 FIXED VALUE

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	0	0x0B	15:0	0xAA55	fixed_value[15:0]	Fixed value 0xAA55

7.7 ACCELEROMETER AND GYROSCOPE Y AND Z FILTER SETTINGS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	0	0x0C	5:0	100000	flt_y[5:0]	Output filter setting for the gyroscope's and accelerometer's y axis.
RW	0	0x0C	11:6	100000	flt_z[5:0]	Output filter setting for the gyroscope's and accelerometer's z axis.

The registers flt_y and flt_z contain the settings for the filters in front of the gyroscope and accelerometer for axes y and z. The filters are set according to Table 19 and Table 20 (all settings not documented in the tables are reserved).

FLT_Z						CUT-OFF FREQUENCY [HZ]	
D11	D10	D9	D8	D7	D6	GYRO_Z	ACCEL_Z
0	0	0	0	0	1	10	10
0	0	0	0	1	0	10	46
0	0	0	0	1	1	10	60
0	0	0	1	0	0	10	250
0	0	0	1	0	1	10	300
0	0	0	1	1	0	10	400
0	0	0	1	1	1	12.5	10
0	0	1	0	0	0	12.5	46
0	0	1	0	0	1	12.5	60
0	0	1	0	1	0	12.5	250
0	0	1	0	1	1	12.5	300
0	0	1	1	0	0	12.5	400
0	0	1	1	0	1	27	10
0	0	1	1	1	0	27	46
0	0	1	1	1	1	27	60
0	1	0	0	0	0	10	10
0	1	0	0	0	1	10	60
0	1	0	0	1	0	60	10
0	1	0	0	1	1	27	250
0	1	0	1	0	0	27	300
0	1	0	1	0	1	27	400
0	1	0	1	1	0	30	10
0	1	0	1	1	1	30	46
0	1	1	0	0	0	30	60
0	1	1	0	0	1	30	250
0	1	1	0	1	0	30	300
0	1	1	0	1	1	30	400
0	1	1	1	0	0	46	10
0	1	1	1	0	1	46	46

FLT_Z						CUT-OFF FREQUENCY [HZ]	
0	1	1	1	1	0	46	60
0	1	1	1	1	1	46	250
1	0	0	0	0	0	60	60
1	0	0	0	0	1	10	60
1	0	0	0	1	0	60	10
1	0	0	0	1	1	46	300
1	0	0	1	0	0	46	400
1	0	0	1	0	1	60	10
1	0	0	1	1	0	60	46
1	0	0	1	1	1	60	60
1	0	1	0	0	0	60	250
1	0	1	0	0	1	60	300
1	0	1	0	1	0	60	400

Table 19. Z-axis Filter Configuration Parameters

FLT_Y						CUT-OFF FREQUENCY [HZ]	
D5	D4	D3	D2	D1	D0	GYRO_Y	ACCEL_Y
0	0	0	0	0	1	10	10
0	0	0	0	1	0	10	46
0	0	0	0	1	1	10	60
0	0	0	1	0	0	10	250
0	0	0	1	0	1	10	300
0	0	0	1	1	0	10	400
0	0	0	1	1	1	12.5	10
0	0	1	0	0	0	12.5	46
0	0	1	0	0	1	12.5	60
0	0	1	0	1	0	12.5	250
0	0	1	0	1	1	12.5	300
0	0	1	1	0	0	12.5	400
0	0	1	1	0	1	27	10
0	0	1	1	1	0	27	46
0	0	1	1	1	1	27	60
0	1	0	0	0	0	10	10
0	1	0	0	0	1	10	60
0	1	0	0	1	0	60	10
0	1	0	0	1	1	27	250
0	1	0	1	0	0	27	300
0	1	0	1	0	1	27	400
0	1	0	1	1	0	30	10
0	1	0	1	1	1	30	46
0	1	1	0	0	0	30	60

FLT_Y						CUT-OFF FREQUENCY [HZ]	
0	1	1	0	0	1	30	250
0	1	1	0	1	0	30	300
0	1	1	0	1	1	30	400
0	1	1	1	0	0	46	10
0	1	1	1	0	1	46	46
0	1	1	1	1	0	46	60
0	1	1	1	1	1	46	250
1	0	0	0	0	0	60	60
1	0	0	0	0	1	10	60
1	0	0	0	1	0	60	10
1	0	0	0	1	1	46	300
1	0	0	1	0	0	46	400
1	0	0	1	0	1	60	10
1	0	0	1	1	0	60	46
1	0	0	1	1	1	60	60
1	0	1	0	0	0	60	250
1	0	1	0	0	1	60	300
1	0	1	0	1	0	60	400

Table 20. Y-axis Filter Configuration Parameters

7.8 STATUS SUMMARY AND X-AXIS FILTER SETTINGS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	0	0x0E	14	0	selftestdis	If selftestdis is 1 all safety mechanisms except SM26 and SM29 are skipped during startup
RW	0	0x0E	13:8	100000	flt_x[5:0]	Output filter setting for the gyroscope's and accelerometer's x axis
R	0	0x0E	6	1	i_s_ok_c	Logic NOR of all the common status bits (see 7.12). 0: At least one alarm flag 1: No alarms
R	0	0x0E	3	1	i_s_ok_a	Logic NOR of all the accelerometer status bits (see 7.11). 0: At least one alarm flag 1: No alarms
R	0	0x0E	0	1	i_s_ok_r	Logic NOR of all the gyroscope status bits (see 7.10). 0: At least one alarm flag 1: No alarms

This register contains the summary of the status of the various status registers. It also contains a bit that disables all startup self-tests (except the OTP related ones, see table above for exact list). This register also allows to configure the filter of the x-axis accelerometer and gyroscope according to Table 21 (all settings not documented in the table are reserved).

FLT_X						CUT-OFF FREQUENCY [HZ]	
D13	D12	D11	D10	D9	D8	GYRO_X	ACCEL_X
0	0	0	0	0	1	10	10
0	0	0	0	1	0	10	46
0	0	0	0	1	1	10	60
0	0	0	1	0	0	10	250
0	0	0	1	0	1	10	300
0	0	0	1	1	0	10	400
0	0	0	1	1	1	12.5	10
0	0	1	0	0	0	12.5	46
0	0	1	0	0	1	12.5	60
0	0	1	0	1	0	12.5	250
0	0	1	0	1	1	12.5	300
0	0	1	1	0	0	12.5	400
0	0	1	1	0	1	27	10
0	0	1	1	1	0	27	46
0	0	1	1	1	1	27	60
0	1	0	0	0	0	10	10
0	1	0	0	0	1	10	60
0	1	0	0	1	0	60	10
0	1	0	0	1	1	27	250
0	1	0	1	0	0	27	300
0	1	0	1	0	1	27	400
0	1	0	1	1	0	30	10
0	1	0	1	1	1	30	46
0	1	1	0	0	0	30	60
0	1	1	0	0	1	30	250
0	1	1	0	1	0	30	300
0	1	1	0	1	1	30	400
0	1	1	1	0	0	46	10
0	1	1	1	0	1	46	46
0	1	1	1	1	0	46	60
0	1	1	1	1	1	46	250
1	0	0	0	0	0	60	60
1	0	0	0	0	1	10	60
1	0	0	0	1	0	60	10
1	0	0	0	1	1	46	300
1	0	0	1	0	0	46	400
1	0	0	1	0	1	60	10
1	0	0	1	1	0	60	46

FLT_X						CUT-OFF FREQUENCY [HZ]	
1	0	0	1	1	1	60	60
1	0	1	0	0	0	60	250
1	0	1	0	0	1	60	300
1	0	1	0	1	0	60	400

Table 21. X-axis Filter Configuration Parameters

7.9 TEMPERATURE SENSORS DIFFERENCE

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	0	0x0F	15:0	N/A	temp12_delta[15:0]	Signed delta(T) = (temp1_data - temp2_data) in 2's complement.

This register contains the difference between temp1_data[15:0] and temp2_data[15:0] in 2's complement. The register is encoded like temp1_data[15:0] and temp2_data[15:0].

7.10 GYROSCOPE ALARM REGISTERS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R/C	0	0x10	12	0	gyro_z_quadadc_alarm	A 1 indicates that the gyroscope quad signal amplitude for the z axis is incorrect (SM04).
R/C	0	0x10	11	0	gyro_y_quadadc_alarm	A 1 indicates that the gyroscope quad signal amplitude for the y axis is incorrect (SM04).
R/C	0	0x10	10	0	gyro_x_quadadc_alarm	A 1 indicates that the gyroscope quad signal amplitude for the x axis is (SM04).
R/C	0	0x10	8	0	gyro_z_drfreqmeas_alarm	A 1 indicates that the PLL drive frequency for the z axis is incorrect (SM03).
R/C	0	0x10	7	0	gyro_y_drfreqmeas_alarm	A 1 indicates that the PLL drive frequency for the y axis is incorrect (SM03).
R/C	0	0x10	6	0	gyro_x_drfreqmeas_alarm	A 1 indicates that the PLL drive frequency for the x axis is incorrect (SM03).
R/C	0	0x11	14	0	gyro_z_dcst_alarm	A 1 indicates that the z-axis check of SM36 failed
R/C	0	0x11	13	0	gyro_y_dcst_alarm	A 1 indicates that the y-axis check of SM36 failed
R/C	0	0x11	12	0	gyro_x_dcst_alarm	A 1 indicates that the x-axis check of SM36 failed
R/C	0	0x11	4	0	gyro_vref_alarm	A 1 indicates that the gyroscope's Vref is incorrect (SM14).
R/C	0	0x11	3	0	gyro_z_drclk_alarm	A 1 indicates that the z axis PLL lock condition is lost, setting off alarm for SM07
R/C	0	0x11	2	0	gyro_y_drclk_alarm	A 1 indicates that the y axis PLL lock condition is lost, setting off alarm for SM07
R/C	0	0x11	1	0	gyro_x_drclk_alarm	A 1 indicates that the x axis PLL lock condition is lost, setting off alarm for SM07

7.11 ACCELEROMETER ALARM REGISTERS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R/C	0	0x12	13	0	vrefshieldz_alarm	A 1 indicates that VrefShieldZ is incorrect (SM17).
R/C	0	0x12	12	0	vrefshieldxy_alarm	A 1 indicates that VrefhshieldXY is incorrect (SM17).
R/C	0	0x12	1	0	accel_cp_alarm	A 1 indicates that the accelerometer's drive voltage is incorrect (SM18).
R/C	0	0x12	0	0	accel_vref_alarm	A 1 indicates that the accelerometer's Vref is incorrect, setting off alarm for SM14
R/C	0	0x13	2	0	accel_x_dcst_alarm	A 1 indicates that the x-axis accelerometer check of SM16 failed
R/C	0	0x13	1	0	accel_y_dcst_alarm	A 1 indicates that the y-axis accelerometer check of SM16 failed
R/C	0	0x13	0	0	accel_z_dcst_alarm	A 1 indicates that the z-axis accelerometer check of SM16 failed

7.12 OTHER ALARMS REGISTERS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R/C	0	0x14	13	0	otp_crc_alarm	A 1 indicates that the expected OTP CRC does not match with the OTP content (SM26)
R/C	0	0x14	12	0	otp_reg_alarm	A 1 indicates that there is a mismatch between OTP content and the registers that were loaded from the OTP (SM26)
R/C	0	0x14	11	0	bg_alarm	A 1 indicates that a bandgap voltage is incorrect (SM34).
R/C	0	0x14	10	0	cp_vref_alarm	A 1 indicates that Vref of one or both charge pumps is incorrect (SM14).
R/C	0	0x14	9	0	temp_vref_alarm	A 1 indicates that Vref of temperature sensor is incorrect (SM14).
R/C	0	0x14	8	0	vdd_alarm	A 1 indicates that VDD is incorrect (SM13).
R/C	0	0x14	7	0	vddio_alarm	A 1 indicates that VDDIO is incorrect (SM13).
R/C	0	0x14	6	0	dvddreg_alarm	A 1 indicates that DVDD is incorrect (SM12).
R/C	0	0x14	5	0	avddreg_alarm	A 1 indicates that AVDD is incorrect (SM11).
R/C	0	0x14	4	0	vddmaster_alarm	A 1 indicates that master regulator is incorrect (SM10)
R/C	0	0x14	3	0	temp12_alarm	A 1 indicates that the difference of the temperature reported by the two temperature sensors is incorrect. This is used by SM08.
R/C	0	0x14	2	0	temp_dsp_alarm	A 1 indicates that the temperature reported by the temperature sensor temp1 is too low or too high (SM08).
R/C	0	0x14	1	0	rcosc2_freqmeas_alarm	A 1 indicates that the frequency of the RC oscillator 2 is incorrect (SM03)
R/C	0	0x14	0	0	rcosc1_freqmeas_alarm	A 1 indicates that the frequency of the RC oscillator 1 is incorrect (SM03)
R/C	0	0x15	13	0	sys_clk_alarm	A 1 indicates that the system clock frequency is incorrect (SM03).
R/C	0	0x15	12	0	otp_cpy_alarm	A 1 indicates that the SM26 OTP loading test took too long (i.e. it timed-out)
R/C	0	0x15	9	0	reg_eccdone_warn	A 1 indicates the correction of a 1 bit error in registers (SM22).
R/C	0	0x15	8	0	reg_eccerr_alarm	A 1 indicates the detection of a 2-bit or more error at hardware register data (SM22).
R/C	0	0x15	7	0	ahb_eccdone_warn	A 1 indicates the correction of a 1-bit error in the AHB bus (SM22).
R/C	0	0x15	6	0	ahb_eccerr_alarm	A 1 indicates the occurrence of a 1-bit error in AHB address or more than 2-bit error in the AHB bus (SM22).

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R/C	0	0x15	5	0	regcheck_alarm	A 1 indicates that one or more registers failed their integrity check (SM33).
R/C	0	0x15	4	0	spi_clkcnt_alarm	A 1 indicates that the SPI number of clock edges is not correct for SM30
R/C	0	0x15	3	0	spi_cmddecod_alarm	A 1 indicates an SPI redundant encode-decode mismatch for command response for SM30
R/C	0	0x15	2	0	spi_crc_alarm	A 1 indicates that the SPI CRC is not correct for SM30
R/C	0	0x15	1	0	ahb_bus_alarm	A 1 indicates that either the address bits or data bits on the bus matrix are not as expected (SM29)

7.13 SAFETY MECHANISMS MANUAL TRIGGERS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	0	0x16	10:9	00	gyro_dummy_dc_trigger[1:0]	Activates the dummy gyroscope DC self-test: 01: DC self-test positive (+50 dps) 10: DC self-test negative (-50 dps) 00, 11: no self-test The self-test will continue until the register is reset (00).
RW	0	0x16	8:7	00	gyro_dc_trigger[1:0]	Activates SM36 - gyroscope DC self-test 11: start self-test 01: DC self-test positive (110 dps) 10: DC self-test negative (-110 dps) 00: no self-test The register is not self-clearing. To execute the test again the register must be reset first. Please also note that 00 does not interrupt the current test.
RW	0	0x16	6:5	00	accel_dummy_dc_trigger[1:0]	Activates the digital portion of SM16 11: start self-test 01: dummy DC self-test positive +4g 10: dummy DC self-test negative -4g 00, 11: no self-test The self-test will continue until the register is reset (00).
RW	0	0x16	4:3	00	accel_dc_trigger[1:0]	Starts SM16: 11: start self-test 01: DC self-test positive 10: DC self-test negative 00: no self-test The register is not self-clearing. To execute the test again the register must be reset first. Please also note that 00 does not interrupt the current test.
RW	0	0x16	2	0	ahbmatrix_check_trigger	If the bit is 0, writing a 1 starts SM29. If the bit is already 1, writing a 1 or a 0 will not start the test. Do not set the bit to 1 if SM16 is being executed.
RW	0	0x16	1	0	otpreg_check_trigger	If the bit is 0, writing a 1 starts SM26. If the bit is already 1, writing a 1 or a 0 will not start the test. Do not set the bit to 1 if SM16 or SM29 is being executed.

7.14 TEST REGISTER

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	0	0x17	15:0	0x0000	test[15:0]	Register available to the host controller for any purpose

This register can be used by the host controller to store temporary data for any purpose.

7.15 RESET CONTROL

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
W/C	0	0x18	3	0	monitor_st	When "1" is written in this bit, the startup self-tests are executed again. The bit will self-clear after a cycle.
W/C	0	0x18	2	0	hard_reset	When "1" is written in hard_reset, a hardware reset is executed (power on reset, reset of register data, OTP load, execution of startup self-tests). Putting 0V on the pin RESETN for 30 ms or more will also trigger a hardware reset.
W/C	0	0x18	1	0	soft_reset	When "1" is written in soft_reset, a software reset is executed. The software reset will: Reset addresses 0x00 to 0x07 Reset bank_select[15:0], i.e. return to bank 0 Reset all bank 0 registers except fixed_value[15:0], test[15:0], gyro_id[3:0], accel_id[4:0], hw_config[4:0, hw_rev[4:0], id_code3[15:0], id_code4[15:0]. Load the OTP if en_soft_reset_otp_load is set to 1 Execute the startup self-tests

These registers allow the user to reset the IC or run the startup self-tests.

7.16 MODE REGISTERS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	0	0x19	15	0	register_write_lock	"Lock of register write" bit 0: Normal 1: Register write function is locked. -When register_write_lock is set, the register write function is locked (disabled). The read function is available. When register write command is sent, the response of MISO is 11b -The release of lock status is enabled only by POR (power down) and hardware reset.
RW	0	0x19	3	0	capture_mode	Writing a 1 in capture_mode stops the refresh of the output data registers (see sections 7.1 to 7.5). Writing a 0 resumes the refresh of the output data registers.
RW	0	0x19	2:0	111	tcode_status[2:0]	Writing the sequence "010→001→100" into tcode_status[2:0] enables writing into banks other than Bank 0 and into bank_select (0x1F, available in all banks). While writing the sequence, tcode_status will be changed to 010->011->111 (e.g. when 001 is written into tcode_status, tcode_status will change to 011). If, before unlocking the banks, any other sequence is written into tcode_status, the register will actually be changed to 000. Only a power-on-reset will lock the banks again.

7.17 ID REGISTERS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	0	0x1B	11:8	0x00	gyro_id[3:0]	Gyroscope revision
RW	0	0x1B	4:0	0x00	accel_id[4:0]	Accelerometer revision
R	0	0x1C	4:0	0x15	hw_rev[4:0]	Sensor hardware revision
RW	0	0x1D	15:0	0x0000	id_code3[15:0]	Reserved
RW	0	0x1E	15:0	0x0000	id_code4[15:0]	Reserved
R	1	0x0E	7:0	0xF2	whoami[7:0]	Unique identifier for IAM-20685

This register contains the revisions of the IC, gyroscope, accelerometer, as well as serial numbers.

7.18 BANK SELECTION

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	0	0x1F	15:0	0x0000	bank_select[15:0]	This register changes the selected bank. This register is normally read-only. To allow changing its contents (thereby selecting a different bank), the register tcode_status[2:0] must be written according to the procedure described in section 7.16. The register bank_select is accessible from all banks. Writing an invalid bank number will prevent from further writing into the register until the IC is reset

7.19 SAFETY MECHANISMS ENABLE REGISTERS

The default enable configuration for the embedded safety mechanisms is set during factory calibration, in line with the target automotive safety integrity level for the component and in accordance to the product qualification. Any change applied to any of the registers 0x11 and 0x12 may affect the embedded safety mechanisms functionality and could deteriorate the overall fault detection of the component. Any change on the registers 0x11 and 0x12 is under customer responsibility and TDK InvenSense is not responsible for any component malfunction derived from the change.

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	1	0x11	14	1	en_temp_sensecheck_sm	If set to 1, the bit enables the safety mechanism SM08
RW	1	0x11	13	1	en_accel_cp_sm	If set to 1, the bit enables the safety mechanism SM18 that monitors the charge pumps.
RW	1	0x11	12	1	en_vrefshield_sm	If set to 1, the bit enables the Vrefshield check safety mechanism, SM17.
RW	1	0x11	11	1	en_accel_dcst_sm	if set to 1, the bit enables the accelerometer DC self-test SM16.
RW	1	0x11	10	1	en_vref_sm	If set to 1, the bit enables the safety mechanism SM14 that monitors the reference voltages.
RW	1	0x11	9	1	en_vdd_sm	If set to 1, the bit enables the safety mechanism SM13 that monitors the regulator VDD.
RW	1	0x11	8	1	en_dvdd_sm	If set to 1, the bit enables the safety mechanism SM12 that monitors the digital regulator DVDD.
RW	1	0x11	7	1	en_avdd_sm	If set to 1, the bit enables the safety mechanism SM11 that monitors the analog regulator AVDD.
RW	1	0x11	6	1	en_vddmaster_sm	If set to 1, the bit enables the safety mechanism SM10 that monitors the 2.4V master regulator.
RW	1	0x11	4	1	en_gyro_quad_adc_sm	if set to 1, the bit enables the gyro quadrature ADC safety mechanism SM04.
RW	1	0x12	12	1	en_gyro_dcst_sm	If set to 1, the bit enables the safety mechanism SM36 (gyro DC self-test)
RW	1	0x12	8	1	en_drivefreq_meas_sm	if set to 1, the bit enables the system frequency check SM03.
RW	1	0x12	7	1	en_bg_sm	If set to 1, the bit enables the safety mechanism SM34 that monitors the bandgaps.

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	1	0x12	6	1	en_regcheck_sm	if set to 1, the bit enables the continuous register data check SM33.
RW	1	0x12	4	1	en_ahbbus_sm	if set to 1, the bit enables the AHB bus matrix master/slave ports check SM29

7.20 SAFETY MECHANISMS MASK REGISTERS

The default mask configuration for the embedded safety mechanisms is set during factory calibration, in line with the target automotive safety integrity level for the component and in accordance to the product qualification. Any change applied to any of the registers 0x13, 0x14, 0x15, 0x16 and 0x17 may affect the system capability to detect a failure. Any change on the registers 0x13, 0x14, 0x15, 0x16 and 0x17 is under customer responsibility and TDK InvenSense is not responsible for any component malfunction derived from the change.

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	1	0x13	13	0	msk_gyro_z_quadadc_alarm	Set to 1 prevents gyro_z_quadadc_alarm from triggering the pin ALARMB (SM04)
RW	1	0x13	12	0	msk_gyro_y_quadadc_alarm	Set to 1 prevents gyro_y_quadadc_alarm from triggering the pin ALARMB (SM04)
RW	1	0x13	11	0	msk_gyro_x_quadadc_alarm	Set to 1 prevents gyro_x_quadadc_alarm from triggering the pin ALARMB (SM04)
RW	1	0x13	10	0	msk_rcosc1_freqmeas_alarm	Set to 1 prevents rcosc1_freqmeas_alarm from triggering the pin ALARMB (SM03)
RW	1	0x13	9	0	msk_sys_clk_alarm	Set to 1 prevents sys_clk_alarm from triggering the pin ALARMB (SM03)
RW	1	0x13	8	0	msk_gyro_z_drfreqmeas_alarm	Set to 1 prevents gyro_z_drfreqmeas_alarm from triggering the pin ALARMB (SM03)
RW	1	0x13	7	0	msk_gyro_y_drfreqmeas_alarm	Set to 1 prevents gyro_y_drfreqmeas_alarm from triggering the pin ALARMB (SM03)
RW	1	0x13	6	0	msk_gyro_x_drfreqmeas_alarm	Set to 1 prevents gyro_x_drfreqmeas_alarm from triggering the pin ALARMB (SM03)
RW	1	0x14	12	0	msk_temp_vref_alarm	Set to 1 prevents temp_vref_alarm from triggering the pin ALARMB (SM14)
RW	1	0x14	11	0	msk_accel_vref_alarm	Set to 1 prevents accel_vref_alarm from triggering the pin ALARMB (SM14)
RW	1	0x14	10	0	msk_gyro_vref_alarm	Set to 1 prevents gyro_vref_alarm from triggering the pin ALARMB (SM14)
RW	1	0x14	9	0	msk_vdd_alarm	Set to 1 prevents vdd_alarm from triggering the pin ALARMB (SM13)
RW	1	0x14	8	0	msk_vddio_alarm	Set to 1 prevents vddio_alarm from triggering the pin ALARMB (SM13)
RW	1	0x14	7	0	msk_dvddreg_alarm	Set to 1 prevents dvddreg_alarm from triggering the pin ALARMB (SM12)
RW	1	0x14	6	0	msk_avddreg_alarm	Set to 1 prevents avddreg_alarm from triggering the pin ALARMB (SM11)
RW	1	0x14	5	0	msk_vddmaster_alarm	Set to 1 prevents vddmaster_alarm from triggering the pin ALARMB (SM10)
RW	1	0x14	4	0	msk_temp12_alarm	Set to 1 prevents temp12_alarm from triggering the pin ALARMB (SM08)
RW	1	0x14	3	0	msk_temp_dsp_alarm	Set to 1 prevents temp_dsp_alarm from triggering the pin ALARMB (SM08)
RW	1	0x14	2	0	msk_gyro_z_drclk_alarm	Set to 1 prevents gyro_z_drclk_alarm from triggering the pin ALARMB (SM07)

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	1	0x14	1	0	msk_gyro_y_drclk_alarm	Set to 1 prevents gyro_y_drclk_alarm from triggering the pin ALARMB (SM07)
RW	1	0x14	0	0	msk_gyro_x_drclk_alarm	Set to 1 prevents gyro_x_drclk_alarm from triggering the pin ALARMB (SM07)
RW	1	0x15	15	0	msk_cp_vref_alarm	Set to 1 prevents cp_vref_alarm from triggering the pin ALARMB (SM14)
RW	1	0x15	14	0	msk_ahb_bus_alarm	Set to 1 prevents ahb_bus_alarm from triggering the pin ALARMB (SM29)
RW	1	0x15	12	0	msk_otp_crc_alarm	Set to 1 prevents otp_crc_alarm from triggering the pin ALARMB (SM26)
RW	1	0x15	11	0	msk_otp_reg_alarm	Set to 1 prevents otp_reg_alarm from triggering the pin ALARMB (SM26)
RW	1	0x15	7	0	msk_reg_eccerr_alarm	Set to 1 prevents reg_eccerr_alarm from triggering the pin ALARMB (SM22)
RW	1	0x15	6	0	msk_ahb_eccerr_alarm	Set to 1 prevents ahb_eccerr_alarm from triggering the pin ALARMB (SM22)
RW	1	0x15	5	0	msk_otp_eccerr_alarm	Set to 1 prevents otp_eccerr_alarm from triggering the pin ALARMB (SM22)
RW	1	0x15	2	0	msk_accel_cp_alarm	Set to 1 prevents accel_cp_alarm from triggering the pin ALARMB (SM18)
RW	1	0x15	1	0	msk_vrefshieldz_alarm	Set to 1 prevents vrefshieldz_alarm from triggering the pin ALARMB (SM17)
RW	1	0x15	0	0	msk_vrefshieldxy_alarm	Set to 1 prevents vrefshieldxy_alarm from triggering the pin ALARMB (SM17)
RW	1	0x16	15	0	msk_gyro_z_dcst_alarm	Set to 1 prevents gyro_z_dcst_alarm (SM36) from triggering the pin ALARMB
RW	1	0x16	14	0	msk_gyro_y_dcst_alarm	Set to 1 prevents gyro_y_dcst_alarm (SM36) from triggering the pin ALARMB
RW	1	0x16	13	0	msk_gyro_x_dcst_alarm	Set to 1 prevents gyro_x_dcst_alarm (SM36) from triggering the pin ALARMB
RW	1	0x16	6	0	msk_rcosc2_freqmeas_alarm	Set to 1 prevents rcosc2_freqmeas_alarm from triggering the pin ALARMB (SM03)
RW	1	0x16	5	0	msk_bg_alarm	Set to 1 prevents bg_alarm from triggering the pin ALARMB (SM34)
RW	1	0x16	4	0	msk_regcheck_alarm	Set to 1 prevents regcheck_alarm from triggering the pin ALARMB (SM33)
RW	1	0x16	3	0	msk_otp_cpy_alarm	Set to 1 prevents otp_cpy_alarm (SM26) from triggering the pin ALARMB
RW	1	0x16	2	0	msk_spi_clkcnt_alarm	Set to 1 prevents spi_clkcnt_alarm from triggering the pin ALARMB (SM30)
RW	1	0x16	1	0	msk_spi_cmddecod_alarm	Set to 1 prevents spi_cmddecod_alarm from triggering the pin ALARMB (SM30)
RW	1	0x16	0	0	msk_spi_crc_alarm	Set to 1 prevents spi_crc_alarm from triggering the pin ALARMB (SM30)
RW	1	0x17	15	0	msk_alarmpin	Set to 1 prevents the alarms from triggering the pin ALARMB
RW	1	0x17	12	0	msk_accel_z_dcst_alarm	Set to 1 prevents accel_z_dcst_alarm (SM16) from triggering the pin ALARMB
RW	1	0x17	11	0	msk_accel_y_dcst_alarm	Set to 1 prevents accel_y_dcst_alarm (SM16) from triggering the pin ALARMB
RW	1	0x17	10	0	msk_accel_x_dcst_alarm	Set to 1 prevents accel_x_dcst_alarm (SM16) from triggering the pin ALARMB

7.21 SAFETY MECHANISMS LATCH ENABLE REGISTERS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	1	0x19	11	0	le_gyro_quadadc_alarm	Set to 1 latches gyro_x_quadadc_alarm, gyro_y_quadadc_alarm, and gyro_z_quadadc_alarm (SM04)
RW	1	0x19	9	0	le_spi_clkcnt_alarm	Set to 1 latches spi_clkcnt_alarm (SM30)
RW	1	0x19	8	0	le_spi_cmddecod_alarm	Set to 1 latches spi_cmddecod_alarm (SM30)
RW	1	0x19	7	0	le_spi_crc_alarm	Set to 1 latches spi_crc_alarm (SM30)
RW	1	0x19	6	0	le_gyro_drfreqmeas_alarm	Set to 1 latches gyro_x_drfreqmeas_alarm, gyro_y_drfreqmeas_alarm, and gyro_z_drfreqmeas_alarm (SM03)
RW	1	0x1A	15	0	le_vrefshieldz_alarm	Set to 1 latches vrefshieldz_alarm (SM17)
RW	1	0x1A	14	0	le_vrefshieldxy_alarm	Set to 1 latches vrefshieldxy_alarm (SM17)
RW	1	0x1A	11	0	le_bg_alarm	Set to 1 latches bg_alarm (SM34)
RW	1	0x1A	10	0	le_vref_alarm	Set to 1 latches cp_vref_alarm, gyro_vref_alarm, accel_vref_alarm, and temp_vref_alarm (SM14)
RW	1	0x1A	9	0	le_vdd_alarm	Set to 1 latches vdd_alarm (SM13)
RW	1	0x1A	8	0	le_vddio_alarm	Set to 1 latches vddio_alarm (SM13)
RW	1	0x1A	7	0	le_dvddreg_alarm	Set to 1 latches dvddreg_alarm (SM12)
RW	1	0x1A	6	0	le_avddreg_alarm	Set to 1 latches avddreg_alarm (SM11)
RW	1	0x1A	5	0	le_vddmaster_alarm	Set to 1 latches vddmaster_alarm (SM10)
RW	1	0x1A	3	0	le_temp_dsp_alarm	Set to 1 latches temp_dsp_alarm and temp12_alarm (SM08)
RW	1	0x1A	1	0	le_accel_cp_alarm	Set to 1 latches accel_cp_alarm (SM18)
RW	1	0x1A	0	0	le_gyro_drclk_alarm	Set to 1 latches gyro_x_drclk_alarm, gyro_y_drclk_alarm, and gyro_z_drclk_alarm (SM07)

7.22 SAFETY MECHANISMS STATUS

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	1	0x1C	15	0	gyro_x_axis_err	Logic OR of all safety mechanisms alarm flags that may affect the x-axis gyroscope operation, i.e., gyro_x_quadadc_alarm, gyro_z_drfreqmeas_alarm, gyro_y_drfreqmeas_alarm, gyro_x_drfreqmeas_alarm, gyro_x_drclk_alarm, otp_crc_alarm, otp_reg_alarm, bg_alarm, cp_vref_alarm, temp_vref_alarm, vdd_alarm, vddio_alarm, dvddreg_alarm, avddreg_alarm, vddmaster_alarm, temp12_alarm, temp_dsp_alarm, rcosc2_freqmeas_alarm, rcosc1_freqmeas_alarm, sys_clk_alarm, otp_cpy_alarm, otp_eccerr_alarm, reg_eccerr_alarm, ahb_eccerr_alarm, regcheck_alarm, spi_clkcnt_alarm, spi_cmddecod_alarm, spi_crc_alarm, ahb_bus_alarm.
R	1	0x1C	14	0	gyro_y_axis_err	Logic OR of all safety mechanisms alarm flags that may affect the y-axis gyroscope operation, i.e. gyro_y_quadadc_alarm, gyro_z_drfreqmeas_alarm, gyro_y_drfreqmeas_alarm, gyro_x_drfreqmeas_alarm, gyro_x_drclk_alarm, gyro_y_drclk_alarm, otp_crc_alarm, otp_reg_alarm, bg_alarm, cp_vref_alarm, temp_vref_alarm, vdd_alarm, vddio_alarm, dvddreg_alarm, avddreg_alarm, vddmaster_alarm, temp12_alarm, temp_dsp_alarm, rcosc2_freqmeas_alarm, rcosc1_freqmeas_alarm, sys_clk_alarm, otp_cpy_alarm, otp_eccerr_alarm, reg_eccerr_alarm, ahb_eccerr_alarm, regcheck_alarm, spi_clkcnt_alarm, spi_cmddecod_alarm, spi_crc_alarm, ahb_bus_alarm.

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	1	0x1C	13	0	gyro_z_axis_err	Logic OR of all safety mechanisms alarm flags that may affect the z-axis gyroscope operation, i.e. gyro_z_quadadc_alarm, gyro_z_drfreqmeas_alarm, gyro_y_drfreqmeas_alarm, gyro_x_drfreqmeas_alarm, gyro_x_drclk_alarm, gyro_z_drclk_alarm, otp_crc_alarm, otp_reg_alarm, bg_alarm, cp_vref_alarm, temp_vref_alarm, vdd_alarm, vddio_alarm, dvddreg_alarm, avddreg_alarm, vddmaster_alarm, temp12_alarm, temp_dsp_alarm, rcosc2_freqmeas_alarm, rcosc1_freqmeas_alarm, sys_clk_alarm, otp_cpy_alarm, otp_eccerr_alarm, reg_eccerr_alarm, ahb_eccerr_alarm, regcheck_alarm, spi_clkcnt_alarm, spi_cmddecod_alarm, spi_crc_alarm, ahb_bus_alarm.
R	1	0x1C	12	0	accel_x_axis_err	Logic OR of all safety mechanisms alarm flags that may affect the x-axis accelerometer operation, i.e. gyro_z_drfreqmeas_alarm, gyro_y_drfreqmeas_alarm, gyro_x_drfreqmeas_alarm, gyro_vref_alarm, gyro_x_drclk_alarm, vrefshieldxy_alarm, accel_cp_alarm, accel_vref_alarm, accel_x_dcst_alarm, otp_crc_alarm, otp_reg_alarm, bg_alarm, cp_vref_alarm, temp_vref_alarm, vdd_alarm, vddio_alarm, dvddreg_alarm, avddreg_alarm, vddmaster_alarm, temp12_alarm, temp_dsp_alarm, rcosc2_freqmeas_alarm, rcosc1_freqmeas_alarm, sys_clk_alarm, otp_cpy_alarm, otp_eccerr_alarm, reg_eccerr_alarm, ahb_eccerr_alarm, regcheck_alarm, spi_clkcnt_alarm, spi_cmddecod_alarm, spi_crc_alarm, ahb_bus_alarm.
R	1	0x1C	11	0	accel_y_axis_err	Logic OR of all safety mechanisms alarm flags that may affect the y-axis accelerometer operation, i.e. gyro_z_drfreqmeas_alarm, gyro_y_drfreqmeas_alarm, gyro_x_drfreqmeas_alarm, gyro_vref_alarm, gyro_x_drclk_alarm, vrefshieldxy_alarm, accel_cp_alarm, accel_vref_alarm, accel_y_dcst_alarm, otp_crc_alarm, otp_reg_alarm, bg_alarm, cp_vref_alarm, temp_vref_alarm, vdd_alarm, vddio_alarm, dvddreg_alarm, avddreg_alarm, vddmaster_alarm, temp12_alarm, temp_dsp_alarm, rcosc2_freqmeas_alarm, rcosc1_freqmeas_alarm, sys_clk_alarm, otp_cpy_alarm, otp_eccerr_alarm, reg_eccerr_alarm, ahb_eccerr_alarm, regcheck_alarm, spi_clkcnt_alarm, spi_cmddecod_alarm, spi_crc_alarm, ahb_bus_alarm.
R	1	0x1C	10	0	accel_z_axis_err	Logic OR of all safety mechanisms alarm flags that may affect the z-axis accelerometer operation, i.e. gyro_z_drfreqmeas_alarm, gyro_y_drfreqmeas_alarm, gyro_x_drfreqmeas_alarm, gyro_vref_alarm, gyro_x_drclk_alarm, vrefshieldz_alarm, accel_cp_alarm, accel_vref_alarm, accel_z_dcst_alarm, otp_crc_alarm, otp_reg_alarm, bg_alarm, cp_vref_alarm, temp_vref_alarm, vdd_alarm, vddio_alarm, dvddreg_alarm, avddreg_alarm, vddmaster_alarm, temp12_alarm, temp_dsp_alarm, rcosc2_freqmeas_alarm, rcosc1_freqmeas_alarm, sys_clk_alarm, otp_cpy_alarm, otp_eccerr_alarm, reg_eccerr_alarm, ahb_eccerr_alarm, regcheck_alarm, spi_clkcnt_alarm, spi_cmddecod_alarm, spi_crc_alarm, ahb_bus_alarm.

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
R	1	0x1C	9	0	temp1_err	Logic OR of all safety mechanisms alarm flags relative to the temperature sensor temp1 operation, i.e. gyro_z_drfreqmeas_alarm, gyro_y_drfreqmeas_alarm, gyro_x_drfreqmeas_alarm, otp_crc_alarm, otp_reg_alarm, bg_alarm, temp_vref_alarm, vdd_alarm, vddio_alarm, dvddreg_alarm, avddreg_alarm, vddmaster_alarm, temp12_alarm, temp_dsp_alarm, rcosc2_freqmeas_alarm, rcosc1_freqmeas_alarm, sys_clk_alarm, otp_cpy_alarm, otp_eccerr_alarm, reg_eccerr_alarm, ahb_eccerr_alarm, regcheck_alarm, spi_clkcnt_alarm, spi_cmddecod_alarm, spi_crc_alarm, ahb_bus_alarm.
R	1	0x1C	8	0	temp2_err	Logic OR of all safety mechanisms alarm flags relative to the temperature sensor temp2 operation. This is identical to temp1_err.
R	1	0x1C	4	0	sc_cont_tests_on	A 1 indicates that the IC is in normal mode, i.e. not performing any safety startup tests.
R	1	0x1C	3	0	error_flag_all_sm	Logic OR of all safety mechanism alarms.

These registers provide information on the status of various safety mechanisms and whether the IC is in normal status or not.

7.23 ODR CONFIGURATION

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	3	0x11	13:8	000000b	ODR_Config_1	ODR clock configuration
RW	3	0x13	7:4	0000b	ODR_Config_2	ODR clock configuration
RW	3	0x14	5	0b	ODR_Config_3	ODR clock configuration
RW	3	0x14	9	0b	ODR_Config_4	ODR clock configuration
RW	3	0x16	0	0b	ODR_Config_5	ODR clock configuration
RW	3	0x17	12	0b	ODR_Config_6	ODR clock configuration

7.24 SENSITIVITY CONFIGURATION

TYPE	BANK	OFFSET	BIT	DEFAULT	NAME	FUNCTION
RW	6	0x14	2:0	001	accel_fs_sel[2:0]	Determines the accelerometer full scale. See Table 23 for full scale options.
RW	7	0x14	3:0	0001	gyro_fs_sel[3:0]	Determines the gyroscope full scale. See Table 22 for full scale values.

GYRO_FS_SEL[3:0]	SENSITIVITY	FS
0000	100 LSB/dps	±328dps
0001	50 LSB/dps	±655 dps
0010	25 LSB/dps	±1311 dps
0011	16.67 LSB/dps	±1966 dps
0100	150 LSB/dps	±218 dps
0101	75 LSB/dps	±437 dps
0110	37.5 LSB/dps	±874 dps
0111	25 LSB/dps	±1311 dps
1000	533.34 LSB/dps	±61 dps
1001	266.67 LSB/dps	±123 dps
1010	133.33 LSB/dps	±246 dps
1011	66.67 LSB/dps	±492 dps
1100	800 LSB/dps	±41 dps
1101	400 LSB/dps	±82 dps
1110	200 LSB/dps	±164 dps
1111	100 LSB/dps	±328 dps

Table 22. Gyroscope full-scale range and sensitivity

ACCEL_FS_SEL[2:0]	FS	FS_{LR}
000	16.384g	32.768g
001	16.384g	65.536g
010	32.768g	32.768g
011	32.768g	65.536g
100	2.048g	4.096g
101	2.048g	16.384g
110	4.096g	4.096g
111	4.096g	8.192g

Table 23. Accelerometer full-scale range and sensitivity

IAM-20685 default full-scale settings are ±655 dps for gyroscope and ±16 g for accelerometer, these settings are applied during component's factory calibration in accordance to the configuration used for product qualification.

Specification numbers reported into Table 1 and Table 2 are guaranteed for default full-scale settings unless otherwise noted.

IAM-20685 implements a security feature to prevent unwanted full-scale change but gives to the users the flexibility to modify the default full scale following a dedicated unlock procedure.

Below procedure must be applied in order to unlock the full-scale change feature:

- 32-bit HEX word command must be sent over SPI: 0xE4000288
- 32-bit HEX word command must be sent over SPI: 0xE400018B
- 32-bit HEX word command must be sent over SPI: 0xE400048E
- 32-bit HEX word command must be sent over SPI: 0xE40300AD
- 32-bit HEX word command must be sent over SPI: 0xE4018017
- 32-bit HEX word command must be sent over SPI: 0xE4028030

Once the procedure above has been completed the new full-scale setting can be applied modifying the bits accel_fs_sel[2:0] into the register address 0x14 of bank 6, and gyro_fs_sel[3:0] into the register address 0x14 of bank 7.

Please note that all the other bits that are contained into the same registers have to be considered reserved and changing them might cause unwanted effects. To avoid unwanted behavior of the chip, before writing into a 16 -bit register, read the whole 16-bit register first and compute the new register value by changing the desired bits only.

8 ASSEMBLY

This section provides general guidelines for assembling TDK Micro Electro-Mechanical Systems (MEMS) gyroscopes and accelerometers packaged in DQFN package.

8.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

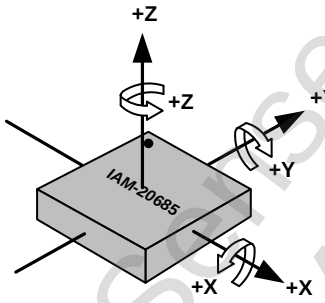

Figure 9. IAM-20685 Orientation of Axes and Polarity of Rotation

8.2 PACKAGE DIMENSIONS

The package top and side view are shown in Figure 10 while the bottom view is shown in Figure 11. The package dimensions and tolerances are shown in Table 24.

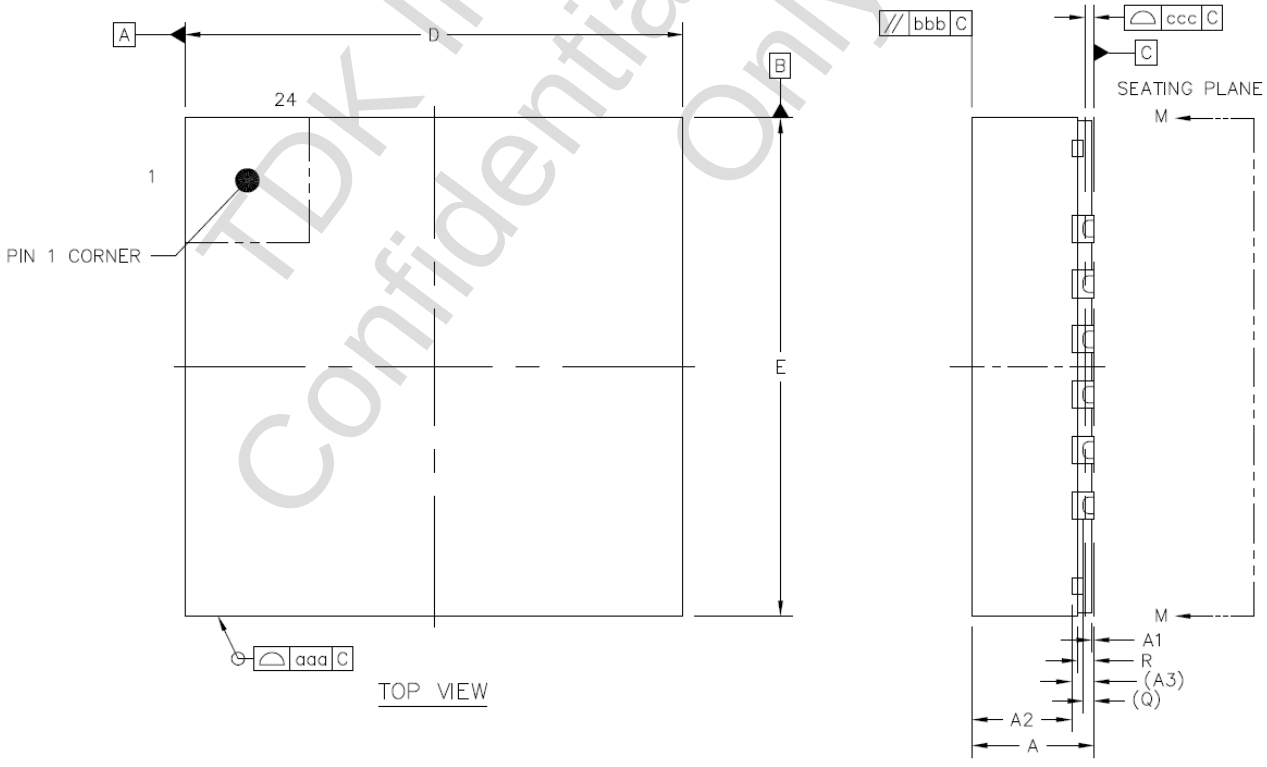

Figure 10. Package Top and Side View

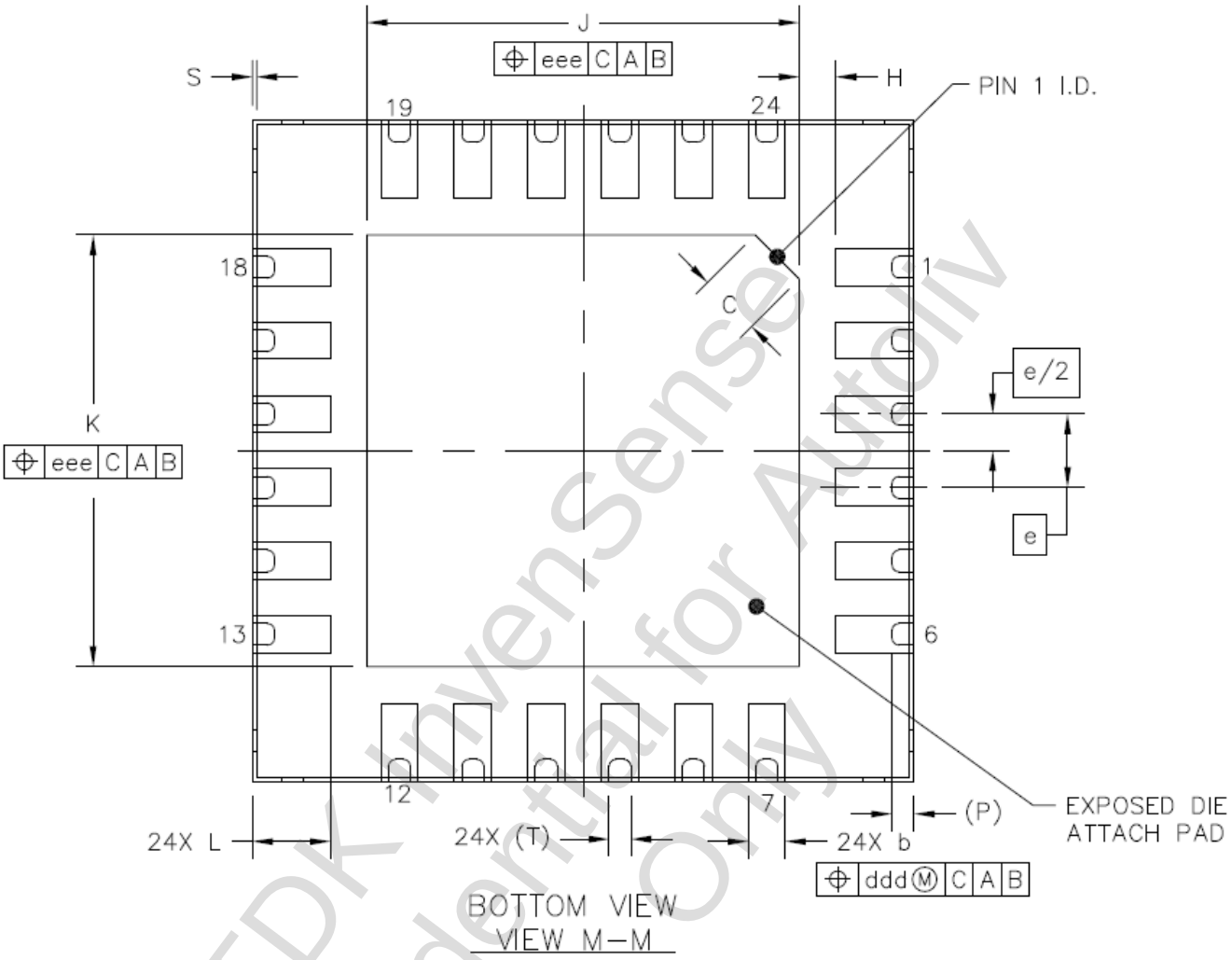

Figure 11. Package Bottom View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	1.05	1.1	1.15
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.9	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.18	0.25	0.3
BODY SIZE	X	D	4.4	4.5	4.6
	Y	E	4.4	4.5	4.6
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	2.89	2.94	2.99
	Y	K	2.89	2.94	2.99
LEAD LENGTH		L	0.48	0.53	0.58
		C	0.374	0.424	0.474
		H	0.2	0.25	0.3
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	
		fff		0.05	
HALF-CUT DEPTH		R	0.11	0.15	0.2
HALF-CUT WIDTH		S	0.001	0.015	0.03
WETTABLE DIMPLE WIDTH		T	0.1	0.15	0.2
WETTABLE DIMPLE LENGTH		P	0.05	0.15	0.25
WETTABLE DIMPLE DEPTH		Q	0.05	0.1	0.15

Table 24. Package Dimensions

9 PART NUMBER PACKAGE MARKING

The part number package marking for IAM-20685 is summarized below:

PART NUMBER	PART NUMBER PACKAGE MARKING
IAM-20685	IAM685

Table 25. Part number package marking

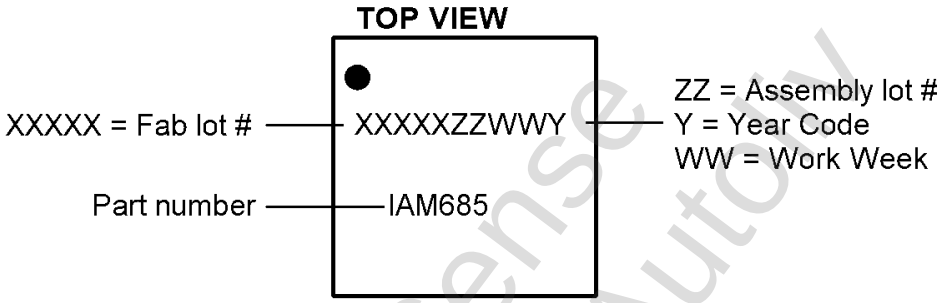

Figure 12. Part number package marking for IAM-20685

Samples with Part Number Package Marking “IAM685 E” are engineering samples and may have deviations in respect to the specifications and functions reported in the datasheet. Engineering samples are not production-intent parts.

10 REFERENCE

Please refer to “InvenSense MEMS Handling Application Note (AN-IVS-0002A-00)” for the following information:

- Manufacturing Recommendations
  - Assembly Guidelines and Recommendations
  - PCB Design Guidelines and Recommendations
  - MEMS Handling Instructions
  - ESD Considerations
  - Reflow Specification
  - Storage Specifications
  - Package Marking Specification
  - Tape & Reel Specification
  - Reel & Pizza Box Label
  - Packaging
  - Representative Shipping Carton Label
- Compliance
  - Environmental Compliance
  - DRC Compliance
  - Compliance Declaration Disclaimer

11 DOCUMENT INFORMATION

11.1 REVISION HISTORY

REVISION DATE	REVISION	DESCRIPTION
06/29/2020	1.0	Initial revision
07/30/2020	1.1	Removed “E” symbol from Part Number Package Marking

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Part Basic Properties			
Generated On(Report Generated Time):	Mar 18, 2022 12:32:25 PM (UTC)	Name:	660446100A 00
Revision:	00	Title:	Integrated Sensor, IAM-20685, QFN-24, Application dependent, SMD, (LF), (A), NEW, 3-axis Gyroscope, 3-axis Accelerometer
State:	Released	Authority:	105218 AHO GPM EL SBE EL SB COMPONENT LIBRARY
Unit of Measure:	EA	Weight as designed(Gram):	0.0
Commodity Code:	NT	Service:	TBD
BOM Uses Flag:		GPM Flag:	New
Material AMD Flag:		Lifecycle Level:	Concept
Change Process Level:	Pre-Serial	Standard BOM:	NO
Master Reference Part:	NO		

Part Specific Properties		
Part Property Definitions:	PPAP	Entry
Moisture Sensitivity Level (MSL)	No	3
1. Industry Name	No	IAM-20685
1. Measurement Range	No	+/- 300 dps
1. Sense Axis	No	XYZ
1. Sense Type	No	ANGULAR RATE
1. Sensor	No	YES
2. Measurement Range	No	+/-36 g
2. Sense Axis	No	XYZ
2. Sense Type	No	LOW G ACCEL
2. Sensor	No	YES
3. Measurement Range	No	
3. Sense Axis	No	X
3. Sense Type	No	ANGULAR RATE
3. Sensor	No	
4. Measurement Range	No	
4. Sense Axis	No	X
4. Sense Type	No	ANGULAR RATE
4. Sensor	No	NO
Geometry Package	No	QFN
Autoliv controlled	No	Application dependent
Appended Geometry Package	No	DQFN24
Lead Free	No	YES
AEC-Q	No	YES
Automotive Grade details	No	
Max. Op. Temp (C)	No	105.0
Min. Op. Temp (C)	No	-40.0
Number of Sensors	No	2
Notes:	No	
Pins	No	24
Process	No	SMD
Replaced by:	No	
Replaces (Legacy PNs)	No	
Priority	No	NEW
Polarity Marking	No	
Appended Title	No	3-axis Gyroscope, 3-axis Accelerometer

CEP / MEP:			
Type:	Name:	Revision:	Title:
Manufacturing Equivalent Part	IAM-20685	000	SENSOR, INTEGRATED, IAM-20685, QFN-24, Application dependent, SMD, (LF), (A), P5, 3-axis Gyroscope, 3-axis Accelerometer

Weight:

Weight(g):	0.500
Source:	Standard Title
Type:	Estimated
Accuracy:	Low

Autoliv Material Definitions (AMD):

The AMD's contain [CC]/[SC] characteristics, which need certification. To find characteristics that must be proven [CC]/[SC], see specifications and standards referenced below:

Autoliv Equivalent Material Definitions (EAMD):

EBOM Overview (Only First Level Shown)

BOM level	F/N	PLC	Engineering Part	Title	Quantity	Weight as designed (Gram)	Unit of measure	Relation-ship	Principal Document
0		C	660446100A 00	Integrated Sensor, IAM-20685, QFN-24, Application dependent, SMD, (LF), (A), NEW, 3-axis Gyroscope, 3-axis Accelerometer		0.0	EA		6604461 000