Release Note

T1-TARGET-SW

Release Note – Version / Template Version: 1.0

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This document provides the release information for T1-TARGET-SW V3.5.1.0 .

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1 Release Information

Software Version	V3.5.1.0
Configuration Management Reference	68423
Software Variant ID	69
Software Variant Short Name	arm7m-iar-69
Supported Target Architecture	ARMv7-M
Compiler	IAR C/C++ Compiler for Arm)
Compiler Version	V9.30.1
Release Status	**release**
Release Restrictions	**Non-certified T1-TARGET-SW release, thus unsuitable for any safety case!**
Comments	**-**

Table 1: Description, version and status

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2 List of deliverables

Path/Name	Description
/interface/T1_baseInterface.h	T1.base API header
/interface/T1_contInterface.h	T1.cont API header
/interface/T1_delayInterface.h	T1.delay API header
/interface/T1_flexInterface.h	T1.flex API header
/interface/T1_MemMap.h	Memory Map for allocation sections
/interface/T1_modInterface.h	T1.mod API header
/interface/T1_scopeInterface.h	T1.scope API header
/interface/T1_targetSpecifics.h	Target specific Declarations
/lib/libt1base.a	Library for T1.base
/lib/libt1cont.a	Library for T1.cont
/lib/libt1delay.a	Library for T1.delay
/lib/libt1flex.a	Library for T1.flex
/lib/libt1mod.a	Library for T1.mod
/lib/libt1scope.a	Library for T1.scope
/lib/version.tx	T1-TARGET-SW version information
/lib/T1_indirects.t1a	T1.stack annotations for T1-TARGET-SW
/make/[usedOS]/T1_projGen.bat	Batch file to start generation of T1 project file
/make/[usedOS]/T1_xxxxx.pm	Perl modules for OS specific extraction of Task/Isr information
/make/T1_perl/T1_projGen.pl	Perl generating of T1 project file
/make/T1_perl/T1_config.pm	Perl generating T1 configuration C files
/src/T1_AppInterface.c	C module of T1/application “glue layer”
/src/T1_AppInterface.h	C header of T1/application “glue layer”
/src/T1_config.c	T1 configuration module
/src/T1_extraConfig.c	Customer specific T1 configuration module
/10_doc/10_ReleaseNote	Release Note for T1-TARGET-SW
/10_doc/30_ResourceUsage	Resource usage summary of T1-TARGET-SW
/10_doc/40_TargetAPI	API description of T1-TARGET-SW

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3 T1-TARGET-SW Version Overview

Software Versions	Feature
V2.2.4.x	First ISO26262 certified release
V2.3.x.x	Support more than three cores (e.g. AURIX 2G)
V2.4.x.x	ISO26262 certified release
V2.5.x.x	New TraceEvent implementation; RH850E2 support starting with V2.5.8.1
V2.6.x.x	ISO26262 certified release; communication library integrated in T1.base; on-target access to T1.cont values for certified releases
V3.1.x.x	Streaming support; Beta T1.cont foreground support
V3.2.x.x	ISO26262 certified release; support for easy configuration of UserEvents, UserStopwatches and AppFeatures in inv file
V3.3.x.x	Full foreground T1.cont support
V3.2.1.1	ISO26262 certified release for VariantID 83/57 including unattended streaming and on-target access to traces
V3.3.2.0 / V3.3.3.0	T1.cont support for more than 255 tasks; T1.flex support for future features, enhancements and bugfixes
V3.4.0.0	ISO26262 certified release; full support for 2nd SWF measurements; T1.cont foreground bugfixes
V3.4.0.1	ISO26262 certified release; support for AURIX3G (V1.8 architecture)
V3.5.0.0	Full support for 2nd SWF measurements; T1.cont foreground bugfixes; Support for AURIX3G (V1.8 architecture)
V3.5.1.0	IAR support for Arm Cortex-M

Table 2: Major Features in Version

4 List of Changes / new Features

4.1 Bugfixes

Ticketnumber	2849
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_InitDelaysPC should return T1_PLUGIN_NOT_AVAILABLE.**
Notes	Workaround: No workaround!
Implemented in Version	V3.5.1.0

Ticketnumber	2851
Core Architecture	all
Compiler	all
Variant	all
Description	**Update Mobilgene OS perl module.**
Notes	Workaround: No workaround!
Implemented in Version	V3.5.1.0

Ticketnumber	2863
Core Architecture	MPC5xxx
Compiler	Diab
Variant	all
Description	**Diab MPC T1.flex does not support NCA on indirect calls through CTR when using T1_OuterExceptionHandlerNoOptCoreN entry symbol.**
Notes	Workaround: No workaround!
Implemented in Version	V3.5.1.0

Ticketnumber	2864
Core Architecture	all
Compiler	all
Variant	all
Description	**Issue in T1_TresosSafetyOs.pm leads to Perl warning about concatenation of string with an uninitialized value.**
Notes	Workaround: Get updated perl script from GLIWA!
Implemented in Version	V3.5.1.0

Ticketnumber	2865
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_TraceUint32PC causes corrupted trace when SWD is applied on the same variable.**
Notes	Workaround: Do not use both on the same variable!
Implemented in Version	V3.5.1.0

Ticketnumber	2773
Core Architecture	ARMV8R
Compiler	all
Variant	all
Description	**Arm Cortex-R LDR (register) to PC indirect call cannot be measured when one of the two source registers is R12/IP (it will crash).**
Notes	Workaround: Use manual T1.stack annotations, rather than performing T1.flex measurements for such indirect calls. As far as we know, this particular instruction is not generated by any of the supported compilers, so this issue relates only to hand-coded assembly.
Implemented in Version	V3.5.0.0

Ticketnumber	2777
Core Architecture	MPC5xxx
Compiler	Diab
Variant	all
Description	**Diab MPC foreground T1.cont UED and UEC with 'halt trigger on access' does not halt tracing.**
Notes	Workaround: No workaround!
Implemented in Version	V3.5.0.0

Ticketnumber	2785
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_ContBgHandler returns T1_BUSY with foreground T1.cont enabled and template code does not handle it.**
Notes	Workaround: Contact GLIWA support to update templates!
Implemented in Version	V3.5.0.0

Ticketnumber	2787
Core Architecture	all
Compiler	all
Variant	all
Description	**Resetting results after overhead calibration causes initial instances of tasks not to be reported by foreground T1.cont.**
Notes	Workaround: No workaround!
Implemented in Version	V3.5.0.0

Ticketnumber	2788
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_TraceSync may produce incorrect results when a trace timer is not a sync timer with fewer bits.**
Notes	Workaround: No workaround!
Implemented in Version	V3.5.0.0

Ticketnumber	2802
Core Architecture	all
Compiler	all
Variant	all
Description	**Some TRACE32 invocation parameter default value are wrongly documented.**
Notes	Workaround: Request updated invocation documentation!
Implemented in Version	V3.5.0.0

Ticketnumber	2835
Core Architecture	all
Compiler	all
Variant	all
Description	**T1.cont does not consider final stopwatch for T1.scope calibration and it tends to be that which observes the lowest overhead.**
Notes	Workaround: No workaround!
Implemented in Version	V3.5.0.0

Ticketnumber	2841
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_ResetDelays should return the documented status values.**
Notes	Workaround: No workaround!
Implemented in Version	V3.5.0.0

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Ticketnumber	2635
Core Architecture	ARM7M
Compiler	all
Variant	all
Description	**Arm7M HardFault will not be forwarded to the application HardFault handler when DWT flags are set after a masked data breakpoint.**
Notes	Workaround: No workaround!
Implemented in Version	V3.4.0.0

Ticketnumber	2664
Core Architecture	all
Compiler	all
Variant	all
Description	**When a focus measurement halts successfully, after counting the given number of events, subsequent focus measurements can give unpredictable results.**
Notes	Workaround: Do not use T1.cont foreground!
Implemented in Version	V3.4.0.0

Ticketnumber	2721
Core Architecture	all
Compiler	all
Variant	all
Description	**MPC and Arm-v7/8R can get spurious T1.flex breakpoints.**
Notes	Workaround: Avoid using the same symbol for SWF/SWC and any other measurement.
Implemented in Version	V3.4.0.0

Ticketnumber	2748
Core Architecture	MPC5xxx
Compiler	Diab
Variant	all
Description	**Diab MPC foreground T1.cont UEDM code addresses are corrupt in the upper 16 bits.**
Notes	Workaround: Do not use T1.cont foreground with Diab/MPC variants.
Implemented in Version	V3.4.0.0

Ticketnumber	2760
Core Architecture	all
Compiler	all
Variant	all
Description	**Task ID is not range-checked at T1_WAIT / T1_RESUME events, which can lead to an illegal memory access.**
Notes	Workaround: Use range check for Task ID in OS trace interface.
Implemented in Version	V3.4.0.0

Ticketnumber	2761
Core Architecture	all
Compiler	all
Variant	all
Description	**If there is a communications timeout with a pending immediate message, the T1-TARGET-SW will make an illegal memory access.**
Notes	Workaround: Do not use immediate messages.
Implemented in Version	V3.4.0.0

Ticketnumber	2762
Core Architecture	all
Compiler	all
Variant	all
Description	**With foreground T1.cont, wait event can produce incorrect CET values in tasks pre-empted by the waiting task.**
Notes	Workaround: Do not use T1.cont foreground in ECC scenarios.
Implemented in Version	V3.4.0.0

Ticketnumber	2477
Core Architecture	all
Compiler	all
Variant	all
Description	**Templates incorrect for T1.cont remote core processing.**
Notes	Workaround: Contact GLIWA for updated templates.
Implemented in Version	V3.4.0.0

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Ticketnumber	2625
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_AppInterface.h checks for T1_UDE_CHECK_INTEGRATION_SYNCTIMER but should check for T1_UDE_CHECK_INTEGRATION_SYNCTIMER_CORE_ALL.**
Notes	Workaround: Ask GLIWA for updates.
Implemented in Version	V3.4.0.0

Ticketnumber	2630
Core Architecture	all
Compiler	all
Variant	all
Description	**$ symbolPrefix is added twice in the Perl scripts.**
Notes	Workaround: Contact GLIWA for updated scripts.
Implemented in Version	V3.4.0.0

Ticketnumber	2637
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_Tresos.pm for AutoCore OS fails to assign CAT2 interrupt to the correct core.**
Notes	Workaround: Contact GLIWA for updated scripts.
Implemented in Version	V3.4.0.0

Ticketnumber	2707
Core Architecture	all
Compiler	all
Variant	all
Description	**Corrupted DAF/CAF results with parallel measurements.**
Notes	Workaround: Do not use parallel T1.flex measurements.
Implemented in Version	V3.4.0.0

Ticketnumber	2485
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_SetStopTrigger may halt only after an entire additional trace buffer when it should have stopped after exactly the first entry.**
Notes	Workaround: -
Implemented in Version	V3.4.0.0

Ticketnumber	2629
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_NOF_CORES definition is checked unconditionally.**
Notes	Workaround: Contact GLIWA for updated templates.
Implemented in Version	V3.4.0.0

Ticketnumber	2644
Core Architecture	all
Compiler	all
Variant	all
Description	**Check integration cross-core test can trigger MPU violation.**
Notes	Workaround: Contact GLIWA for updated templates.
Implemented in Version	V3.4.0.0

Ticketnumber	2649
Core Architecture	all
Compiler	all
Variant	all
Description	**When tracing halts with a running focus measurement, there can be a timeout in the communications link.**
Notes	Workaround: -
Implemented in Version	V3.4.0.0

Ticketnumber	2751
Core Architecture	all
Compiler	all
Variant	all
Description	**Foreground T1.cont checks constraints also when the are disabled.**
Notes	Workaround: -
Implemented in Version	V3.4.0.0

Ticketnumber	2617
Core Architecture	all
Compiler	all
Variant	all
Description	**Min value of cross-core event chain does not get updated until the max value is updated.**
Notes	Workaround: -
Implemented in Version	V3.4.0.0

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Ticketnumber	2675
Core Architecture	all
Compiler	all
Variant	all
Description	**Focus on cross-core activation does not work with foreground T1.cont.**
Notes	Workaround: -
Implemented in Version	V3.4.0.0

Ticketnumber	2690
Core Architecture	all
Compiler	all
Variant	all
Description	**Foreground T1.cont does not support tracing T1_STOPWATCH_STOP_START_INC with the last T1.cont-supervised user stopwatch ID plus one.**
Notes	Workaround: -
Implemented in Version	V3.4.0.0

Ticketnumber	2691
Core Architecture	all
Compiler	all
Variant	all
Description	**Foreground T1.cont assumes that T1_STOPWATCH_STOP_START_INC is only used with pairs of stopwatches of the same (CET/GET) type.**
Notes	Workaround: -
Implemented in Version	V3.4.0.0

Ticketnumber	2610
Core Architecture	all
Compiler	all
Variant	all
Description	**Unreliable cross-core event chain results.**
Notes	Workaround: Do not use cross-core event chain with foreground T1.cont!
Implemented in Version	V3.3.3.0

Ticketnumber	2611
Core Architecture	all
Compiler	all
Variant	all
Description	**Wrong T1.cont result from cross-core event chain.**
Notes	Workaround: Do not use cross-core event chain with foreground T1.cont!
Implemented in Version	V3.3.3.0

Ticketnumber	1810
Core Architecture	all
Compiler	all
Variant	all
Description	**Sanity checks on the included header file are also performed for unused systems.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2312
Core Architecture	TCall
Compiler	Tasking
Variant	all
Description	**Tasking __disable_and_save intrinsic can generate more than one disable instruction.**
Notes	Workaround: Not needed as T1 libraries were not affected! See also bug notification 2312.
Implemented in Version	V3.3.2.0

Ticketnumber	2317
Core Architecture	ARM7M
Compiler	GCC
Variant	all
Description	**Arm7m T1_GET_PRIMASK lacks volatile qualifier.**
Notes	Workaround: If necessary, add qualifier manually!
Implemented in Version	V3.3.2.0

Ticketnumber	2320
Core Architecture	TCall
Compiler	all
Variant	all
Description	**TriCore DPC is not effective for SWFB and SWC.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.2.0

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Ticketnumber	2337
Core Architecture	all
Compiler	all
Variant	all
Description	**Some events between calibration and the first run of the background handler are discarded.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2344
Core Architecture	TCall
Compiler	Tasking
Variant	all
Description	**Remove pragma noclear from Tasking T1_MemMap.h because it conflicts with option –eabi-compliant.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2345
Core Architecture	all
Compiler	all
Variant	all
Description	**Check on osBasicSchedFrameId is not working if value is 0.**
Notes	Workaround: Contact GLIWA for a perl script update!
Implemented in Version	V3.3.2.0

Ticketnumber	2364
Core Architecture	all
Compiler	all
Variant	all
Description	**Tracing cross-core activation indicates the wrong activating core with background T1.cont.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2384
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_RtaOs.pm can parse non-task element if TASK is in their name.**
Notes	Workaround: Contact GLIWA for a perl script update!
Implemented in Version	V3.3.2.0

Ticketnumber	2390
Core Architecture	all
Compiler	all
Variant	all
Description	**-featureMaskCallback can not be disabled after it has been enabled.**
Notes	Workaround: Contact GLIWA for a perl script update!
Implemented in Version	V3.3.2.0

Ticketnumber	2394
Core Architecture	all
Compiler	all
Variant	all
Description	**Macros T1_CORE_COMMS_SEC_VAR_POWER_ON_CLEARED_8/16 are not defined.**
Notes	Workaround: If needed, define the macros manually!
Implemented in Version	V3.3.2.0

Ticketnumber	2399
Core Architecture	all
Compiler	all
Variant	all
Description	**Perl Script Issue: Event Chain cannot be taken over from previous T1P if used systemelemts ID by Event Chain is 0.**
Notes	Workaround: Contact GLIWA for a perl script update!
Implemented in Version	V3.3.2.0

Ticketnumber	2408
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_SetStopTrigger return value T1_VALUE is not documented.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2409
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_SetStopTrigger returns T1_NOFUNC in case of an error.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2422
Core Architecture	all
Compiler	all
Variant	all
Description	**If T1.cont is disabled via the plugin table, T1_ConfigEventChainIntern crashes if called from T1_CONT_CALIBRATE_OVERHEADS....**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2450
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_RTA.h fail compilation with RTA OS generator.**
Notes	Workaround: Contact GLIWA for updated T1_RTA.h!
Implemented in Version	V3.3.2.0

Ticketnumber	2479
Core Architecture	all
Compiler	all
Variant	all
Description	**Core specific symbol files will cause corrupted T1 project file.**
Notes	Workaround: Contact GLIWA for a perl script update!
Implemented in Version	V3.3.2.0

Ticketnumber	2480
Core Architecture	all
Compiler	all
Variant	all
Description	**Parameters -retainMax and -retainIgnoreCase are ignored.**
Notes	Workaround: Contact GLIWA for a perl script update!
Implemented in Version	V3.3.2.0

Ticketnumber	2486
Core Architecture	all
Compiler	all
Variant	all
Description	**T1 project file is written using UTF-8 encoding, but read using the systems locale encoding.**
Notes	Workaround: Contact GLIWA for a perl script update!
Implemented in Version	V3.3.2.0

Ticketnumber	2509
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_configBuff.c includes T1_bid.h.**
Notes	Workaround: Contact GLIWA for a perl script update!
Implemented in Version	V3.3.2.0

Ticketnumber	2537
Core Architecture	all
Compiler	all
Variant	all
Description	**When calibrated overhead is slightly too large, foreground T1.cont can produce large errors in CET and CPU load.**
Notes	Workaround: Check for correct overhead calibration if possible!
Implemented in Version	V3.3.2.0

Ticketnumber	2560
Core Architecture	all
Compiler	all
Variant	all
Description	**Correct IPT for task with multiple activations when that task can stop and restart at a single stop/start event.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2564
Core Architecture	all
Compiler	all
Variant	all
Description	**Setting the T1.scope overhead to 0 might result in an error during compile time.**
Notes	Workaround: Contact GLIWA for a workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2583
Core Architecture	all
Compiler	all
Variant	all
Description	**Array out of bounds in T1_AppInit.**
Notes	Workaround: Contact GLIWA for a workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2590
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_TransmitFrame( ) unused parameter pData.**
Notes	Workaround: Contact GLIWA for a workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2599
Core Architecture	ARM7M
Compiler	all
Variant	all
Description	**ARMv7M FPBv1: NCA/PCA do not work.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.2.0

Ticketnumber	2300
Core Architecture	ARM7R
Compiler	all
Variant	all
Description	**SWD does not work on TI RM57 (ARMv7-R LE).**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.1.0

Ticketnumber	2303
Core Architecture	all
Compiler	all
Variant	all
Description	**Cross-core event chain min value does not reset.**
Notes	Workaround: Ignore the min value of the cross-core event chain!
Implemented in Version	V3.3.1.0

Ticketnumber	2196
Core Architecture	ARM8R
Compiler	all
Variant	all
Description	**Armv8R T1.flex ARM instruction set fails to forward non-T1.flex Prefetch Abort exception to application.**
Notes	Workaround: Customers with variant 85 at V3.2.1.0 must use the Thumb instruction set entry points to T1.flex to avoid this bug!)
Implemented in Version	V3.3.0.0

Ticketnumber	2219
Core Architecture	all
Compiler	all
Variant	all
Description	**Shifted memory-mapped trace timer cannot be used as synchronization timer.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.0.0

Ticketnumber	2039
Core Architecture	all
Compiler	all
Variant	all
Description	**T1.cont state T1_WRN_INCOMPLETE_ANALYSIS is set during init and in background handler.**
Notes	Workaround: No workaround!
Implemented in Version	V3.3.0.0

Ticketnumber	2139
Core Architecture	all
Compiler	all
Variant	all
Description	**Invalid inputs from T1-HOST-SW can cause unexpected behaviour.**
Notes	Workaround: No workaround needed! (Use only released T1-HOST-SW versions!)
Implemented in Version	V3.2.1.0

Ticketnumber	2101
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_flexInitSem is not in .T1_clear.**
Notes	Workaround: No workaround needed!
Implemented in Version	V3.2.0.0

Ticketnumber	1994
Core Architecture	all
Compiler	all
Variant	all
Description	**T1.flex should not check code addresses when starting a data measurement.**
Notes	Workaround: No workaround needed!
Implemented in Version	V3.2.0.0

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Ticketnumber	2057
Core Architecture	all
Compiler	all
Variant	all
Description	**Enable cross-core activation only when there is really more than one core.**
Notes	Workaround: No workaround needed!
Implemented in Version	V3.2.0.0

Ticketnumber	2056
Core Architecture	V850E3
Compiler	GHS
Variant	all
Description	**Checksums missing in version.tx for libs.**
Notes	Workaround: No workaround!
Implemented in Version	V3.2.0.0

Ticketnumber	2043
Core Architecture	all
Compiler	all
Variant	all
Description	**Remote core T1.cont is not compatible with SWD when sync timer == trace timer.**
Notes	Workaround: Do not use T1.cont remote core or use different timers for trace timer and sync timer!
Implemented in Version	V3.2.0.0

Ticketnumber	2002
Core Architecture	ARM7R
Compiler	GCC
Variant	all
Description	**ARMv7-R UEDM / DCA address is off by 4.**
Notes	Workaround: No workaround!
Implemented in Version	V3.2.0.0

Ticketnumber	1997
Core Architecture	all
Compiler	all
Variant	all
Description	**With remote T1.cont, "SetStopTrigger" checks the size of input parameter "afterXevents" against wrong core's buffer size.**
Notes	Workaround: No workaround!
Implemented in Version	V3.2.0.0

Ticketnumber	2032
Core Architecture	all
Compiler	all
Variant	all
Description	**SWD fails when sync timer is trace timer and 28 bits or more (V3.1.5.0 concerned).**
Notes	Workaround: Use a sync timer with less than 28 bits or avoid SWD measurements!
Implemented in Version	V3.2.0.0

Ticketnumber	1967
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_cpuLoadTxPeriodPC and T1_avgCPULoadSamplesPC are not of the same type.**
Notes	Workaround: Make sure that -cpuLoadAvgSamples and -cpuLoadTxPeriod are set to max 255!
Implemented in Version	V3.2.0.0

Ticketnumber	1966
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_TraceUint16 only works for big-endian processors.**
Notes	Workaround: No workaround!
Implemented in Version	V3.1.5.0

Ticketnumber	1861
Core Architecture	all
Compiler	all
Variant	all
Description	**When no events are being logged to the trace buffer, streaming can generate corrupt trace data.**
Notes	Workaround: Ensure that at least one event is traced between every two calls to T1_HandlerPC
Implemented in Version	V3.1.5.0

Ticketnumber	1771
Core Architecture	all
Compiler	all
Variant	all
Description	**User Stopwatches with ids >= 256 will wrap back to lower ID space.**
Notes	Workaround: Use Stopwatch IDs < 256!
Implemented in Version	V3.1.5.0

Ticketnumber	1951
Core Architecture	all
Compiler	all
Variant	all
Description	**T1.cont only supports 128 stopwatches (user plus flex plus event chains), not 255 - from 3.1.0.z to 3.1.3.z.**
Notes	Workaround: Use at maximum 128 stopwatches!
Implemented in Version	V3.1.5.0

Ticketnumber	1935
Core Architecture	TC1.6.1
Compiler	all
Variant	all
Description	**Some T1.flex measurement on a "syscall" instruction do not work.**
Notes	Workaround: Contact GLIWA for details!
Implemented in Version	V3.1.5.0

Ticketnumber	1841
Core Architecture	all
Compiler	all
Variant	all
Description	**V3.1.3.x allows at most 128 T1.flex stopwatches to be supervised by T1.cont.**
Notes	Workaround: Do not define more than 128 T1.flex stopwatches!
Implemented in Version	V3.1.5.0

Ticketnumber	1844
Core Architecture	ARM7M
Compiler	all
Variant	all
Description	**ARM-v7M T1.flex forwarding of non T1.flex HardFault exceptions crashes.**
Notes	Workaround: No workaround!
Implemented in Version	V3.1.4.0

Ticketnumber	1847
Core Architecture	ARM7R
Compiler	Keil
Variant	all
Description	**T1_TraceData leaves interrupts disabled.**
Notes	Workaround: Disable interrupts some other way (e.g. T1_Suspend/ResumeAllInterrupts) and use T1_TraceDataNoSusp.
Implemented in Version	V3.1.4.0

Ticketnumber	1823
Core Architecture	all
Compiler	all
Variant	all
Description	**ns to tick conversion for core0 is used for all cores to initialize T1 overheads.**
Notes	Workaround: Always (re)calibrate overheads immediately after T1_Init().
Implemented in Version	V3.1.3.1

Ticketnumber	1767
Core Architecture	all
Compiler	all
Variant	all
Description	**Target-configured minimum constraints (T1_STPW_IDX_CONSTRAINT) fire only when value is 2 trace timer ticks below the threshold.**
Notes	Workaround: Reduce target-configured constraints by two timer ticks with releases before V3.1.3.0.
Implemented in Version	V3.1.3.0

Ticketnumber	1353
Core Architecture	all
Compiler	all
Variant	all
Description	**Ensure that the T1.cont stopwatches corresponding to the calibration T1.flex stopwatch and the event chains are cleared before use.**
Notes	Details: T1-HOST-SW V2.5.0 or higher has a workaround for the problem.
Implemented in Version	V3.1.1.0

Ticketnumber	1474
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_Handler can fail to run in user mode if the T1-HOST-SW requests (re)calibration.**
Notes	Details: If the calibration is done in supervisor mode and it fails or is disabled, T1_Handler no longer works in user mode.
Implemented in Version	V3.1.0.0

Ticketnumber	1497
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_COUNT_PREEMPTION is not compatible with T1_TraceStartAct/T1_TraceStartNoAct.**
Notes	Workaround: Use either T1_COUNT_PREEMPTION or T1_TraceStartAct/T1_TraceStartNoAct but not both together.
Implemented in Version	V3.1.0.0

Ticketnumber	1558
Core Architecture	ARM7R
Compiler	all
Variant	all
Description	**ARMv7R stops responding when doing an advanced DAF measurement and the flexAnalysisCapacity is set to 9.**
Notes	Workaround: Do not set the flexAnalysisCapacity to ’9’.
Implemented in Version	V3.1.0.0

Ticketnumber	1614
Core Architecture	all
Compiler	all
Variant	all
Description	**Require Perl version 5.6.0.**
Notes	
Implemented in Version	V3.1.0.0

Ticketnumber	1717
Core Architecture	all
Compiler	all
Variant	all
Description	**Type of T1_traceTimerBitLengthPC is wrong.**
Notes	Details: The type of T1_traceTimerBitLengthPC is T1_uint8_t but not T1_bool_t.
Implemented in Version	V3.1.0.0

Ticketnumber	1414
Core Architecture	all
Compiler	all
Variant	all
Description	**Increased CET at traceBuffer wrap-around.**
Notes	Details: At tracebuffer wraparound the CET of the measured system element at that time was increased by around 70ns (depends on the cpu core!). This is only relevant for very short functions and especially with DPC measurements.
Implemented in Version	V2.6.0.0

Ticketnumber	726
Core Architecture	all
Compiler	all
Variant	all
Description	**T1.mod is not multi-core-safe.**
Notes	Details: T1.mod could be safely used only in single-core environments.
Implemented in Version	V2.5.8.0

Ticketnumber	1376
Core Architecture	all
Compiler	all
Variant	all
Description	**Number of constraints can have multiple definitions.**
Notes	Details: T1_NOF_CSRNS_COREX can be defined in T1_AppInterface.h instead of using the inv parameter, but it is not checked and the Perl script will always generate a macro in T1_config.h
Implemented in Version	V2.5.8.0

Ticketnumber	1056
Core Architecture	all
Compiler	all
Variant	all
Description	**ISR events cannot be used as BSF delimiters.**
Notes	
Implemented in Version	V2.5.8.0

Ticketnumber	1374
Core Architecture	ARM7R
Compiler	all
Variant	all
Description	**T1 ARMv7R libraries can enable IRQs while CPU is in IRQ mode.**
Notes	Workaround: No Workaround, see bug notification **t1target_1374_arm7rFlexEnableInterrupts.pdf**
Implemented in Version	V2.5.7.0

Ticketnumber	1344
Core Architecture	TC1.3.1
Compiler	Tasking
Variant	all
Description	**Macro T1_INTERRUPTS_ARE_ENABLED is wrong for TriCore 1.3.1 (TASKING).**
Notes	Workaround: No Workaround
Implemented in Version	V2.5.7.0

Ticketnumber	1342
Core Architecture	V850E3
Compiler	all
Variant	all
Description	**RH850 core-specific code is in .T1_codeFast but should be in .T1_codeCoreN.**
Notes	
Implemented in Version	V2.5.5.0

Ticketnumber	1183
Core Architecture	all
Compiler	all
Variant	all
Description	**Re-configuration of calibration event chains fails.**
Notes	Workaround: No workaround possible, calibration event chains GET IDs 1, 2, 3 can not be used.
Implemented in Version	V2.5.5.0

Ticketnumber	1328
Core Architecture	all
Compiler	all
Variant	all
Description	**Allow T1-TARGET-SW to receive messages split into multiple frames using comN library.**
Notes	Workaround: Do not use comN-lib.
Implemented in Version	V2.4.2.0

Ticketnumber	1327
Core Architecture	all
Compiler	all
Variant	multicore
Description	**Multi-core SWD results are unsafe when the trace timer is different from the sync timer.**
Notes	Workaround: Ensure that T1_flexGlobalsX.syncTimerIsTraceTimer_ is zero if the sync timer is not the trace timer for core ”X”. This can be done just before T1_Init.
Implemented in Version	V2.5.4.0

Ticketnumber	1326
Core Architecture	all
Compiler	all
Variant	all
Description	**Use of uninitialized value in T1_config.pm (diagMaxTxDataSize).**
Notes	
Implemented in Version	V2.5.4.0

Ticketnumber	1236
Core Architecture	TCall
Compiler	all
Variant	all
Description	**A trace buffer cannot be located at the start of a TriCore memory segment.**
Notes	
Implemented in Version	V2.5.4.0

Ticketnumber	1138
Core Architecture	MPC5xxx
Compiler	all
Variant	all
Description	**T1_FlexDisallowExternalDebug does not allow debugger coexistence with MPC5xxx parts that should support it.**
Notes	Workaround: If debugger-coexistence is required, manually check that the required resources IDM, IAC6, IAC7, IAC8 and DACx are SW-controlled and over-ride T1_FlexDisallowExternalDebug to return always T1_FALSE.
Implemented in Version	V2.5.4.0

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Ticketnumber	1306
Core Architecture	all
Compiler	all
Variant	multicore
Description	**T1_CONT_REMOTE is not supported since trace event rework (V2.5.0.0).**
Notes	Workaround: Do not use T1_CONT_REMOTE with V2.5.0-2.x versions.
Implemented in Version	V2.5.3.0

Ticketnumber	1304
Core Architecture	all
Compiler	all
Variant	multicore
Description	**T1_COUNT_PREEMPTION configuration supports at most 3 cores.**
Notes	Workaround: Do not use T1_COUNT_PREEMPTION in systems with more than 3 cores with V2.5.0-2.x versions.
Implemented in Version	V2.5.3.0

Ticketnumber	1300
Core Architecture	all
Compiler	all
Variant	all
Description	**Focus measurement is unreliable for data age with more than one read of any particular written values.**
Notes	Workaround: Do not use focus results of data-aga measurements if more than one code location reads the data.
Implemented in Version	V2.5.3.0

Ticketnumber	gcp:28
Core Architecture	all
Compiler	all
Variant	all
Description	**Variable length communication library (comN) fails with host-to-target data blocks that exceed the frame length.** **See also bug notification "commprotocol_28_comNblocksData.pdf"!**
Notes	Workaround: a) Use com8 lib (libcom8.a) b) Ensure that the frame size in bytes is at least 6 + 4 x nOfAddresses, where nOfAddresses is the size of the T1.flex address list.
Implemented in Version	V2.5.2.0

Ticketnumber	1266
Core Architecture	all
Compiler	all
Variant	all
Description	**Invalid paths in generated T1 project file if build folder path contains whitespaces.**
Notes	Workaround: Use file- /path-names without whitespaces.
Implemented in Version	V2.5.2.0

Ticketnumber	1254
Core Architecture	all
Compiler	all
Variant	multicore
Description	**T1_GetTaskIdByIdxPC needs unconditional prototype.**
Notes	Workaround: If you get a compile error copy the prototype of T1_GetTaskIdByIdxPC from T1_scopeInterface.h to T1_Config.c.
Implemented in Version	V2.5.0.0

Ticketnumber	1242
Core Architecture	all
Compiler	all
Variant	all
Description	**The units for timeoutRx and timeoutTx are described as being milliseconds but are actually numbers of the T1_Handler period.**
Notes	
Implemented in Version	V2.5.0.0

Ticketnumber	1225
Core Architecture	TCall
Compiler	all
Variant	all
Description	**PCA on a function that exceeds the measurement limit misses an expected sequential result.**
Notes	Workaround: No Workaround possible.
Implemented in Version	V2.5.0.0

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Ticketnumber	1010
Core Architecture	all
Compiler	all
Variant	all
Description	**Support for t1a files with T1_projGen.pl.**
Notes	Configuration of T1.stack annotation files by .inv files is now supported.
Implemented in Version	V2.5.0.0

Ticketnumber	1127
Core Architecture	ARM7M
Compiler	all
Variant	all
Description	**ARM Cortex M T1_TraceEvent (not NoSusp) is not thread-safe for some processors.**
Notes	Workaround: Use only NoSusp variants. Implement T1_SuspendAllInterrupts and T1_ResumeAllInterrupts to use OS routines.
Implemented in Version	V2.5.0.0

Ticketnumber	1219
Core Architecture	V850E3
Compiler	all
Variant	all
Description	**V850 test for JR/JARL disp32 instruction is unreachable in T1_ContinueData.**
Notes	No customer relevance.
Implemented in Version	V2.4.1.0

Ticketnumber	1223
Core Architecture	all
Compiler	all
Variant	all
Description	**DCA address list over-run causes a huge overhead.**
Notes	This is rarely noticed by the customer as it concerns the time for collecting access results, not the timing results!
Implemented in Version	V2.4.1.0

Ticketnumber	1212
Core Architecture	TC1.6.2
Compiler	Tasking
Variant	all
Description	**Tasking does not define __CORE_TC16X__ with TC39X.**
Notes	
Implemented in Version	V2.4.0.0

Ticketnumber	994
Core Architecture	MPC5xxx
Compiler	all
Variant	all
Description	**MPC5xxx T1.flex NCA only works with NoOpt outer exception handler.**
Notes	Workaround: Use only NoOpt outer exception handler, i.e. one of T1_OuterExceptionHandlerNoOptCore0, T1_OuterExceptionHandlerNoOptCore1, T1_OuterExceptionHandlerNoOptCore2 or T1_OuterExceptionHandlerNoOpt (any core).
Implemented in Version	V2.3.0.0

Ticketnumber	1092
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_TraceEventNoSuspTimePC is not mapped to an empty macro if T1 is disabled.**
Notes	
Implemented in Version	V2.4.0.0

Ticketnumber	1200
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_VALUE is not returned when receiving a (corrupted) message with an invalid pluginId.**
Notes	
Implemented in Version	V2.3.9.0

Ticketnumber	1195
Core Architecture	all
Compiler	all
Variant	all
Description	**With overridden T1_TraceEvent_ and T1_TraceEventNoSusp_, T1_TraceEventNoSuspTime_ must not attempt to read the current time directly.**
Notes	
Implemented in Version	V2.3.9.0

Ticketnumber	1188
Core Architecture	V850E3
Compiler	GHS
Variant	all
Description	**CAF/COV/UEC/UECS/NCA/PCA and data measurements cannot run simultaneously.**
Notes	
Implemented in Version	V2.3.9.0

Ticketnumber	1185
Core Architecture	V850E3
Compiler	GHS
Variant	all
Description	**T1 Target gliwOS Perl script does not support compilers with a prefix underscore added to symbol names.**
Notes	
Implemented in Version	V2.3.8.0

Ticketnumber	1182
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_SetStopTrigger, when the write pointer is near the end of the trace buffer, captures not the first trace buffer but the second.**
Notes	Workaround: Clearly, a complete fix can only be achieved by updating the T1.scope library. However, a common failure case occurs when capturing the start-up trace and the work-around for this specific case is to trace at least one event, for example a T1_EMPTY event, before calling T1_SetStopTrigger.
Implemented in Version	V2.3.8.0

Ticketnumber	1180
Core Architecture	all
Compiler	all
Variant	multicore
Description	**Cross-core SWD and task activation require a sync timer with at least 28 bits.**
Notes	
Implemented in Version	V2.3.8.0

Ticketnumber	1169
Core Architecture	all
Compiler	all
Variant	all
Description	**TC1.3.1 inverse restricted DAF reports zero.**
Notes	
Implemented in Version	V2.3.7.0

Ticketnumber	1161
Core Architecture	TCall
Compiler	all
Variant	all
Description	**TriCore DPC leaves ICR.IE in an unpredicatble state.**
Notes	
Implemented in Version	V2.3.6.0

Ticketnumber	1158
Core Architecture	all
Compiler	all
Variant	all
Description	**Off by one with trace buffer under-fill protection causes one too many events to be captured before trigger.**
Notes	
Implemented in Version	V2.3.6.0

Ticketnumber	1157
Core Architecture	all
Compiler	all
Variant	all
Description	**Add T1_invalidCETeventChainIdx to avoid compiler errors.**
Notes	
Implemented in Version	V2.3.6.0

Ticketnumber	1149
Core Architecture	all
Compiler	all
Variant	all
Description	**There is no consistency in the declaration of coreId as const or not as a function parameter.**
Notes	
Implemented in Version	V2.3.6.0

Ticketnumber	1151
Core Architecture	MPC5xxx
Compiler	Diab
Variant	oldCompiler
Description	**Wind River MPC5xxx V5.9.0.0 compiler bug affects T1.base and requires T1 update.**
Notes	
Implemented in Version	V2.3.5.3

Ticketnumber	1148
Core Architecture	all
Compiler	all
Variant	all
Description	**After restoring T1.cont results, auto-calibration is not possible.**
Notes	Workaround: After a soft-reset, previous calibration results can be preserved by saving and restoring T1_contGlobalsPC[coreID].overhead_ and T1_contGlobalsPC[coreID].flexOverhead_ around T1_InitPC. This avoids the need for re-calibration.
Implemented in Version	V2.3.5.0

Ticketnumber	1144
Core Architecture	all
Compiler	all
Variant	multicore
Description	**When called from core 0, template routine T1_AppSetStopTriggerAllCores only stops tracing on core 0.**
Notes	Workaround: Replace "0u != –shadowTriggerIndex" by "0u != shadowTriggerIndex–" in T1_AppInterface.c
Implemented in Version	V2.3.5.0

Ticketnumber	1129
Core Architecture	all
Compiler	all
Variant	all
Description	**If T1_InitExtra1 or T1_InitExtra1 and T1_InitExtra2 are called without T1_InitExtra3 then the next call to T1_Handler crashes.**
Notes	Workaround: Call all or none of If T1_InitExtra1, T1_InitExtra2 and T1_InitExtra3
Implemented in Version	V2.3.4.0

Ticketnumber	1121
Core Architecture	V850E3
Compiler	all
Variant	multicore
Description	**RH850 core-specific outer exception handlers only work on core 0.**
Notes	Workaround: Use shared core-independent handler for cores 1..
Implemented in Version	V2.3.3.1

Ticketnumber	1080
Core Architecture	TC1.6.1
Compiler	all
Variant	multicore
Description	**Remove core-specific flag from HighTec TriCore section pragmas in T1_MemMap.h.**
Notes	
Implemented in Version	V2.3.1.1

Ticketnumber	1055
Core Architecture	all
Compiler	all
Variant	all
Description	**Restricted SWF may give wrong results.**
Notes	
Implemented in Version	V2.2.5.0

Ticketnumber	1071
Core Architecture	all
Compiler	all
Variant	multicore
Description	**T1_taskDataPC and T1_traceIndirect are not located in explicit T1 sections.**
Notes	
Implemented in Version	V2.3.1.0

Ticketnumber	1063
Core Architecture	all
Compiler	all
Variant	all
Description	**configuration of GET Event Chains used for overhead calibration info.**
Notes	
Implemented in Version	V2.3.1.0

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Ticketnumber	1059
Core Architecture	all
Compiler	all
Variant	all
Description	**Optimize stopwatch start case for CET stopwatch.**
Notes	
Implemented in Version	V2.3.1.0

Ticketnumber	1056
Core Architecture	all
Compiler	all
Variant	all
Description	**ISR events cannot be used as BSF delimiters.**
Notes	
Implemented in Version	V2.3.1.0

Ticketnumber	1051
Core Architecture	all
Compiler	all
Variant	all
Description	**GCP_T1interface.h still uses T1_MemMap.h.**
Notes	
Implemented in Version	V2.3.1.0

Ticketnumber	1047
Core Architecture	TC1.6.2
Compiler	all
Variant	all
Description	**T1_GetCoreIdOffset must support TC39X, where CPU5 has CORE_ID = 6, for HighTec and Tasking**
Notes	Workaround: Define a suitable macro T1_GetCoreIdOffset before the include of T1_baseInterface.h.
Implemented in Version	V2.3.1.0

Ticketnumber	1034
Core Architecture	all
Compiler	all
Variant	all
Description	**T1.cont should recognise T1_START as BSF delimiter also when T1.scope logs T1_START_STOP.**
Notes	
Implemented in Version	V2.3.1.0

Ticketnumber	1027
Core Architecture	all
Compiler	all
Variant	all
Description	**Need to update settings for Vector in Perl Script.**
Notes	
Implemented in Version	V2.3.1.0

Ticketnumber	1025
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_config.pm does not balance start and stop section includes with default constraint configuration.**
Notes	Workaround: Do not use the new default constraint configuration option
Implemented in Version	V2.3.1.0

Ticketnumber	1018
Core Architecture	MPC5xxx
Compiler	all
Variant	multicore
Description	**Use core-specific section names (T1_codeCoreN) for the MPC5xxx core-specific T1.flex outer exception handlers, rather than T1_codeFast.**
Notes	
Implemented in Version	V2.3.1.0

4.2 Enhancements

Ticketnumber	1139
Core Architecture	ARM7M
Compiler	IAR
Variant	all
Description	**New adaption: IAR ARM-v7M.**
Notes	
Implemented in Version	V3.5.1.0

Ticketnumber	2487
Core Architecture	all
Compiler	all
Variant	all
Description	**Add an option to allow to specify the encoding of source files read and written by the Perl script.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2790
Core Architecture	all
Compiler	all
Variant	all
Description	**Improve accuracy for foreground T1.cont task CET/GET focus.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2792
Core Architecture	all
Compiler	all
Variant	all
Description	**Allow the traced sync width to be either 32 bits (as before) or 56 bits.**
Notes	This will be supported by T1-HOST-SW starting with V3.6.0!
Implemented in Version	V3.5.0.0

Ticketnumber	2796
Core Architecture	all
Compiler	all
Variant	all
Description	**Allow CPU load tx period to be set by T1-HOST-SW.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2804
Core Architecture	all
Compiler	all
Variant	all
Description	**Add support for TI / TMS320C66x (without T1.flex).**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2807
Core Architecture	all
Compiler	all
Variant	all
Description	**Update Perl script for support of Vlan ID when using Ethernet channel of Vector box.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2809
Core Architecture	TCall
Compiler	all
Variant	all
Description	**At least for TriCore, reduce CSA consumption by one CSA (=64 bytes) in T1_Init / T1_InitExtra3.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2823
Core Architecture	all
Compiler	all
Variant	all
Description	**Add breakpoint annotations so that T1.flex is fully analysed by T1.stack / T1.accessPredictor.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2825
Core Architecture	ARM7M
Compiler	all
Variant	all
Description	**Ensure a build-time error for invalid Arm-v7M FPB version.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2827
Core Architecture	all
Compiler	all
Variant	all
Description	**Remove requirement for cross-core accesses to T1_scopeConsts also when remote core T1.cont is configured.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2829
Core Architecture	all
Compiler	all
Variant	all
Description	**Improve performance of T1_TraceData.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2830
Core Architecture	all
Compiler	all
Variant	all
Description	**Improve performance of template T1_TraceEventUMPC.**
Notes	
Implemented in Version	V3.5.0.0

Ticketnumber	2782
Core Architecture	TCall
Compiler	all
Variant	all
Description	**Update T1.flex to support also TC4xx (AURIX 3G).**
Notes	
Implemented in Version	V3.4.0.1

Ticketnumber	2820
Core Architecture	TC1.8
Compiler	GCC
Variant	all
Description	**Manual adaptation of EVTA is required for interactive debug of TC4xx (AURIX3G) while T1.flex is active.**
Notes	In order to interactively debug on core N after running with T1.flex active, the user must halt the core and manually set HRA_DBGACT.EVTA to 2. At the end of interactive debugging, the user must manually set EVTA back to 3 before continuing to run with T1.flex active.
Implemented in Version	V3.4.0.1

Ticketnumber	2632
Core Architecture	TCall
Compiler	GCC
Variant	all
Description	**HighTec TriCore T1_MemMap.h incompatible with compiler option -mpragma-section-filter.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	0624
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_Init preserving full trace after "warm" reset.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	1974
Core Architecture	all
Compiler	all
Variant	all
Description	**INC_T1_ERROR_COUNT should halt the tracing when an error is found.**
Notes	
Implemented in Version	V3.4.0.0

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Ticketnumber	2576
Core Architecture	all
Compiler	all
Variant	all
Description	**'Check Integration' event chain shows high values.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2608
Core Architecture	all
Compiler	all
Variant	all
Description	**Document priority of -initFeatureMask over init parameter of -allocateAF.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2614
Core Architecture	ARM7R
Compiler	GCC
Variant	all
Description	**Linker error with TI compiler and GCC libs.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2638
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_ReadTraceBuffer(PC) parameter documentation.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2640
Core Architecture	all
Compiler	all
Variant	all
Description	**Update T1_DelayRoutinePC documentation on usage.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2658
Core Architecture	all
Compiler	all
Variant	all
Description	**Improve documentation about diagnostic interface.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2669
Core Architecture	all
Compiler	all
Variant	all
Description	**Add hints on how to use debugger scripts.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2689
Core Architecture	all
Compiler	all
Variant	all
Description	**Add separate flag for T1.flex code measurement B complete to better support 2nd SWF measurement.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2702
Core Architecture	all
Compiler	all
Variant	all
Description	**Protect against failed T1.flex measurements when using slots A and B in parallel.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2708
Core Architecture	all
Compiler	all
Variant	all
Description	**Provide trace buffer size in the T1P file.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2717
Core Architecture	ARM7M
Compiler	GCC
Variant	all
Description	**GCC Arm Cortex-M libs now use unaligned accesses consistently.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2741
Core Architecture	ARM7M
Compiler	GHS
Variant	all
Description	**Green Hills ARM variants reserve one register for compatibility with applications that do this also.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2753
Core Architecture	all
Compiler	all
Variant	all
Description	**Update Perl script for the connection of Ethernet channel of Vector box.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2757
Core Architecture	ARM7M
Compiler	GHS
Variant	all
Description	**Use 8-byte ARM stack alignment also with GHS.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2648
Core Architecture	all
Compiler	all
Variant	all
Description	**Update documentation for T1_Init/T1_InitPC.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2764
Core Architecture	all
Compiler	all
Variant	all
Description	**Uninitialized variables in template code.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	2674
Core Architecture	all
Compiler	all
Variant	all
Description	**Protect T1_CET_EVT_CHAIN_TO_IDX_CORE0 with ifndef to allow user override.**
Notes	
Implemented in Version	V3.4.0.0

Ticketnumber	1384
Core Architecture	all
Compiler	all
Variant	all
Description	**Allow T1.cont to supervise more than 255 tasks.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	1754
Core Architecture	all
Compiler	all
Variant	all
Description	**Enhance T1_Microsar.h to use switch between "NoSusp" and standard variants more easily.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	1976
Core Architecture	all
Compiler	all
Variant	all
Description	**Provide means to generate constraint(s) for T1 user stopwatch configuration.**
Notes	
Implemented in Version	V3.3.2.0

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Ticketnumber	1984
Core Architecture	all
Compiler	all
Variant	all
Description	**Add Lauterbach TRACE32 Target Interface Support to T1_projGen.pl.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	1986
Core Architecture	all
Compiler	all
Variant	all
Description	**Update T1_projGen.pl for New Communication Configurations format.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	1993
Core Architecture	all
Compiler	all
Variant	all
Description	**Generate macro configuration from invocation files.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2187
Core Architecture	TCall
Compiler	all
Variant	all
Description	**TriCore T1.flex init should check PROCONDBG (UCB_DBG) and report a failure if locked.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2281
Core Architecture	TCall
Compiler	all
Variant	all
Description	**Support T1.flex measurement of data address ranges for AURIX (not supported on other core architectures).**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2283
Core Architecture	all
Compiler	all
Variant	all
Description	**Document invocation file parameter -checkIntegration.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2286
Core Architecture	all
Compiler	all
Variant	all
Description	**Add T1_InitDelaysPC() to T1_AppInit().**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2293
Core Architecture	all
Compiler	all
Variant	all
Description	**Add support for -targetType=ARM8R to T1_projGen.pl.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2373
Core Architecture	all
Compiler	all
Variant	all
Description	**Document T1_AppInterface.h inclusion in generated files.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2376
Core Architecture	all
Compiler	all
Variant	all
Description	**Invocation file parameter -syncTimeBitLength should be set automatically if -traceTimerIsSyncTimer=true.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2413
Core Architecture	all
Compiler	all
Variant	all
Description	**T1 check integration should allow checking of trace timer overflow also in init trace.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2414
Core Architecture	all
Compiler	all
Variant	all
Description	**Add CERT-C compliance.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2415
Core Architecture	all
Compiler	all
Variant	all
Description	**Enhance "T1 overhead measurement 0" (support finishing).**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2420
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_projGen.pl does not have to generate .t0p.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2424
Core Architecture	all
Compiler	all
Variant	all
Description	**Support also FIFO/LIFO stopwatch types with -allocateUserSW.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2427
Core Architecture	all
Compiler	all
Variant	all
Description	**Generating stack information out of OS configuration.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2465
Core Architecture	all
Compiler	all
Variant	all
Description	**Do not include T1_targetSpecifics.h if T1 is disabled.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2503
Core Architecture	all
Compiler	all
Variant	all
Description	**Preserve project level StackQueryConfiguration.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2566
Core Architecture	all
Compiler	all
Variant	all
Description	**Invert ISR prios for ARM in T1_Tresos.pm.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2575
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_flexInterface.h unconditionally declares variables T1_addrsCore0...2.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2581
Core Architecture	all
Compiler	all
Variant	all
Description	**Check number of bytes in T1_ReceiveMessage also for a standard GCP message.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	2593
Core Architecture	all
Compiler	all
Variant	all
Description	**When T1.cont is enabled, it might read old trace data from when the analysis was supposed to be disabled.**
Notes	
Implemented in Version	V3.3.2.0

Ticketnumber	1513
Core Architecture	ARM7M
Compiler	all
Variant	all
Description	**Support for Cortex-M FPBv1 and FPBv2 with one library.**
Notes	
Implemented in Version	V3.3.0.1

Ticketnumber	784
Core Architecture	all
Compiler	all
Variant	all
Description	**Split T1.cont functionality into foreground and background processing.**
Notes	Please contact GLIWA support for details on activating foreground T1.cont!
Implemented in Version	V3.3.0.0

Ticketnumber	793
Core Architecture	all
Compiler	all
Variant	all
Description	**Support Cross-core event chain.**
Notes	T1 supports now one real cross-core event-chain.
Implemented in Version	V3.3.0.0

Ticketnumber	2164
Core Architecture	all
Compiler	all
Variant	all
Description	**Add T1_TraceFloat, T1_TraceUint64 and T1_TraceSint64 to the T1-TARGET-SW API.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	2154
Core Architecture	all
Compiler	all
Variant	all
Description	**Reintroduce T1_TraceSyncTimer.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	2107
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_ContResetBgTaskIdPC has no Doxygen description.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	2138
Core Architecture	all
Compiler	all
Variant	all
Description	**The inv parameter -usingMulticoreLibs should default to true.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	2141
Core Architecture	all
Compiler	all
Variant	all
Description	**Document (Doxygen) which T1 APIs are callbacks and which are callouts.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	2226
Core Architecture	all
Compiler	all
Variant	all
Description	**Create new T1_Trace...NoSuspTimePC APIs so that we can pass in a particular time.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	1954
Core Architecture	all
Compiler	all
Variant	all
Description	**Provide means to generate T1.delay configuration.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	1955
Core Architecture	all
Compiler	all
Variant	all
Description	**Allow static initialization of T1.delay(s).**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	1957
Core Architecture	all
Compiler	all
Variant	all
Description	**Provide means to generate User Data Event configuration.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	2161
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_gliwOS.pm needs to get "cross-core activation tasks" to be visible to all cores.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	2236
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_rawData_t is unused and could therefore be removed.**
Notes	
Implemented in Version	V3.3.0.0

Ticketnumber	2159
Core Architecture	all
Compiler	all
Variant	all
Description	**T1-TARGET-SW stand-alone (streaming without T1-HOST-SW) and on-target Access to Traces for certified Libraries.**
Notes	
Implemented in Version	V3.2.1.1

Ticketnumber	1980
Core Architecture	all
Compiler	all
Variant	all
Description	**Allow assignment of Runnables to ISRs.**
Notes	
Implemented in Version	V3.2.0.0

Ticketnumber	1956
Core Architecture	all
Compiler	all
Variant	all
Description	**Provide means to generate User Event configuration.**
Notes	User Events can now be configured easily in inv files.
Implemented in Version	V3.2.0.0

Ticketnumber	1912
Core Architecture	all
Compiler	all
Variant	all
Description	**Add comments to T1_configGen.c.**
Notes	
Implemented in Version	V3.2.0.0

Ticketnumber	2095
Core Architecture	all
Compiler	all
Variant	all
Description	**Adopt recommended AUTOSAR naming scheme for T1_MemMap.h macro names.**
Notes	
Implemented in Version	V3.2.0.0

Ticketnumber	2017
Core Architecture	all
Compiler	all
Variant	all
Description	**Add shared memory host communications (e.g. for debugger as target interface) to templates.**
Notes	
Implemented in Version	V3.2.0.0

Ticketnumber	1983
Core Architecture	all
Compiler	all
Variant	all
Description	**Add IPv6 Target Interface Support to T1_projGen.pl.**
Notes	
Implemented in Version	V3.2.0.0

Ticketnumber	1958
Core Architecture	all
Compiler	all
Variant	all
Description	**Provide means to generate Application Feature configuration.**
Notes	AppFeatures can now be configured easily in inv files.
Implemented in Version	V3.2.0.0

Ticketnumber	1593
Core Architecture	all
Compiler	all
Variant	all
Description	**Use macros rather than magic numbers in T1_configGen.c.**
Notes	
Implemented in Version	V3.2.0.0

Ticketnumber	1483
Core Architecture	all
Compiler	all
Variant	all
Description	**Add bounds check to trace buffer write pointer for CERT releases.**
Notes	
Implemented in Version	V3.2.0.0

Ticketnumber	1824
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_TRIGGER_SYNC renamed to T1_TRIGGER.**
Notes	
Implemented in Version	V3.1.5.0

Ticketnumber	1933
Core Architecture	all
Compiler	all
Variant	all
Description	**Provide means to generate T1 user stopwatch configuration.**
Notes	Stopwatches can now be configured easily in inv files.
Implemented in Version	V3.1.5.0

Ticketnumber	1909
Core Architecture	all
Compiler	all
Variant	all
Description	**Allow UEDM trigger to be inhibited.**
Notes	
Implemented in Version	V3.1.5.0

Ticketnumber	1838
Core Architecture	MPC5xxx
Compiler	Diab
Variant	all
Description	**Set unused, empty Wind River section name to an obviously illegal section name.**
Notes	
Implemented in Version	V3.1.3.2

Ticketnumber	1835
Core Architecture	MPC5xxx
Compiler	Diab
Variant	all
Description	**Reserve Wind River MPC5xxx registers R14..R21 for potential SDA support.**
Notes	
Implemented in Version	V3.1.3.1

Ticketnumber	1235
Core Architecture	all
Compiler	all
Variant	all
Description	**Make a callback on AppFeature-changed, to void T1_AppFeatureChanged(void).**
Notes	Details: On customer request there was introduced a callback function which is called if an AppFeature bit changes.
Implemented in Version	V3.1.1.0

Ticketnumber	1263
Core Architecture	all
Compiler	all
Variant	all
Description	**Support IPT for Multi Cross-Core Activation.**
Notes	Details: Before this release, only one cross-core activation was supported. Now multiple cross-core activations are supported.
Implemented in Version	V3.1.0.0

Ticketnumber	1551
Core Architecture	all
Compiler	all
Variant	all
Description	**Continuous trace download (streaming).**
Notes	Details: Support for streaming continuous scheduling traces was added.
Implemented in Version	V3.1.0.0

Ticketnumber	1711
Core Architecture	all
Compiler	all
Variant	all
Description	**Add optional parameter -enableStreaming to enable streaming to T1_projGen.pl.**
Notes	Details: This parameter can be used during integration to indicate to the T1-HOST-SW that streaming is possible with this target.
Implemented in Version	V3.1.0.0

Ticketnumber	1431
Core Architecture	ARM7R
Compiler	Keil
Variant	all
Description	**Port ARM Cortex-R libs for ARM (Keil) compiler.**
Notes	
Implemented in Version	V3.1.0.0

Ticketnumber	784
Core Architecture	all
Compiler	all
Variant	all
Description	**BETA: Split T1.cont functionality into foreground and background processing.**
Notes	Details: A beta version of T1.cont foreground was implemented. The final version will be released in an upcoming release!
Implemented in Version	V3.1.0.0

Ticketnumber	1482
Core Architecture	all
Compiler	all
Variant	all
Description	**Provide an API to trace an event from user mode only when T1.flex is enabled.**
Notes	
Implemented in Version	V3.1.0.0

Ticketnumber	1500
Core Architecture	ARM7R
Compiler	all
Variant	all
Description	**Extend T1.flex for the ARM Cortex-R to support all Cortex-R processors.**
Notes	
Implemented in Version	V3.1.0.0

Ticketnumber	1617
Core Architecture	all
Compiler	all
Variant	all
Description	**Update 'T1 Prepare for Integration Guide' for T1-TARGET-SW V3.1.0.0.**
Notes	
Implemented in Version	V3.1.0.0

Ticketnumber	1677
Core Architecture	all
Compiler	all
Variant	all
Description	**Run-/Compile-time check of T1_commsCoreOffset.**
Notes	Details: The T1 communication core must be configured to the core the communication stack is actually running on. This is now checked for the RX side.
Implemented in Version	V3.1.0.0

Ticketnumber	1581
Core Architecture	all
Compiler	all
Variant	all
Description	**Optimize execution time of T1_projGen.pl if runnables header is not required.**
Notes	
Implemented in Version	V3.1.0.0

Ticketnumber	1405
Core Architecture	all
Compiler	all
Variant	all
Description	**Use multi-step init only for CERT releases.**
Notes	Details: In future, non-certified releases of T1-TARGET-SW, the T1_InitExtra1/2/3 will have no effect and possibly be removed.
Implemented in Version	V2.6.0.0

Ticketnumber	1404
Core Architecture	all
Compiler	all
Variant	all
Description	**API for access to T1.cont results on the target.**
Notes	Details: This functions are only present in certified releases of T1-TARGET-SW. Please contact support@gliwa.com for more details!
Implemented in Version	V2.6.0.0

Ticketnumber	1365
Core Architecture	all
Compiler	all
Variant	all
Description	**Add option to avoid .t0p being generated.**
Notes	Details: If the configuration parameter `noRefT0p` in the inv file is set to true, no T0p file is generated.
Implemented in Version	V2.6.0.0

Ticketnumber	1279
Core Architecture	all
Compiler	all
Variant	all
Description	**Merge comN and T1.base libs.**
Notes	Details: The communication libraries (comN) are now integrated into T1.base so there is no need to link additional comX library. Please contact support@gliwa.com for integration details!
Implemented in Version	V2.6.0.0

Ticketnumber	1111
Core Architecture	all
Compiler	all
Variant	all
Description	**Add T1-TARGET-SW API function to start tracing.**
Notes	Details: A function T1_InitTraceBuffer() to start tracing on the target was introduced. This function is only present in certified releases of T1-TARGET-SW. Please contact support@gliwa.com for more details!
Implemented in Version	V2.6.0.0

Ticketnumber	1402
Core Architecture	V850E3
Compiler	GHS
Variant	multicore
Description	**Support RH850 E2 core.**
Notes	Hint: Define 'T1_GetCoreIdOffset' explicitly before including T1_AppInterface.h so that you do not fall back on the default implementation (RH850 E2 has a different core ID register!
Implemented in Version	V2.5.8.1

Ticketnumber	1407
Core Architecture	V850E3
Compiler	all
Variant	multicore
Description	**RH850 T1.flex multi-core (not core-specific) handler is different for RH850E2.**
Notes	Hint: Use alternative exception handler T1_OuterExceptionHandlerG4 for RH850 E2 devices.!
Implemented in Version	V2.5.8.1

Ticketnumber	1383
Core Architecture	TCall
Compiler	all
Variant	all
Description	**Add check that TriCore T1_dcx alignment requirements are actually fulfilled before allowing T1.flex to start.**
Notes	Details: DCX section pointer must be 64-byte aligned, i.e. low 6 bits of address / pointer are clear. This is now checked in T1_Init()!
Implemented in Version	V2.5.8.0

Ticketnumber	1372
Core Architecture	all
Compiler	all
Variant	all
Description	**Support trace buffer larger than or equal to 64KB.**
Notes	
Implemented in Version	V2.5.7.0

Ticketnumber	1359
Core Architecture	all
Compiler	all
Variant	all
Description	**Remove 'TraceCount' from T1_projGen.pl to support T1-HOST-SW V2.5.0.**
Notes	Note: If this deprecated attribute is not removed, T1-HOST-SW issues an information entry.
Implemented in Version	V2.5.6.0

Ticketnumber	1355
Core Architecture	all
Compiler	all
Variant	all
Description	**Perl Script(.pm module) for Microsar_2017_Architecture should read information of Cat1 ISRs too.**
Notes	
Implemented in Version	V2.5.6.0

Ticketnumber	1346
Core Architecture	all
Compiler	all
Variant	all
Description	**Issue error if T1_GET_TRACE_TIME needs to be defined in T1_AppInterface.h.**
Notes	
Implemented in Version	V2.5.6.0

Ticketnumber	1331
Core Architecture	all
Compiler	all
Variant	all
Description	**Document how T1_GET_TRACE_TIME shall be implemented by the integrator.**
Notes	
Implemented in Version	V2.5.6.0

Ticketnumber	1340
Core Architecture	all
Compiler	all
Variant	all
Description	**Write the T1-TARGET-SW release version number into each header file comment.**
Notes	
Implemented in Version	V2.5.5.0

Ticketnumber	1324
Core Architecture	all
Compiler	all
Variant	all
Description	**Access sync timer via defined macro or function rather than direct read from memory.**
Notes	
Implemented in Version	V2.5.4.0

Ticketnumber	1296
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_TRACE_ACT_EVENT_AND_CROSS_CORE_ACT and T1_CROSS_CORE_ACT can't be defined at the same time.**
Notes	Do not define T1_TRACE_ACT_EVENT_AND_CROSS_CORE_ACT.
Implemented in Version	V2.5.3.0

Ticketnumber	1285
Core Architecture	all
Compiler	all
Variant	all
Description	**Allow exact timer width to be specified.**
Notes	
Implemented in Version	V2.5.3.0

Ticketnumber	1252
Core Architecture	all
Compiler	all
Variant	all
Description	**Enable T1_ContBgHandler re-enty check also for production build.**
Notes	
Implemented in Version	V2.5.2.0

Ticketnumber	24
Core Architecture	all
Compiler	all
Variant	all
Description	**Added first version of T1-TARGET-SW API documentation.**
Notes	
Implemented in Version	V2.5.1.0

Ticketnumber	1253
Core Architecture	all
Compiler	all
Variant	all
Description	**Implement spinlocks via callbacks in T1_config.c.**
Notes	The user can implement a project specific version of the spinlocks.
Implemented in Version	V2.5.0.0

Ticketnumber	1198
Core Architecture	all
Compiler	all
Variant	all
Description	**Allow trace timer to be read using a macro (T1_GET_TRACE_TIME).**
Notes	This enables the user to use any timer as trace timer and can save a lot of overhead e.g. 40% on the AURIX by using the performance counters.
Implemented in Version	V2.5.0.0

Ticketnumber	1181
Core Architecture	all
Compiler	all
Variant	multicore
Description	**Run calibration code in such a way as to minimize any multicore resource conflicts.**
Notes	Workaround: Serialize calls to T1_CONT_CALIBRATE_OVERHEADS_NOSUSP_PC until T1 is enhanced to do this.
Implemented in Version	V2.3.9.0

Ticketnumber	1174
Core Architecture	MPC5xxx
Compiler	all
Variant	all
Description	**T1 Integration Guide: remove requirement of tail-call optimization for T1_PreExceptionHandler.**
Notes	
Implemented in Version	V2.3.9.0

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Ticketnumber	1029
Core Architecture	all
Compiler	all
Variant	all
Description	**T1 Integration Guide: max. task ID for T1_STOP_START.**
Notes	
Implemented in Version	V2.3.9.0

Ticketnumber	1184
Core Architecture	all
Compiler	all
Variant	all
Description	**Add new API calls T1_TraceStartNoAct... for optimized tracing the start of ISRs (or tasks) that certainly have no traced activation and T1_TraceStartAct... for tracing the start of ISRs with no traced activation but where the activation time is known.**
Notes	
Implemented in Version	V2.3.8.0

Ticketnumber	1142
Core Architecture	TCall
Compiler	all
Variant	all
Description	**Check and restore OCDS watchdog setting if disabled by starting T1.flex**
Notes	
Implemented in Version	V2.3.5.0

Ticketnumber	1115
Core Architecture	all
Compiler	all
Variant	all
Description	**Avoid missing the definiton of T1_WAIT_RESUME**
Notes	
Implemented in Version	V2.3.3.0

Ticketnumber	1031
Core Architecture	TC1.6.1
Compiler	GCC
Variant	all
Description	**Use the built-in HighTec macros to identify the AURIX (as opposed to other non-AURIX TriCores).**
Notes	
Implemented in Version	V2.3.0.1

Ticketnumber	1006
Core Architecture	all
Compiler	all
Variant	all
Description	**Generate optionally StaticRunnableID with T1_projGen.pl**
Notes	
Implemented in Version	V2.3.0.0

Ticketnumber	841
Core Architecture	all
Compiler	all
Variant	multicore
Description	**Support up to 15 cores**
Notes	
Implemented in Version	V2.3.0.0

Ticketnumber	445
Core Architecture	all
Compiler	all
Variant	all
Description	**T1.cont shall support also ECC tasks that both terminate and wait**
Notes	
Implemented in Version	V2.3.0.0

Ticketnumber	1022
Core Architecture	all
Compiler	GCC
Variant	multicore
Description	**Use HighTec core-specific code and data section flags to support HighTec multi-core linking concept, cf. "CORE_SEC".**
Notes	
Implemented in Version	V2.3.0.0

5 List of Known Issues

Ticketnumber	1919
Core Architecture	all
Compiler	all
Variant	all
Description	**T1.cont does not check for overflow of stopwatch duration or overflow of focus duration or cross-core duration.**
Notes	Workaround: Check results of long-running measurements carefully.
Implemented in Version	

Ticketnumber	464
Core Architecture	all
Compiler	all
Variant	all
Description	**DCA problems with interrupted address.**
Notes	This is as a matter of principle a limitation of the DCA functionality.
Implemented in Version	

Ticketnumber	746
Core Architecture	MPC5xxx
Compiler	all
Variant	all
Description	**MPC5xxx SWC exception on successive addresses.**
Notes	This could not yet be reproduced and is subject of further investigation.
Implemented in Version	

Ticketnumber	846
Core Architecture	all
Compiler	all
Variant	all
Description	**T1_TraceData disables interrupts but not T1.flex.**
Notes	Please ask support@gliwa.com for a workaround when using T1_TraceData().
Implemented in Version	

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