User Manual

for S32K1 MCL Driver

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Chapter 1

Revision History

Revision	Date	Author	Description
1.0	24.02.2022	NXP RTD Team	Prepared for release RTD S32K1 Version 1.0.1

Chapter 2

Introduction

- Supported Derivatives
- Overview
- About This Manual
- Acronyms and Definitions
- Reference List

This User Manual describes NXP Semiconductor MCL for *platform*. MCL driver configuration parameters and deviations from the specification are described in Driver chapter of this document. MCL driver requirements and APIs are described in the MCL driver software specification document.

2.1 Supported Derivatives

The software described in this document is intended to be used with the following microcontroller devices of NXP Semiconductors:

- s32k116_qfn32
- s32k116_lqfp48
- $s32k118_lqfp48$
- s32k118_lqfp64
- $s32k142_lqfp48$
- $s32k142_lqfp64$
- s32k142_lqfp100
- $s32k142w_lqfp48$
- s32k142w_lqfp64
- s32k144 lqfp48

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- s32k144_lqfp64
- s32k144_lqfp100
- s32k144_mapbga100
- s32k144w lqfp48
- s32k144w_lqfp64
- s32k146_lqfp64
- s32k146_lqfp100
- s32k146_mapbga100
- $s32k146_lqfp144$
- s32k148_lqfp100
- s32k148_mapbga100
- $s32k148_lqfp144$
- s32k148_lqfp176

All of the above microcontroller devices are collectively named as S32K1.

2.2 Overview

AUTOSAR (AUTomotive Open System ARchitecture) is an industry partnership working to establish standards for software interfaces and software modules for automobile electronic control systems.

AUTOSAR:

- paves the way for innovative electronic systems that further improve performance, safety and environmental friendliness.
- is a strong global partnership that creates one common standard: "Cooperate on standards, compete on implementation".
- is a key enabling technology to manage the growing electrics/electronics complexity. It aims to be prepared for the upcoming technologies and to improve cost-efficiency without making any compromise with respect to quality.
- facilitates the exchange and update of software and hardware over the service life of the vehicle.

2.3 About This Manual

This Technical Reference employs the following typographical conventions:

- Boldface style: Used for important terms, notes and warnings.
- *Italic* style: Used for code snippets in the text. Note that C language modifiers such "const" or "volatile" are sometimes omitted to improve readability of the presented code.

Notes and warnings are shown as below:

Note

This is a note.

Warning

This is a warning

2.4 Acronyms and Definitions

Term	Definition	
API	Application Programming Interface	
ASM	Assembler	
BSMI	Basic Software Make file Interface	
CAN	Controller Area Network	
C/CPP	C and C++ Source Code	
CS	Chip Select	
CTU	Cross Trigger Unit	
DEM	Diagnostic Event Manager	
DET	Development Error Tracer	
DMA	MA Direct Memory Access	
ECU	Electronic Control Unit	
FIFO	First In First Out	
LSB	Least Signifigant Bit	
MCU	Micro Controller Unit	
MIDE	Multi Integrated Development Environment	
MSB	Most Significant Bit	
N/A	Not Applicable	
RAM	Random Access Memory	
SIU	Systems Integration Unit	
SWS	Software Specification	
VLE	Variable Length Encoding	
XML	Extensible Markup Language	

2.5 Reference List

#	${f Title}$	Version
1	S32K1xx Series Reference Manual	Rev. 14, 09/2021
2	Errata S32K116_0N96V	Rev. 22/OCT/2021
3	Errata S32K118_0N97V	Rev. 22/OCT/2021
4	Errata S32K142_0N33V	Rev. 22/OCT/2021
5	Errata S32K144_0N57U	Rev. 22/OCT/2021
6	Errata S32K144W_0P64A	Rev. 22/OCT/2021
7	Errata S32K146_0N73V	Rev. 22/OCT/2021
8	Errata S32K148_0N20V	Rev. 22/OCT/2021
9	S32K1xx Data Sheet	Rev. 14, 08/2021

Chapter 3

Driver

- Requirements
- Driver Design Summary
- Hardware Resources
- Deviations from Requirements
- Driver Limitations
- Driver usage and configuration tips
- Runtime errors
- Symbolic Names Disclaimer

3.1 Requirements

Requirements for this driver are detailed in the Driver Software Specification document (See Table Reference List).

For CDD: MCL Driver is a Complex Device Driver (CDD), so there are no requirements regarding this module.

It has vendor-specific requirements and implementation.

3.2 Driver Design Summary

The Mcl Driver controls the DMA(Direct Memory Access) and CACHE modules of the S32K1 device. It provides the following features:

- Configuration and initialization of the DMA.
- Configuration and initialization of the CACHE.
- Handling of the DMA interrupt requests.
- DMA Normal Transfer Mode and Scatter/Gather Mode.

Driver

3.3 Hardware Resources

The Mcl Driver consists of:

- 1. A DMA Peripheral which has 1 Hardware Instance with 4 Hardware Channels for S32K11X and 16 Hardware Channels for S32K14X.
- 2. A CACHE Memory is Local Memory Controller (LMEM).

3.4 Deviations from Requirements

The driver deviates from the Mcl Driver Software Specification in some places.

The table Status Column Description identifies the requirements that are not fully implemented, implemented differently, or out of scope for the Mcl Driver.

The table Mcl Requirements Deviations provides the "Status" column description.

Term	Definition	
N/S	Not In Scope	
N/F	Not Fully Implemented	
N/I	Not Implemented	

3.4.0.0.1 Status Column Description

Requirement	Status	Description	Notes
None	None	None	None

3.4.0.0.2 Mcl Requirements Deviations Files Mcl_<VariantName>_PBcfg.c and Mcl_<Variant←Name>_PBcfg.h will contain the definitions for all parameters that are variant aware, independent of the configuration class that will be selected (PC, LT, PB).

Files Mcl_Cfg.c and Mcl_Cfg.h will contain the definitions for all parameters that are not variant aware.

3.5 Driver Limitations

The Mcl Driver has the following limitations:

• When DMA is used with CACHE enabled, the user shall Invalidate/Clean the CACHE in order to synchronize the transferred data.

- When using CACHE Invalidate and Clean functionalities, the user shall take into consideration that all variables that reside in the cache, are affected.
- The Cache Invalidate function need to be called before Cache Enable function is called (make sure that Cache wasn't enabled before).
- The Cache Clean function need to be called before Cache Disable function is called.
- The DMA Driver shall have the Source Address and Destination Address configured at runtime. These two parameters are not available in the configurator.
- When the DMA transfer has errors, user must call Mcl_SetDmaChannelCommand/Dma_Ip_SetLogic← ChannelCommand function to clear error state and error status.
- When using Mcl_CacheDisable/Cache_Ip_Disable and Mcl_CacheInvalidate/Cache_Ip_Invalidate, the stack shall be put into non-cacheable memory.
- When using Virtual Address Mapping feature, the user shall handle the linker file to avoid the memory address
 is invalid.
- For DMA hardware version 2, the ActiveId is not available in CR register.

3.6 Driver usage and configuration tips

3.6.1 MCAL MCL DMA migration guide to RTD MCL

3.6.1.1 Introduction

The RTD MCL DMA Driver brings a Generic Interface, to help the User in application development across multiple SoCs. The Generic Interface consists of software functions that are fully configurable using User defined configurations. The Generic Interface is structured into four function groups:

- 1. Set Command Functions
- 2. Get Status Functions
- 3. Set List Functions
- 4. Get Information (Parameter) Functions

The Set Command Functions shall trigger actions specific to the invoked Logic Entity. For example, the Logic Dma Instance shall be commanded to: "Stop execution", "Stop execution with error signaling", "Pause execution" or "Resume execution".

The Get Status Functions shall read the status specific to the invoked Logic Entity. For example, the Logic Dma Instance shall return: "Hardware Errors specific to the IP", "The Active Channel Id" and "Active Status".

The Set List Functions shall configure a user defined list of settings for the invoked Logic Entity. For example, the Logic Dma Channel shall be configurable with the Transfer List of Parameters like: "Source Address", " \leftarrow Destination Address", "Source Signed Offset", "Destination Signed Offset", "Major Loop Count", etc... For the specific ScatterGather mode, the additional Logic Element parameter specifies the Software TCD that shall be loaded with the ScatterGather List of Parameters.

The Get Parameter Functions shall return specific parameter value. For example, the Logic Dma Channel shall return the "Destination Address" value, which contains the last accessed destination memory location.

Driver

3.6.1.2 TRESOS Configuration

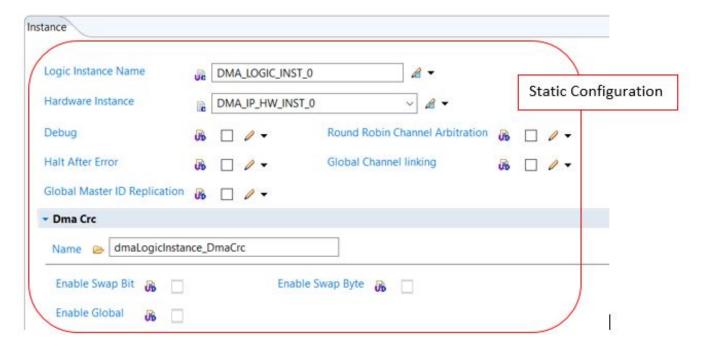


Figure 3.1 DMA Logic Instance

The DMA Logic Instance configuration presented in Figure 3.1 is static, thus it can't be changed dynamically during runtime. The "Logic Instance Name" represents the Handler(Tag) used with the DMA API. The Handler(Tag) is set by the User for the specific Application; for example the "DMA_LOGIC_INSTANCE_0" shall be changed to "DMA_LOGIC_INST_COMMUNICATION".

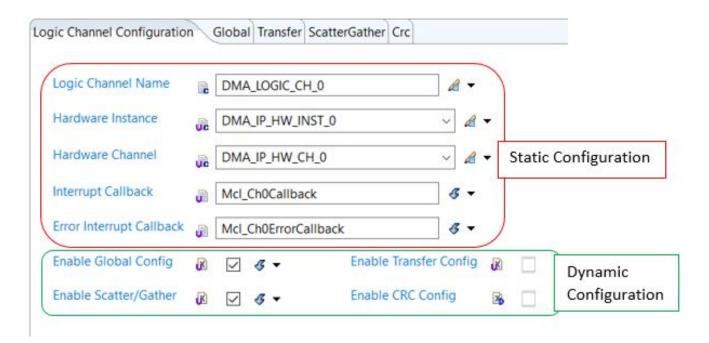


Figure 3.2 DMA Logic Channel

The DMA Logic Channel configuration in Figure 3.2 is composed of static and dynamic settings.

- 1. The static configuration is needed in order for the DMA Logic Channel to be created and used. The static configuration allocates resources for the DMA Logic Channel basic configuration. The static configuration can't be changed during runtime. The "Logic Channel Name" represents the Handler(Tag) used with the DMA API. The Handler(Tag) is set by the User based on the Application; For example the "DMA_LOGIC_CH_0" shall be changed to "DMA_CH_CANO_RX" or "DMA_LOGIC_CH_SPI2_TX".
- 2. The dynamic configuration can be set in TRESOS and shall be automatically loaded in the DMA Logic Channel at initialization time. By enabling a checkbox, the respective configuration option is enabled and system memory is allocated during generation. The dynamic configuration can be set during runtime by using the specific API. By disabling a checkbox, the respective configuration option is disabled and system memory is not allocated during generation.
- 2.1. The "Enable Global Config" contains settings outside the Transfer Control Descriptor (TCD).
- 2.2. The "Enable Transfer Config" contains settings of the Transfer Control Descriptor (TCD).
- 2.3. The "Enable Scatter/Gather" contains settings that extend the "Transfer Config" by creating Software Transfer Control Descriptors (STCDs).
- 2.4. The "Enable CRC Config" contains settings for the DMA Logic Channel CRC computation functionality.

Note: The DMA Logic Channel can be configured in "Transfer Mode" or "Scatter/Gather Mode", thus only one of the 2 configurations can be set at any time. During runtime, the DMA Logic Channel can be configured between the 2 modes by calling the "SetTransfer" or "SetScatterGather" API.

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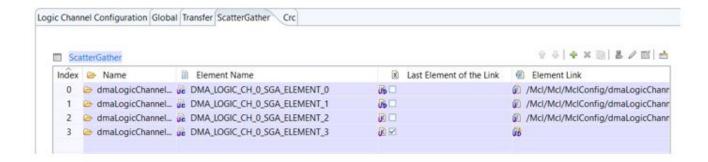


Figure 3.3 DMA Logic Channel – ScatterGather Element List

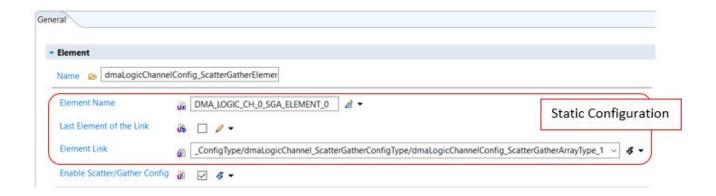


Figure 3.4 DMA Logic Channel – ScatterGather Element Configuration

The DMA Logic Channel ScatterGather Element list (Figure 3.3) shall be loaded with the required number of elements. Each element represents a STCD and is part of a linked list of elements.

The DMA Logic Channel ScatterGather Element Configuration (Figure 3.4) contains the static configuration of the element.

- 1. The "Element Name" represents the Handler (Tag) (static configuration).
- 2. The "Last Element of the Link" sets the element as the last link element (static configuration).
- 3. The "Element Link" points to the next element of the link (static configuration).
- 4. The "Enable Scatter/Gather Config" enables the element configuration.

Note1: Element can't be added during runtime. The elements are allocated resources during generation (System memory for STCDs and configuration if set). The element linkage can't be changed during runtime.

Note2: The DMA Logic Channel ScatterGather Element List can be configured to contain multiple independent chained lists. During runtime, the Logic Channel can be assigned a different Chained List.

Note3: Each Element is allocated 32 bytes of memory space aligned to 32 bytes, representing the STCD. Additionaly, if the configuration is enabled from TRESOS, additional 60 bytes are allocated.

3.6.2 Channel State Machine

3.6.2.1 MCL Driver

The MCL DMA Driver runs based on the presented State Machine Diagram.

The MCL DMA State Machine applies to the MCL DMA Channels and it contains 5 States.

The State Machine supports the following 21 Transitions:

```
T0: Hardware Reset
T1: Mcl_Init() with DMA Channel no Transfer or Scatter/Gather generated configurations
T2: Mcl_DeInit()
T3: Mcl_SetDmaChannelTransferList()
T4: Mcl_Init() with DMA Channel Transfer generated configuration
T5: Mcl_SetDmaChannelScatterGatherList() + Mcl_SetDmaChannelScatterGatherConfig()
T6: Mcl_SetDmaChannelTransferList()
T7: Mcl_SetDmaChannelScatterGatherList() + Mcl_SetDmaChannelScatterGatherConfig()
T8: Mcl_Init() with DMA Channel Scatter/Gather generated configuration
T9: Detection of channel error
T10: Mcl_SetDmaInstanceCommand(CHANNEL, MCL_DMA_CH_ACK_ERROR)
T11: Detection of channel error
T12: Mcl_DeInit()
T13: Mcl_DeInit()
T14: Detection of channel error
T15: Detection of channel error
T16: Mcl_DeInit()
T17: Mcl_DeInit()
T18: Mcl_SetDmaChannelCommand(CHANNEL, MCL_DMA_CH_ACK_ERROR)
T19: Mcl_SetDmaChannelTransferList()
T20: Mcl_SetDmaChannelScatterGatherList() + Mcl_SetDmaChannelScatterGatherConfig()
T21: Detection of channel error
```

When the DMA Driver detects a software or hardware error for the Logic Channel, it shall enter the "MCL_DM \leftarrow A_CH_ERROR_STATE".

To exit from the "MCL DMA CH ERROR STATE", the application shall use the specified transitions.

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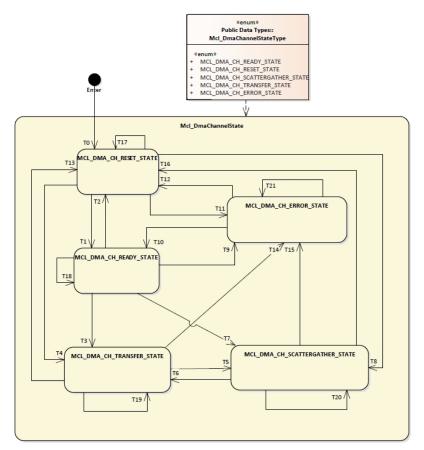


Figure 3.5 MCL DMA Channel State Machine

3.6.2.2 DMA Driver

The DMA IP Driver runs based on the presented State Machine Diagram.

The DMA State Machine applies to the DMA Logic Channels and it contains 5 States.

The State Machine supports the following 21 Transitions:

T0: Hardware Reset

T1: Dma_Ip_LogicChannelInit() with no Transfer or Scatter/Gather generated configurations

T2: Dma_Ip_LogicChannelDeinit()

T3: Dma_Ip_SetLogicChannelTransferList()

T4: Dma_Ip_LogicChannelInit() with Transfer generated configuration

T5: Dma_Ip_SetLogicChannelScatterGatherList() + Dma_Ip_SetLogicChannelScatterGatherConfig()

T6: Dma_Ip_SetLogicChannelTransferList()

T7: Dma_Ip_SetLogicChannelScatterGatherList() + Dma_Ip_SetLogicChannelScatterGatherConfig()

```
T8: Dma_Ip_LogicChannelInit() with Scatter/Gather generated configuration

T9: Detection of channel error

T10: Dma_Ip_SetLogicChannelCommand(CHANNEL, DMA_IP_CH_CLEAR_ERROR)

T11: Detection of channel error

T12: Dma_Ip_LogicChannelDeinit()

T13: Dma_Ip_LogicChannelDeinit()

T14: Detection of channel error

T15: Detection of channel error

T16: Dma_Ip_LogicChannelDeinit()

T17: Dma_Ip_LogicChannelDeinit()

T18: Dma_Ip_LogicChannelDeinit()

T19: Dma_Ip_SetLogicChannelCommand(CHANNEL, DMA_IP_CH_CLEAR_ERROR)

T19: Dma_Ip_SetLogicChannelTransferList()

T20: Dma_Ip_SetLogicChannelScatterGatherList() + Dma_Ip_SetLogicChannelScatterGatherConfig()

T21: Detection of channel error
```

When the DMA Driver detects a software or hardware error for the Logic Channel, it shall enter the "DMA_IP_ \leftarrow CH_ERROR_STATE".

To exit from the "DMA_IP_CH_ERROR_STATE", the application shall use the specified transitions.

S32K1 MCL Driver

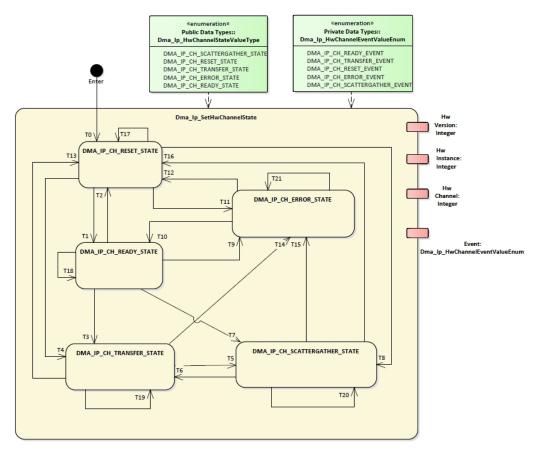


Figure 3.6 DMA IP Channel State Machine

3.7 Runtime errors

The driver generates the following DET errors at runtime.

Function	Error Code	Condition triggering the error
Mcl_Init()	MCL_E_UNINIT	API is called with a NULL pointer
		as parameter.
Mcl_DeInit()	MCL_E_PARAM_CONFIG	API is called with invalid configura-
"		tion parameter.
Mcl_DeInit()	MCL_E_UNINIT	API is called with a NULL pointer
		as parameter.
$Mcl_SetDmaInstanceCommand()$	MCL_DET_DMA_INSTANCE←	API is called with invalid instance
	_COMMAND	command.
Mcl_GetDmaInstanceStatus()	MCL_E_INVALID_INSTANCE	API is called with invalid instance.
Mcl_SetDmaChannelCommand()	MCL_E_INVALID_CHANNEL	API is called with invalid channel.
Mcl_SetDmaChannelCommand()	MCL_E_INVALID_COMMAND	API is called with invalid command.
Mcl_GetDmaChannelStatus()	MCL_E_INVALID_CHANNEL	API is called with invalid channel.
${\bf Mcl_SetDmaChannelGlobalList()}$	MCL_E_INVALID_CHANNEL	API is called with invalid channel.

Function	Error Code	Condition triggering the error
${\bf Mcl_SetDmaChannelGlobalList()}$	MCL_E_INVALID_PARAME↔ TER	API is called with invalid parame-
	-	ter.
Mcl_SetDmaChannelTransferList()	MCL_E_INVALID_CHANNEL	API is called with invalid channel.
Mcl_SetDmaChannelTransferList()	MCL_E_INVALID_PARAME←	API is called with invalid parame-
	TER	ter.
$Mcl_SetDmaChannelScatter \leftarrow$	MCL_E_INVALID_CHANNEL	API is called with invalid channel.
GatherList()		
Mcl_SetDmaChannelScatter←	MCL_E_INVALID_PARAME←	API is called with invalid parame-
GatherList()	TER	ter.
Mcl_GetDmaChannelParam()	MCL_E_INVALID_CHANNEL	API is called with invalid channel.
Mcl_GetDmaChannelParam()	MCL_E_INVALID_PARAME←	API is called with invalid parame-
V	TER	ter.
$Mcl_SetDmaChannelScatter \leftarrow$	MCL_E_INVALID_CHANNEL	API is called with invalid channel.
GatherConfig()		
Mcl_SetDmaChannelCrcList()	MCL_E_INVALID_CHANNEL	API is called with invalid channel.
Mcl_CacheEnable()	MCL_E_INVALID_INSTANCE	API is called with invalid instance.
Mcl_CacheDisable()	MCL_E_INVALID_INSTANCE	API is called with invalid instance.
Mcl_CacheInvalidate()	MCL_E_INVALID_INSTANCE	API is called with invalid instance.
Mcl_CacheClean()	MCL_E_INVALID_INSTANCE	API is called with invalid instance.
Mcl_CacheInvalidateByAddr()	MCL_E_INVALID_INSTANCE	API is called with invalid instance.
Mcl_CacheCleanByAddr()	MCL_E_INVALID_INSTANCE	API is called with invalid instance.
Mcl_CacheCleanByAddr()	MCL_E_INVALID_INSTANCE	API is called with invalid instance.

3.8 Symbolic Names Disclaimer

All containers having symbolicNameValue set to TRUE in the AUTOSAR schema will generate defines like:

```
#define <Mip>Conf_<Container_ShortName>_<Container_ID>
```

For this reason it is forbidden to duplicate the names of such containers across the RTD configurations or to use names that may trigger other compile issues (e.g. match existing #ifdefs arguments).

Chapter 4

Tresos Configuration Plug-in

This chapter describes the Tresos configuration plug-in for the driver. All the parameters are described below.

- Module Mcl
 - Container MclGeneral
 - * Parameter MclEnableDemReportErrorStatus
 - $* \ Parameter \ MclEnableDevErrorDetect \\$
 - * Parameter Mcl_VersionInfoApi
 - * Parameter MclEnableUserModeSupport
 - * Parameter MclEnableVirtualAddressMappingSupport
 - * Container MclDma
 - · Parameter MclEnableDma
 - * Container MclCache
 - · Parameter MclEnableCache
 - · Parameter MclCacheTimeoutValue
 - · Parameter MclCacheTimeoutMethod
 - * Container MclTrgMux
 - · Parameter MclEnableTrgMux
 - * Container MclFlexioCommon
 - · Parameter MclEnableFlexioCommon
 - * Container MclFtmCommon
 - · Parameter Mcl_FtmCommonTimebase
 - Container MclConfig
 - * Container MclVirtualMemorySection
 - · Parameter MclVirtualAddressStart
 - · Parameter MclVirtualAddressEnd
 - · Parameter MclPhysicalAddressStart
 - · Parameter MclPhysicalAddressEnd
 - * Container MclDemEventParameterRefs
 - · Reference MCL_E_TIMEOUT_FAILURE
 - * Container dmaLogicInstance ConfigType
 - · Parameter dmaLogicInstance_IdName
 - · Parameter dmaLogicInstance hwId

- · Parameter dmaLogicInstance enDebug
- · Parameter dmaLogicInstance_enRoundRobin
- \cdot Parameter dmaLogicInstance_enHaltAfterError
- · Parameter dmaLogicInstance enChLinking
- * Container dmaLogicChannel Type
 - · Parameter dmaLogicChannel_LogicName
 - · Parameter dmaLogicChannel HwInstId
 - · Parameter dmaLogicChannel_HwChId
 - · Parameter dmaLogicChannel_InterruptCallback
 - \cdot Parameter dmaLogicChannel_ErrorInterruptCallback
 - · Parameter dmaLogicChannel_EnableGlobalConfig
 - · Parameter dmaLogicChannel_EnableTransferConfig
 - · Parameter dmaLogicChannel_EnableScatterGather
 - · Container dmaLogicChannel_ConfigType
 - · Container dmaLogicChannel GlobalConfigType
 - $\cdot \quad Container \ dmaLogicChannelConfig_GlobalRequestType$
 - · Parameter dmaGlobalRequest enDmamuxTrigger
 - · Parameter dmaGlobalRequest_enDmamuxSource
 - · Parameter dmaGlobalRequest Dmamux0HwRequest
 - · Parameter dmaGlobalRequest_enDmaRequest
 - · Container dmaLogicChannelConfig GlobalInterruptType
 - $\cdot \ \ Parameter \ dmaGlobalInterrupt_enDmaErrorInterrupt \\$
 - · Container dmaLogicChannelConfig GlobalPriorityType
 - · Parameter dmaGlobalPriority_LevelPriority
 - · Parameter dmaGlobalPriority enPreemption
 - · Parameter dmaGlobalPriority_disPreempt
 - · Container dmaLogicChannel TransferConfigType
 - · Container dmaLogicChannelConfig TransferControlType
 - · Parameter dmaLogicChannelConfig enStart
 - · Parameter dmaLogicChannelConfig_enDmaMajorInterrupt
 - · Parameter dmaLogicChannelConfig enDmaHalfMajorInterrupt
 - · Parameter dmaLogicChannelConfig disDmaAutoHwReq
 - · Parameter dmaLogicChannelConfig bandwidthControl
 - · Parameter dmaLogicChannelConfig_ScatterGatherAddressType
 - · Parameter dmaLogicChannelConfig DestinationStoreAddressType
 - $\cdot \quad Container \ dmaLogicChannelConfig_TransferSourceType$
 - · Parameter dmaLogicChannelConfig SourceAddressType
 - · Parameter dmaLogicChannelConfig_SourceSignedOffsetType
 - · Parameter dmaLogicChannelConfig SourceLastAddressAdjustmentType
 - · Parameter dmaTransferConfig TransferSizeType
 - · Parameter dmaLogicChannelConfig SourceModuloType
 - · Container dmaLogicChannelConfig_TransferDestinationType
 - · Parameter dmaLogicChannelConfig DestinationAddressType
 - · Parameter dmaLogicChannelConfig DestinationSignedOffsetType
 - · Parameter dmaLogicChannelConfig DestinationLastAddressAdjustmentType
 - · Parameter dmaTransferConfig_TransferSizeType
 - · Parameter dmaLogicChannelConfig_DestinationModuloType

Tresos Configuration Plug-in

- · Container dmaLogicChannelConfig_TransferMinorLoopType
- · Parameter dmaLogicChannelConfig_enSourceOffset
- · Parameter dmaLogicChannelConfig enDestinationOffset
- · Parameter dmaLogicChannelConfig_OffsetValueType
- · Parameter dmaLogicChannelConfig enMinorLoopLinkCh
- · Parameter dmaLogicChannelConfig_MinorLoopSizeType
- · Reference dynamic dmaLogicChannelConfig MinorLoopLinkChValueType
- · Container dmaLogicChannelConfig_TransferMajorLoopType
- $\cdot \quad Parameter \; dmaLogicChannelConfig_enMajorLoopLinkCh$
- $\cdot \ \, {\bf Parameter} \ {\bf dmaLogicChannelConfig_MajorLoopCountType}$
- $\cdot \ \ Reference \ dynamic_dmaLogicChannelConfig_MajorLoopLinkChValueType$
- · Container dmaLogicChannel_ScatterGatherConfigType
- · Container dmaLogicChannelConfig_ScatterGatherArrayType
- $\cdot \quad Container \ dmaLogic Channel Config_Scatter Gather Element Config Type$
- $\cdot \ \ Parameter \ dmaLogicChannelConfig_ScatterGatherElementNameType$
- $\cdot \ \, Parameter \ dmaLogicChannelConfig_LastElementLink_ScatterGatherType$
- · Parameter dmaLogicChannelConfig enScatterGatherConfig
- · Reference dynamic_dmaLogicChannelConfig_BasicElementLink_ScatterGatherType
- · Container dmaLogicChannelConfig TransferControlType
- · Parameter dmaLogicChannelConfig_enStart
- · Parameter dmaLogicChannelConfig enDmaMajorInterrupt
- · Parameter dmaLogicChannelConfig enDmaHalfMajorInterrupt
- · Parameter dmaLogicChannelConfig disDmaAutoHwReq
- · Parameter dmaLogicChannelConfig_bandwidthControl
- · Parameter dmaLogicChannelConfig ScatterGatherAddressType
- $\cdot \ \ Parameter \ dmaLogic Channel Config_Destination Store Address Type$
- · Container dmaLogicChannelConfig TransferSourceType
- · Parameter dmaLogicChannelConfig_SourceAddressType
- · Parameter dmaLogicChannelConfig SourceSignedOffsetType
- $\cdot \ \, Parameter \ dmaLogicChannelConfig_SourceLastAddressAdjustmentType$
- · Parameter dmaTransferConfig TransferSizeType
- · Parameter dmaLogicChannelConfig_SourceModuloType
- · Container dmaLogicChannelConfig_TransferDestinationType
- · Parameter dmaLogicChannelConfig_DestinationAddressType
- · Parameter dmaLogicChannelConfig DestinationSignedOffsetType
- $\cdot \ \, \mathbf{Parameter} \ dmaLogicChannelConfig_DestinationLastAddressAdjustmentType$
- · Parameter dmaTransferConfig TransferSizeType
- $\cdot \ \ Parameter \ dmaLogicChannelConfig_DestinationModuloType$
- $\cdot \quad Container \ dmaLogicChannelConfig_TransferMinorLoopType$
- · Parameter dmaLogicChannelConfig_enSourceOffset
- · Parameter dmaLogicChannelConfig enDestinationOffset
- · Parameter dmaLogicChannelConfig_OffsetValueType
- · Parameter dmaLogicChannelConfig enMinorLoopLinkCh
- · Parameter dmaLogicChannelConfig MinorLoopSizeType
- · Reference dynamic dmaLogicChannelConfig MinorLoopLinkChValueType
- $\cdot \quad Container \ dmaLogicChannelConfig_TransferMajorLoopType$
- · Parameter dmaLogicChannelConfig enMajorLoopLinkCh

- · Parameter dmaLogicChannelConfig_MajorLoopCountType
- · Reference dynamic_dmaLogicChannelConfig_MajorLoopLinkChValueType
- * Container trgmuxLogicGroup
 - · Parameter trgmuxLogicGroup Name
 - · Parameter trgmuxLogicGroup_Lock
 - $\cdot \ \ Container \ trgmuxLogicTrigger$
 - · Parameter trgmuxLogicTrigger_Name
 - $\cdot \ \ Parameter \ trgmuxLogicTrigger_Output$
 - · Parameter trgmuxLogicTrigger Input
- * Container FlexioCommon
 - · Parameter FlexioMclInstances
 - · Parameter FlexioDebugEnable
 - · Container FlexioMclLogicChannels
 - · Parameter FlexioMclChannelId
 - · Parameter FlexioMclPinId
 - · Parameter FlexioMclAddPinEnable
 - · Parameter FlexioMclAddPinId
 - · Parameter FlexioMclAddChannelEnable
 - · Parameter FlexioMclAddChannelId
- Container CommonPublishedInformation
 - * Parameter ArReleaseMajorVersion
 - * Parameter ArReleaseMinorVersion
 - * Parameter ArReleaseRevisionVersion
 - * Parameter ModuleId
 - * Parameter SwMajorVersion
 - * Parameter SwMinorVersion
 - * Parameter SwPatchVersion
 - * Parameter VendorId

4.1 Module Mcl

Vendor specific: Configuration of the Mcl (MicroController Library) module.

Included containers:

- MclGeneral
- MclConfig
- CommonPublishedInformation

	Property	Value
	type	ECUC-MODULE-DEF
	lowerMultiplicity	1
	upperMultiplicity	1
	postBuildVariantSupport	S32K1 MCL Driver
NXP Semicono	luctors supportedConfigVariants	VARIANT-POST-BUILD, VARIANT-PRE-COMPILE

4.2 Container MclGeneral

Vendor specific: Configuration of general Mcl parameters.

Included subcontainers:

- MclDma
- MclCache
- MclTrgMux
- MclFlexioCommon
- MclFtmCommon

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.3}\quad {\bf Parameter\ MclEnable Dem Report Error Status}$

Enable/Disable the Production Error Reporting (DEM).

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.4 Parameter MclEnableDevErrorDetect

Vendor specific:

Enable/Disable the Development Error Detection (DET).

true: Enabled.

false: Disabled.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.5 Parameter Mcl_VersionInfoApi

Vendor specific: Enables/Disables the get version info API function

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

${\bf 4.6}\quad {\bf Parameter\ MclEnable User Mode Support}$

When this parameter is enabled, the MCL module will adapt to run from User Mode, with the following measures:

b) using 'call trusted function' stubs for all internal function calls that access registers requiring supervisor mode.

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for more information, please see chapter 5.7 User Mode Support in IM

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComingClasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

${\bf 4.7} \quad {\bf Parameter} \ {\bf MclEnable Virtual Address Mapping Support}$

Enable/Disable Virtual Address Mapping support

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.8 Container MclDma

Vendor specific:

Container for the Dma related configuration parameters.

Included subcontainers:

• None

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Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.9 Parameter MclEnableDma

Vendor specific: Enable/Disable DMA support.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.10 Container MclCache

Vendor specific:

Container for the CACHE related configuration parameters.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

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Parameter MclEnableCache 4.11

Vendor specific:

Enable/Disable all CACHE support.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
valueComigCiasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

Parameter MclCacheTimeoutValue 4.12

Set Cache timeout value

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967295
min	0

Parameter MclCacheTimeoutMethod 4.13

Mcl Cache Time out Method

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Configures the timeout method.

Based on this selection a certain timeout method from OsIf will be used in the driver.

Note: If OSIF_COUNTER_SYSTEM or OSIF_COUNTER_CUSTOM are selected make sure the corresponding timer is enabled in OsIf General configuration.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	OSIF_COUNTER_DUMMY
literals	['OSIF_COUNTER_DUMMY', 'OSIF_COUNTER_SYSTEM', 'OSIF_COU⊷ NTER_CUSTOM']

4.14 Container MclTrgMux

Vendor specific:

Container for the TRGMUX related configuration parameters.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.15 Parameter MclEnableTrgMux

Vendor specific: Enable/Disable TRGMUX support.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.16 Container MclFlexioCommon

Vendor specific:

Container for the Flexio Common related configuration parameters.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.17 Parameter MclEnableFlexioCommon

Vendor specific: Enable/Disable Flexio common support.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

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Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.18 Container MclFtmCommon

Vendor specific:

Container for the FTM Common related configuration parameters.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.19 Parameter Mcl_FtmCommonTimebase

Enables/Disables the option to set the a common timebase for multiple FTM modules.

Note:

Note This is an Implementation Specific Parameter. Enabling this feature will allow the use of the Mcl_Select CommonTimebase API

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.20 Container MclConfig

Vendor specific: This container is the base for a multiple configuration set

Included subcontainers:

- $\bullet \quad Mcl Virtual Memory Section$
- $\bullet \quad MclDemEventParameterRefs$
- $\bullet \ \ dmaLogicInstance_ConfigType$
- $\bullet \ \, dmaLogicChannel_Type$
- trgmuxLogicGroup
- FlexioCommon

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.21 Container MclVirtualMemorySection

Vendor specific:

Data to configure Virtual address and Physical address.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	Infinite
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.22 Parameter MclVirtualAddressStart

This parameter represents the Virtual Address Start.

The address must be aligned to 4 bytes.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967295
min	0

4.23 Parameter MclVirtualAddressEnd

This parameter represents the Virtual Address End.

The address must be aligned to 4 bytes.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	255
max	4294967295
min	0

${\bf 4.24} \quad {\bf Parameter\ MclPhysical Address Start}$

This parameter represents the Physical Address Start.

The address must be aligned to 4 bytes.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	4294967295
min	0

4.25 Parameter MclPhysicalAddressEnd

This parameter represents the Physical Address End.

The address must be aligned to 4 bytes.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	255
max	4294967295
min	0

4.26 Container MclDemEventParameterRefs

Container for the references to DemEventParameter elements which shall be invoked using the API Dem_ReportErrorStatus API in case the corresponding error occurs.

The EventId is taken from the referenced DemEventParameter's DemEventId value.

The standardized errors are provided in the container and can be extended by vendor specific error references.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

4.27 Reference MCL_E_TIMEOUT_FAILURE

Reference to configured DEM event to report Timeout failure.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
multiplicity ComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueConnigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	true
destination	/AUTOSAR/EcucDefs/Dem/DemConfigSet/DemEventParameter

${\bf 4.28}\quad {\bf Container~dmaLogicInstance_ConfigType}$

Vendor specific: Configuration of a DMA Instance.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	2
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

${\bf 4.29 \quad Parameter \ dmaLogicInstance_IdName}$

Vendor specific:

Logic Instance Name.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false

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Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	DMA_LOGIC_INST_0

${\bf 4.30} \quad {\bf Parameter~dmaLogicInstance_hwId}$

Vendor specific:

Select the Hardware DMA Instance.

NOTE: This is an Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_HW_INST_0
literals	['DMA_IP_HW_INST_0']

4.31 Parameter dmaLogicInstance_enDebug

Vendor specific:

 $DMA_CR[EDBG].$

Enable Debug.

0 - The assertion of the system debug control input is ignored.

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1 - The assertion of the system debug control input causes the eDMA to stall the start of a new channel.

Executing channels are allowed to complete.

Channel execution will resume when either the system debug control input is negated or the EDBG bit is cleared.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

$Parameter\ dmaLogicInstance_enRoundRobin$ 4.32

Vendor specific:

DMA_CR[ERCA].

Enable Round Robin Channel Arbitration.

- 0 Fixed-priority arbitration is used for channel selection within each group.
- 1 Round-Robin arbitration is used for channel selection within each group.

Note: Implementation Specific Parameter.

	Property	Value
	type	ECUC-BOOLEAN-PARAM-DEF
	origin	NXP
	symbolicNameValue	false
	lowerMultiplicity	1
	upperMultiplicity	1
	postBuildVariantMultiplicity	N/A
	multiplicityConfigClasses	N/A
	postBuildVariantValue	true
	valueConfigClasses S3	VARIANT-POST-BUILD: POST-BUILD 2K1 RMCLT PRIVECOMPILE: PRE-COMPILE
NXP Semiconduc	tQfSfaultValue	false

4.33 Parameter dmaLogicInstance_enHaltAfterError

Vendor specific:

instances.

DMA_CR[HOE] for eDMA2 instances or DMA_CSR[HAE] for eDMA3

Halt On/After Error.

0 - Normal operation.

1 - Any error will cause the HALT bit to be set.

Subsequently, all service requests will be ignored until the HALT bit is

cleared.

Note: Implementation Specific Parameter.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

4.34 Parameter dmaLogicInstance enChLinking

Vendor specific:

DMA_CR[GCLC].

Global Channel Linking Control.

- 0 Channel linking is disabled for all channels.
- 1 Channel linking is available and controlled by each channel's link settings.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

4.35 Container dmaLogicChannel_Type

Vendor specific:

Logic Channel Configuration.

Included subcontainers:

 $\bullet \ \, dmaLogicChannel_ConfigType$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	16
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE

4.36 Parameter dmaLogicChannel_LogicName

Vendor specific:

Logic Channel Name.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	DMA_LOGIC_CH_0

4.37 Parameter dmaLogicChannel_HwInstId

Vendor specific:

Select the Hardware DMA Instance.

NOTE: This is an Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_HW_INST_0
literals	['DMA_IP_HW_INST_0']

4.38 Parameter dmaLogicChannel_HwChId

Vendor specific:

Select the physical eDMA Channel.

NOTE: This is an Implementation Specific Parameter.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_HW_CH_0
literals	

${\bf 4.39} \quad {\bf Parameter~dmaLogicChannel_InterruptCallback}$

Vendor specific:

User callback function to report that the transfer is half or complete depending on

configuration.

NOTE: Use NULL_PTR w/o quotes. If the used string is different from NULL_PTR it will be used as the configured function name.

Property	Value
type	ECUC-FUNCTION-NAME-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NULL_PTR

4.40 Parameter dmaLogicChannel_ErrorInterruptCallback

Vendor specific:

User callback function

NOTE: Use NULL_PTR w/o quotes. If the used string is different from NULL_PTR it will be used as the configured function name.

Property	Value
type	ECUC-FUNCTION-NAME-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	NULL_PTR

4.41 Parameter dmaLogicChannel_EnableGlobalConfig

Vendor specific: Enable and allocate memory for Global Configuration. Global Configuration can be configured during generation time or during runtime.

Note: If the check box is enabled, then memory space is allocated for the configuration.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.42 Parameter dmaLogicChannel_EnableTransferConfig

Vendor specific: Enable and allocate memory for Transfer Configuration. Transfer Configuration can be configured during generation time or during runtime.

Note: If the check box is enabled, then memory space is allocated for the configuration.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.43 \quad Parameter \ dmaLogic Channel_Enable Scatter Gather}$

Vendor specific: Enable and allocate memory for ScatterGather Transfer Mode.

The ScatterGather Transfer Mode shall allocate memory for each Element, comprised of: Element Linkage and Element Software TCD.

The Element allocation can be done only in the configurator.

The Element Configuration can be further enabled for each individual element.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.44 Container dmaLogicChannel_ConfigType

Vendor specific: Logic Channel Configuration.

Included subcontainers:

- $\bullet \ \ dmaLogicChannel_GlobalConfigType$
- $\bullet \ \ dmaLogicChannel_TransferConfigType$
- $\bullet \ \, dmaLogicChannel_ScatterGatherConfigType$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.45 Container dmaLogicChannel_GlobalConfigType

Vendor specific:

Logic Channel Global Configuration.

Included subcontainers:

- dmaLogicChannelConfig_GlobalRequestType
- $\bullet \ \, dmaLogicChannelConfig_GlobalInterruptType$
- dmaLogicChannelConfig_GlobalPriorityType

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.46 Container dmaLogicChannelConfig_GlobalRequestType

Vendor specific:

TCD Request Control.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.47 Parameter dmaGlobalRequest_enDmamuxTrigger

Vendor specific: Enable the Dma Channel Mux Trigger.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.48} \quad {\bf Parameter~dmaGlobalRequest_enDmamuxSource}$

Vendor specific: Enable the Dma Channel Mux Source.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

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Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.49} \quad {\bf Parameter~dmaGlobalRequest_Dmamux0HwRequest}$

Vendor specific: DMAMUX0 Source

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_REQ_MUX0_DISABLED

Property	Value
literals	['DMA_IP_REQ_MUX0_DISABLED', 'DMA_IP_REQ_MUX0_ENET_
	TIMER_CH0_CH3', 'DMA_IP_REQ_MUX0_LPUART0_RX', 'DMA_IP↔
	_REQ_MUX0_LPUART0_TX', 'DMA_IP_REQ_MUX0_LPUART1_RX',
	$ ^{'}DMA_IP_REQ_MUX0_LPUART1_TX', ^{'}DMA_IP_REQ_MUX0_LPU \hookleftarrow \\ ^{'}$
	ART2_RX', 'DMA_IP_REQ_MUX0_LPUART2_TX', 'DMA_IP_REQ
	_MUX0_LPI2C1_RX', 'DMA_IP_REQ_MUX0_LPI2C1_TX', 'DMA_I-
	P_REQ_MUX0_FLEXIO_SHIFTER0', 'DMA_IP_REQ_MUX0_FLEXI
	O_SHIFTER1', 'DMA_IP_REQ_MUX0_FLEXIO_SHIFTER2_SAI1_RX',
	'DMA_IP_REQ_MUX0_FLEXIO_SHIFTER3_SAI1_TX', 'DMA_IP_RE←
	Q_MUX0_LPSPI0_RX', 'DMA_IP_REQ_MUX0_LPSPI0_TX', 'DMA_I
	P_REQ_MUX0_LPSPI1_RX', 'DMA_IP_REQ_MUX0_LPSPI1_TX', 'D↔ MA_IP_REQ_MUX0_LPSPI2_RX', 'DMA_IP_REQ_MUX0_LPSPI2_TX',
	MA_IP_REQ_MUXU_LPSP12_RX, 'DMA_IP_REQ_MUXU_LPSP12_IX, 'DMA_IP_REQ_MUX0_FTM1_CHANNEL_0', 'DMA_IP_REQ_MUX0←
	_FTM1_CHANNEL_1', 'DMA_IP_REQ_MUX0_FTM1_CHANNEL_2',
	DMA_IP_REQ_MUX0_FTM1_CHANNEL_3', 'DMA_IP_REQ_MUX0←
	FTM1 CHANNEL 4', 'DMA IP REQ MUX0 FTM1 CHANNEL 5',
	DMA_IP_REQ_MUX0_FTM1_CHANNEL_6', 'DMA_IP_REQ_MUX0↔
	FTM1 CHANNEL 7', 'DMA IP REQ MUX0 FTM2 CHANNEL 0',
	DMA_IP_REQ_MUX0_FTM2_CHANNEL_1', 'DMA_IP_REQ_MUX0←
	_FTM2_CHANNEL_2', 'DMA_IP_REQ_MUX0_FTM2_CHANNEL_3',
	$\label{eq:channel_4'} \mbox{'DMA_IP_REQ_MUX0_FTM2_CHANNEL_4', 'DMA_IP_REQ_MUX0} \leftarrow$
	_FTM2_CHANNEL_5', 'DMA_IP_REQ_MUX0_FTM2_CHANNEL_6',
	$ ^{\text{'DMA_IP_REQ_MUX0_FTM2_CHANNEL_7'}}, ^{\text{'DMA_IP_REQ_MUX0}} \leftarrow ^{$
	_FTM0_OR_CH0_CH7', 'DMA_IP_REQ_MUX0_FTM3_OR_CH0_CH7',
	'DMA_IP_REQ_MUX0_FTM4_OR_CH0_CH7', 'DMA_IP_REQ_MUX0↔
	_FTM5_OR_CH0_CH7', 'DMA_IP_REQ_MUX0_FTM6_OR_CH0_CH7',
	'DMA_IP_REQ_MUX0_FTM7_OR_CH0_CH7', 'DMA_IP_REQ_MUX0←
	_ADC0', 'DMA_IP_REQ_MUX0_ADC1', 'DMA_IP_REQ_MUX0_LPI2\cdots C0 RX', 'DMA IP REQ MUX0 LPI2C0 TX', 'DMA IP REQ MUX0\cdots
	PDB0', 'DMA_IP_REQ_MUX0_LPI2C0_IX', 'DMA_IP_REQ_MUX0CMP0',
	'DMA_IP_REQ_MUX0_PORTA', 'DMA_IP_REQ_MUX0_PORTB',
	DMA_II_REQ_MOX0_FORTCI, 'DMA_II_REQ_MOX0_FORTDI, 'DMA_II_REQ_MUX0_PORTDI', 'DMA_II_REQ_MUX0_POR
	MA IP REQ MUX0 PORTE', 'DMA IP REQ MUX0 FLEXCANO', 'De-
	MA_IP_REQ_MUX0_FLEXCAN1', 'DMA_IP_REQ_MUX0_FLEXCAN2',
	'DMA_IP_REQ_MUX0_SAI0_RX', 'DMA_IP_REQ_MUX0_SAI0_TX',
	'DMA_IP_REQ_MUX0_LPTMR0', 'DMA_IP_REQ_MUX0_QUADSPI_
	RX', 'DMA_IP_REQ_MUX0_QUADSPI_TX', 'DMA_IP_REQ_MUX0_
	ALWAYS_ON0', 'DMA_IP_REQ_MUX0_ALWAYS_ON1']

${\bf 4.50}\quad {\bf Parameter~dmaGlobalRequest_enDmaRequest}$

Vendor specific: Enable the Dma Channel Hardware Request.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1

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Property	Value
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.51}\quad {\bf Container~dmaLogicChannelConfig_GlobalInterruptType}$

Vendor specific:

 ${\it TCD}$ Global Interrupt.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.52} \quad {\bf Parameter} \ {\bf dmaGlobalInterrupt_enDmaErrorInterrupt}$

Vendor specific: Enable the Dma Channel Error Interrupt.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE

Property	Value
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.53 Container dmaLogicChannelConfig_GlobalPriorityType

Vendor specific:

TCD Global Interrupt.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.54 Parameter dmaGlobalPriority_LevelPriority

Vendor specific: Set the Dma Channel Level Priority.

Note:

- If you want to change this value, you must Enable Global Config on "Logic Channel Configuration" tag.
- When have larger than one configured channel, the selected priority shall be from the pool of the configured channels, maintaining priority uniqueness. Ex: the user configures 3 channels: 0, 5, 15, by default the channel priority: 0-0, 5-5, 15-15. But the user wants to changes their channel priorities, the value only is selected one of 3 values (0, 5, 15) and they must be unique.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A

Property	Value
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_LEVEL_PRIO0
literals	['DMA_IP_LEVEL_PRIO0', 'DMA_IP_LEVEL_PRIO1', 'DMA_IP_LEV← EL_PRIO2', 'DMA_IP_LEVEL_PRIO3', 'DMA_IP_LEVEL_PRIO4', 'DM← A_IP_LEVEL_PRIO5', 'DMA_IP_LEVEL_PRIO6', 'DMA_IP_LEVEL_P← RIO7', 'DMA_IP_LEVEL_PRIO8', 'DMA_IP_LEVEL_PRIO9', 'DMA_IP← LEVEL_PRIO10', 'DMA_IP_LEVEL_PRIO11', 'DMA_IP_LEVEL_PRI← O12', 'DMA_IP_LEVEL_PRIO13', 'DMA_IP_LEVEL_PRIO14', 'DMA_I← P_LEVEL_PRIO15']

4.55 Parameter dmaGlobalPriority_enPreemption

Vendor specific: Enable the Dma Channel Preemption.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.56} \quad {\bf Parameter~dmaGlobalPriority_disPreempt}$

Vendor specific: Disable the Dma Channel Preempt.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.57 Container dmaLogicChannel_TransferConfigType

Vendor specific:

Logic Channel Transfer Configuration.

Included subcontainers:

- $\bullet \ \ dmaLogicChannelConfig_TransferControlType$
- $\bullet \ \, dmaLogicChannelConfig_TransferSourceType$
- $\bullet \ \ dmaLogicChannelConfig_TransferDestinationType$
- $\bullet \ \ dmaLogicChannelConfig_TransferMinorLoopType$
- $\bullet \ \, dmaLogicChannelConfig_TransferMajorLoopType$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.58}\quad {\bf Container~dmaLogicChannelConfig_TransferControlType}$

Vendor specific:

TCD Global Interrupt.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.59 \quad Parameter \ dmaLogicChannelConfig_enStart}$

Vendor specific: Enable the Dma Channel start service request (software request).

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.60 Parameter dmaLogicChannelConfig_enDmaMajorInterrupt

Vendor specific: Enable the Dma Channel major interrupt.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.61 Parameter dmaLogicChannelConfig_enDmaHalfMajorInterrupt

Vendor specific: Enable the Dma Channel half major interrupt.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.62 Parameter dmaLogicChannelConfig_disDmaAutoHwReq

Vendor specific: Disable the Dma Channel automatic request.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.63 \quad Parameter \ dmaLogic Channel Config_bandwidth Control}$

Vendor specific: Set the Dma Channel bandwidth control.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

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Property	Value
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_BWC_ENGINE_NO_STALL
literals	['DMA_IP_BWC_ENGINE_NO_STALL', 'DMA_IP_BWC_ENGINE_4C \Leftrightarrow YCLE_STALL', 'DMA_IP_BWC_ENGINE_8CYCLE_STALL']

${\bf 4.64} \quad {\bf Parameter~dmaLogicChannelConfig_ScatterGatherAddressType}$

Vendor specific: ScatterGather Address

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0U

${\bf 4.65 \quad Parameter} \\ {\bf dmaLogicChannelConfig_DestinationStoreAddressType}$

Vendor specific: Destination Store Address

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false

Property	Value
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0U

${\bf 4.66}\quad {\bf Container~dmaLogic Channel Config_Transfer Source Type}$

Vendor specific: Transfer Source

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.67} \quad {\bf Parameter~dmaLogicChannelConfig_SourceAddressType}$

Vendor specific: Source Address

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0

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${\bf 4.68 \quad Parameter \; dmaLogicChannelConfig_SourceSignedOffsetType}$

Vendor specific: Set the Dma Channel source signed offset value.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	32767
min	-32767

${\bf 4.69 \quad Parameter} \\ {\bf dmaLogicChannelConfig_SourceLastAddressAdjustmentType}$

Vendor specific: Set the Dma Channel source signed last address adjustment.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	2147483647
min	-2147483647

${\bf 4.70 \quad Parameter \; dmaTransferConfig_TransferSizeType}$

Vendor specific: Set the Dma Channel source transfer size.

Property	Value	
type	ECUC-ENUMERATION-PARAM-DEF	
origin	NXP	
symbolicNameValue	false	
lowerMultiplicity	1	
upperMultiplicity	1	
postBuildVariantMultiplicity	N/A	
multiplicityConfigClasses	N/A	
postBuildVariantValue	true	
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE	
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD	
defaultValue	DMA_IP_TRANSFER_SIZE_1_BYTE	
literals	['DMA_IP_TRANSFER_SIZE_1_BYTE', 'DMA_IP_TRANSFER_SIZE_←	
	$2_BYTE'$, 'DMA $_IP_TRANSFER_SIZE_4_BYTE'$, 'DMA $_IP_TRANSFE \leftarrow$	
	R_SIZE_16_BYTE', 'DMA_IP_TRANSFER_SIZE_32_BYTE']	

${\bf 4.71} \quad {\bf Parameter~dmaLogicChannelConfig_SourceModuloType}$

Vendor specific: Set the Dma Channel source modulo.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	31
min	0

4.72 Container dmaLogicChannelConfig_TransferDestinationType

Vendor specific: Transfer Destination

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.73 \quad Parameter \ dmaLogic Channel Config_Destination Address Type}$

Vendor specific: Destination Address

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0

${\bf 4.74 \quad Parameter} \\ {\bf dmaLogicChannelConfig_DestinationSignedOffsetType}$

Vendor specific: Set the Dma Channel destination signed offset value.

Property	Value
type	ECUC-INTEGER-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	32767
min	-32767

Vendor specific: Set the Dma Channel destination signed last address adjustment.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	2147483647
min	-2147483647

${\bf 4.76}\quad {\bf Parameter~dmaTransferConfig_TransferSizeType}$

Vendor specific: Set the Dma Channel destination transfer size.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

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Property	Value
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_TRANSFER_SIZE_1_BYTE
literals	

4.77 Parameter dmaLogicChannelConfig_DestinationModuloType

Vendor specific: Set the Dma Channel destination modulo.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	31
min	0

${\bf 4.78}\quad {\bf Container~dmaLogic Channel Config_Transfer Minor Loop Type}$

Vendor specific: Transfer Minor Loop

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.79}\quad {\bf Parameter~dmaLogicChannelConfig_enSourceOffset}$

Vendor specific: Enable the Dma Channel minor loop source offset.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.80 Parameter dmaLogicChannelConfig_enDestinationOffset

Vendor specific: Enable the Dma Channel minor loop destination offset.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

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${\bf 4.81 \quad Parameter \; dmaLogicChannelConfig_OffsetValueType}$

Vendor specific: Set the Dma Channel minor loop signed offset.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	1048575
min	-1048575

4.82 Parameter dmaLogicChannelConfig_enMinorLoopLinkCh

Vendor specific: Enable the Dma Channel minor loop logic channel linking.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.83 Parameter dmaLogicChannelConfig_MinorLoopSizeType

Vendor specific: Set the Dma Channel minor loop transfer size.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	1073741823
min	0

Vendor specific: Set the Dma Channel minor loop logic channel link.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	true
destination	/AUTOSAR/EcucDefs/Mcl/MclConfig/dmaLogicChannel_Type

${\bf 4.85}\quad {\bf Container~dmaLogic Channel Config_Transfer Major Loop Type}$

Vendor specific: Transfer Major Loop

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.86 Parameter dmaLogicChannelConfig_enMajorLoopLinkCh

Vendor specific: Enable the Dma Channel major loop logic channel linking.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

4.87 Parameter dmaLogicChannelConfig_MajorLoopCountType

Vendor specific: Sets the Dma Channel major loop count.

If minor loop channel linking is enabled, the major loop count limit is between 0 and 511.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE

Property	Value
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	32767
min	0

Vendor specific: Set the Dma Channel major loop logic channel link.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
${\it requires Symbolic Name Value}$	true
destination	/AUTOSAR/EcucDefs/Mcl/MclConfig/dmaLogicChannel_Type

4.89 Container dmaLogicChannel_ScatterGatherConfigType

Vendor specific:

Logic Channel ScatterGather Configuration.

Included subcontainers:

 $\bullet \ \, dmaLogicChannelConfig_ScatterGatherArrayType$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

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${\bf 4.90 \quad Container \ dmaLogic Channel Config_Scatter Gather Array Type}$

Vendor specific: Logic Channel ScatterGather Configuration.

Included subcontainers:

 $\bullet \ \, dmaLogicChannelConfig_ScatterGatherElementConfigType$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	256
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD

$\begin{array}{ccc} 4.91 & Container \\ & dmaLogicChannelConfig_ScatterGatherElementConfigType \end{array}$

Vendor specific: Element

Included subcontainers:

- dmaLogicChannelConfig_TransferControlType
- $\bullet \ \ dmaLogicChannelConfig_TransferSourceType$
- dmaLogicChannelConfig_TransferDestinationType
- $\bullet \ \ dmaLogicChannelConfig_TransferMinorLoopType$
- $\bullet \ \, dmaLogicChannelConfig_TransferMajorLoopType$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.92 \quad Parameter} \\ {\bf dmaLogicChannelConfig_ScatterGatherElementNameType}$

Vendor specific: Element Name

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0_SGA_ELEMENT_0

${\bf 4.93 \quad Parameter} \\ {\bf dmaLogicChannelConfig_LastElementLink_ScatterGatherType}$

Vendor specific: For non-circular lists, the last element shall have this checkbox set.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.94} \quad {\bf Parameter~dmaLogicChannelConfig_enScatterGatherConfig}$

Vendor specific: Enable Scatter/Gather Configuration

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

$\begin{array}{lll} 4.95 & Reference\ dynamic_dmaLogicChannelConfig_BasicElement_{\leftarrow} \\ & Link_ScatterGatherType \end{array}$

Vendor specific: Element Link. Elements shall be part of the same Logic Channel.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
multiplicity ComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
varueComigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
${\it requires Symbolic Name Value}$	true
destination	$/AUTOSAR/EcucDefs/Mcl/MclConfig/dmaLogicChannel_Type/dmaLogic \leftarrow$
	$Channel_ConfigType/dmaLogicChannel_ScatterGatherConfigType/dma {\leftarrow}$
	LogicChannelConfig_ScatterGatherArrayType

${\bf 4.96}\quad {\bf Container~dmaLogicChannelConfig_TransferControlType}$

Vendor specific:

TCD Global Interrupt.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.97 Parameter dmaLogicChannelConfig_enStart

Vendor specific: Enable the Dma Channel start service request (software request).

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.98}\quad {\bf Parameter~dmaLogicChannelConfig_enDmaMajorInterrupt}$

Vendor specific: Enable the Dma Channel major interrupt.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

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${\bf 4.99 \quad Parameter \ dmaLogic Channel Config_enDmaHalf Major Interrupt}$

Vendor specific: Enable the Dma Channel half major interrupt.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.100 \quad Parameter \; dmaLogic Channel Config_disDmaAutoHwReq}$

Vendor specific: Disable the Dma Channel automatic request.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.101 \quad Parameter \ dmaLogicChannelConfig_bandwidthControl}$

Vendor specific: Set the Dma Channel bandwidth control.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_BWC_ENGINE_NO_STALL
literals	['DMA_IP_BWC_ENGINE_NO_STALL', 'DMA_IP_BWC_ENGINE_4C↔ YCLE_STALL', 'DMA_IP_BWC_ENGINE_8CYCLE_STALL']

${\bf 4.102 \quad Parameter} \\ {\bf dmaLogicChannelConfig_ScatterGatherAddressType}$

Vendor specific: ScatterGather Address

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0U

$\begin{array}{ccc} 4.103 & Parameter \\ & dmaLogicChannelConfig_DestinationStoreAddressType \end{array}$

Vendor specific: Destination Store Address

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0U

4.104 Container dmaLogicChannelConfig_TransferSourceType

Vendor specific: Transfer Source

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.105} \quad {\bf Parameter~dmaLogicChannelConfig_SourceAddressType}$

Vendor specific: Source Address

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true

Property	Value
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0

${\bf 4.106 \quad Parameter \ dmaLogicChannelConfig_SourceSignedOffsetType}$

Vendor specific: Set the Dma Channel source signed offset value.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
${\it symbolic} Name Value$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	32767
min	-32767

${\bf 4.107 \quad Parameter} \\ {\bf dmaLogicChannelConfig_SourceLastAddressAdjustmentType}$

Vendor specific: Set the Dma Channel source signed last address adjustment.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD

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Property	Value
defaultValue	0
max	2147483647
min	-2147483647

${\bf 4.108} \quad {\bf Parameter~dmaTransferConfig_TransferSizeType}$

Vendor specific: Set the Dma Channel source transfer size.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigClasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_TRANSFER_SIZE_1_BYTE
literals	

${\bf 4.109}\quad {\bf Parameter~dmaLogicChannelConfig_SourceModuloType}$

Vendor specific: Set the Dma Channel source modulo.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0

Property	Value
max	31
min	0

$4.110 \quad Container \ dmaLogicChannelConfig_TransferDestinationType$

Vendor specific: Transfer Destination

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.111} \quad {\bf Parameter~dmaLogicChannelConfig_DestinationAddressType}$

Vendor specific: Destination Address

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0

${\bf 4.112 \quad Parameter} \\ {\bf dmaLogicChannelConfig_DestinationSignedOffsetType}$

Vendor specific: Set the Dma Channel destination signed offset value.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	32767
min	-32767

${\bf 4.113~ Parameter~dmaLogicChannelConfig_DestinationLastAddress} {\bf AdjustmentType}$

Vendor specific: Set the Dma Channel destination signed last address adjustment.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	2147483647
min	-2147483647

${\bf 4.114} \quad {\bf Parameter~dmaTransferConfig_TransferSizeType}$

Vendor specific: Set the Dma Channel destination transfer size.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varaecomigerasses	VARIANT-POST-BUILD: POST-BUILD
defaultValue	DMA_IP_TRANSFER_SIZE_1_BYTE
literals	['DMA_IP_TRANSFER_SIZE_1_BYTE', 'DMA_IP_TRANSFER_SIZE_←
	$2_BYTE'$, 'DMA $_IP_TRANSFER_SIZE_4_BYTE'$, 'DMA $_IP_TRANSFE$ \leftarrow
	R_SIZE_16_BYTE', 'DMA_IP_TRANSFER_SIZE_32_BYTE']

${\bf 4.115} \quad {\bf Parameter~dmaLogicChannelConfig_DestinationModuloType}$

Vendor specific: Set the Dma Channel destination modulo.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	31
min	0

4.116 Container dmaLogicChannelConfig_TransferMinorLoopType

Vendor specific: Transfer Minor Loop

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.117} \quad {\bf Parameter~dmaLogicChannelConfig_enSourceOffset}$

Vendor specific: Enable the Dma Channel minor loop source offset.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
${\it symbolicNameValue}$	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.118} \quad {\bf Parameter~dmaLogicChannelConfig_enDestinationOffset}$

Vendor specific: Enable the Dma Channel minor loop destination offset.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.119} \quad {\bf Parameter~dmaLogicChannelConfig_OffsetValueType}$

Vendor specific: Set the Dma Channel minor loop signed offset.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	1048575
min	-1048575

${\bf 4.120} \quad {\bf Parameter~dmaLogicChannelConfig_enMinorLoopLinkCh}$

Vendor specific: Enable the Dma Channel minor loop logic channel linking.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1

Property	Value
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.121} \quad {\bf Parameter~dmaLogicChannelConfig_MinorLoopSizeType}$

Vendor specific: Set the Dma Channel minor loop transfer size.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	0
max	1073741823
min	0

$\begin{array}{lll} \textbf{4.122} & \textbf{Reference dynamic_dmaLogicChannelConfig_MinorLoopLink} \\ & \textbf{ChValueType} \end{array}$

Vendor specific: Set the Dma Channel minor loop logic channel link.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE

Property	Value
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	true
destination	$/AUTOSAR/EcucDefs/Mcl/MclConfig/dmaLogicChannel_Type$

4.123 Container dmaLogicChannelConfig_TransferMajorLoopType

Vendor specific: Transfer Major Loop

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

${\bf 4.124} \quad {\bf Parameter~dmaLogicChannelConfig_enMajorLoopLinkCh}$

Vendor specific: Enable the Dma Channel major loop logic channel linking.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	false

${\bf 4.125 \quad Parameter \ dmaLogicChannelConfig_MajorLoopCountType}$

Vendor specific: Set the Dma Channel major loop count.

If minor loop channel linking is enabled, the major loop count limit is between 0 and 511.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: POST-BUILD
defaultValue	1
max	32767
min	0

$4.126 \quad Reference \ dynamic_dmaLogicChannelConfig_MajorLoopLink_{\leftarrow} \\ ChValueType$

Vendor specific: Set the Dma Channel major loop logic channel link.

Property	Value
type	ECUC-REFERENCE-DEF
origin	NXP
lowerMultiplicity	0
upperMultiplicity	1
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
postBuildVariantValue	false
valueConfigClasses	VARIANT-POST-BUILD: POST-BUILD
	VARIANT-PRE-COMPILE: PRE-COMPILE
requiresSymbolicNameValue	true
destination	/AUTOSAR/EcucDefs/Mcl/MclConfig/dmaLogicChannel_Type

4.127 Container trgmuxLogicGroup

List of Logic Trigger Groups.

Included subcontainers:

• trgmuxLogicTrigger

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	25
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

${\bf 4.128} \quad {\bf Parameter} \ {\bf trgmuxLogicGroup_Name}$

Logic Trigger Group.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueConnigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TRGMUX_IP_DMA
literals	

${\bf 4.129} \quad {\bf Parameter} \ {\bf trgmuxLogicGroup_Lock}$

Logic Trigger Lock.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	false

${\bf 4.130}\quad {\bf Container}\ {\bf trgmuxLogicTrigger}$

List of Logic Triggers.

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	58
postBuildVariantMultiplicity	true
multiplicityConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE

4.131 Parameter trgmuxLogicTrigger_Name

Logic Trigger Name.

Property	Value
type	ECUC-STRING-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TRGMUX_LOGIC_GROUP_0_TRIGGER↔
	_0

${\bf 4.132} \quad {\bf Parameter} \ {\bf trgmuxLogicTrigger_Output}$

Logic Trigger Output.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
varueComigCiasses	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TRGMUX_IP_OUTPUT_FLEXIO_TRG_TIM0

['TRGMUX_IP_OUTPUT_DMA_CH0', 'TRGMUX_IP_OUTPUT_DMA_CH1', 'TRGMUX_IP_OUTPUT_DMA_CH2', 'TRGMUX_IP_OUTPU_F T_DMA_CH3', 'TRGMUX_IP_OUTPUT_EXTOUT0_TRGMUX_OUT0 'TRGMUX_IP_OUTPUT_EXTOUT0_TRGMUX_OUT1', 'TRGMUX_IP_OUTPUT_EXTOUT0_TRGMUX_OUT2', 'TRGMUX_IP_OUTPUT_EXTOUT0_TRGMUX_IP_OUTPUT_EXTOUT1_TR_GMUX_OUT3', 'TRGMUX_IP_OUTPUT_EXTOUT1_TR_GMUX_OUT4', 'TRGMUX_IP_OUTPUT_EXTOUT1_TRGMUX_OUT5 'TRGMUX_IP_OUTPUT_EXTOUT1_TRGMUX_OUT5', 'TRGMUX_F	Property
IP_OUTPUT_EXTOUTI_TRGMUX_OUT7', 'TRGMUX_IP_OUTPUT_ADC0_ADHWT_TRIG_0', 'TRGMUX_IP_OUTPUT_ADC0_ADHWT_TRIG_1', 'TRGMUX_IP_OUTPUT_ADC0_ADHWT_TRIG_2' 'TRGMUX_IP_OUTPUT_ADC0_ADHWT_TRIG_3', 'TRGMUX_IP_OUTPUT_ADC1_ADHWT_TRIG_3', 'TRGMUX_IP_OUTPUT_ADC1_ADHWT_TRIG_3', 'TRGMUX_IP_OUTPUT_ADC1_ADHWT_TRIG_3', 'TRGMUX_IP_OUTPUT_ADC1_ADHWT_TRIG_3', 'TRGMUX_IP_OUTPUT_ADC1_ADHWT_TRIG_3', 'TRGMUX_IP_OUTPUT_ADC1_ADHWT_TRIG_3', 'TRGMUX_IP_OUTPUT_CMP0_SAMPLE_INPUT', 'TRGMUX_IP_OUTPUT_FTM0_FAULT0', 'TRGMUX_IP_OUTPUT_FTM0_FAULT1', 'TRGMUX_IP_OUTPUT_FTM0_FAULT1', 'TRGMUX_IP_OUTPUT_FTM0_FAULT1', 'TRGMUX_IP_OUTPUT_FTM1_FAULT1', 'TRGMUX_IP_OUTPUT_FTM1_FAULT1', 'TRGMUX_IP_OUTPUT_FTM1_FAULT1', 'TRGMUX_IP_OUTPUT_FTM2_FAULT1', 'TRGMUX_IP_OUTPUT_FTM2_FAULT1', 'TRGMUX_IP_OUTPUT_FTM3_FAULT1', 'TRGMUX_IP_OUTPUT_FTM3_FAULT1', 'TRGMUX_IP_OUTPUT_FTM3_FAULT1', 'TRGMUX_IP_OUTPUT_FTM3_FAULT1', 'TRGMUX_IP_OUTPUT_FTM3_FAULT1', 'TRGMUX_IP_OUTPUT_FTM3_FAULT1', 'TRGMUX_IP_OUTPUT_FTM3_FAULT2', 'TRGMUX_IP_OUTPUT_FTM3_FAULT2', 'TRGMUX_IP_OUTPUT_FTM3_FAULT2', 'TRGMUX_IP_OUTPUT_FTM3_FAULT3', 'TRGMUX_IP_OUTPUT_FTM4_FAUTA3_OUTPUT_FTM4_HWTRIG0', 'TRGMUX_IP_OUTPUT_FTM4_HWTRIG0', 'TRGMUX_IP_OUTPUT_FTM4_HWTRIG0', 'TRGMUX_IP_OUTPUT_FTM4_HWTRIG0', 'TRGMUX_IP_OUTPUT_FTM4_HWTRIG0', 'TRGM	2 0

${\bf 4.133 \quad Parameter \ trgmuxLogicTrigger_Input}$

Logic Trigger Input.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP

Property	Value
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-POST-BUILD: PRE-COMPILE
	VARIANT-PRE-COMPILE: PRE-COMPILE
defaultValue	TRGMUX_IP_INPUT_LOGIC0_VSS
literals	TRGMUX_IP_INPUT_LOGICO_VSS', 'TRGMUX_IP_INPUT_LOGICO_VDD', 'TRGMUX_IP_INPUT_TRGMUX_INO', 'TRGMUX_IP_INPUT_TRGMUX_IP_INPUT_TRGMUX_IP', 'TRGMUX_X IP_INPUT_TRGMUX_INO', 'TRGMUX_IP_INPUT_TRGMUX_INO', 'TRGMUX_INO', 'TRGMUX_INO', 'TRGMUX_INO', 'TRGMUX_INO', 'TRGMUX_INO', 'TRGMUX_INO', 'TRGMUX_INO', 'TRGMUX_INO', 'TRGMUX_INO', 'TRGMUX_IP_INPUT_TRGMUX_INO', 'TRGMUX_IP_INPUT_TRGMUX_INO', 'TRGMUX_IP_INPUT_TRGMUX_INO', 'TRGMUX_IP_INPUT_TRGMUX_INO', 'TRGMUX_IP_INPUT_TRGMUX_INO', 'TRGMUX_IP_INPUT_LPIT_CHO', 'TRGMUX_IP_INPUT_LPIT_CHO', 'TRGMUX_IP_INPUT_LPIT_CHO', 'TRGMUX_IP_INPUT_LPIT_CHO', 'TRGMUX_IP_INPUT_LPIT_CHO', 'TRGMUX_IP_INPUT_LPIT_CHO', 'TRGMUX_IP_INPUT_LPIT_CHO', 'TRGMUX_IP_INPUT_TRGMUX_IP_INPUT_TRGMO', 'TRGMUX_IP_INPUT_TAGMU, 'TRGMUX_IP_INPUT_TAGMO', 'TRGMUX_IP_INPUT_ADCO', 'T

4.134 Container FlexioCommon

List of Flexio instances available on the platform.

Included subcontainers:

$\bullet \quad FlexioMclLogicChannels \\$

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	0
upperMultiplicity	8
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
muniphency Connig Classes	VARIANT-POST-BUILD: POST-BUILD

4.135 Parameter FlexioMclInstances

Select one of the Flexio instance available on the platform.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	FLEXIO_0
literals	['FLEXIO_0']

${\bf 4.136}\quad {\bf Parameter\ FlexioDebugEnable}$

Enable Debug Mode

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

${\bf 4.137}\quad {\bf Container\ FlexioMclLogicChannels}$

Flexio Logic Channel Configuration

Included subcontainers:

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	4
postBuildVariantMultiplicity	false
multiplicityConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
martipherty ComigCiasses	VARIANT-POST-BUILD: PRE-COMPILE

4.138 Parameter FlexioMclChannelId

Select one of the Flexio channels available on the platform for selected instance.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

Property	Value
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	CHANNEL_0
literals	['CHANNEL_0', 'CHANNEL_1', 'CHANNEL_2', 'CHANNEL_3']

4.139 Parameter FlexioMclPinId

Select one of the Flexio pins available on the platform for selected instance.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueConnigClasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	PIN_0
literals	['PIN_0', 'PIN_1', 'PIN_2', 'PIN_3', 'PIN_4', 'PIN_5', 'PIN_6', 'PIN_7']

4.140 Parameter FlexioMclAddPinEnable

Enable feature to select one more Flexio pin.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComingClasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

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4.141 Parameter FlexioMclAddPinId

Select one of the Flexio pins available on the platform for selected instance.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	PIN_1
literals	['PIN_0', 'PIN_1', 'PIN_2', 'PIN_3', 'PIN_4', 'PIN_5', 'PIN_6', 'PIN_7']

4.142 Parameter FlexioMclAddChannelEnable

Enable feature to select one more Flexio channel.

Property	Value
type	ECUC-BOOLEAN-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
varueComigCiasses	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	false

4.143 Parameter FlexioMclAddChannelId

Select one of the Flexio channels available on the platform for selected instance.

Property	Value
type	ECUC-ENUMERATION-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	true
valueConfigClasses	VARIANT-PRE-COMPILE: PRE-COMPILE
	VARIANT-POST-BUILD: PRE-COMPILE
defaultValue	CHANNEL_0
literals	['CHANNEL_0', 'CHANNEL_1', 'CHANNEL_2', 'CHANNEL_3']

4.144 Container CommonPublishedInformation

Vendor specific:

Common container, aggregated by all modules. It contains published information about

Included subcontainers:

vendor and versions.

• None

Property	Value
type	ECUC-PARAM-CONF-CONTAINER-DEF
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A

4.145 Parameter ArReleaseMajorVersion

Vendor specific:

Major version number of AUTOSAR specification on which the appropriate implementation

is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF

Property	Value
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

4.146 Parameter ArReleaseMinorVersion

Vendor specific:

 $\label{eq:minor} \mbox{Minor version number of AUTOSAR specification on which the appropriate implementation}$

is based on.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	4
max	4
min	4

4.147 Parameter ArReleaseRevisionVersion

Vendor specific:

Revision version number of AUTOSAR specification on which the appropriate implementation

is based on.

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Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

4.148 Parameter ModuleId

Vendor specific:

Module ID of this module from Module List.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	255
max	255
min	255

4.149 Parameter SwMajorVersion

Vendor specific:

 $\label{eq:major version number of the vendor specific implementation of the module. The numbering is vendor specific.$

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	1
max	1
min	1

4.150 Parameter SwMinorVersion

Vendor specific:

Minor version number of the vendor specific implementation of the module. The numbering is vendor specific.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	0
max	0
min	0

4.151 Parameter SwPatchVersion

Vendor specific:

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Patch level version number of the vendor specific implementation of the module. The numbering is vendor specific.

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	1
max	1
min	1

4.152 Parameter VendorId

Vendor specific:

vendor list.

Vendor ID of the dedicated implementation of this module according to the AUTOSAR

Property	Value
type	ECUC-INTEGER-PARAM-DEF
origin	NXP
symbolicNameValue	false
lowerMultiplicity	1
upperMultiplicity	1
postBuildVariantMultiplicity	N/A
multiplicityConfigClasses	N/A
postBuildVariantValue	false
valueConfigClasses	VARIANT-PRE-COMPILE: PUBLISHED-INFORMATION
	VARIANT-POST-BUILD: PUBLISHED-INFORMATION
defaultValue	43
max	43
min	43

This chapter describes the Tresos configuration plug-in for the driver Driver. The most of the parameters are described below.

Chapter 5

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5.1 Software Specification

Here is a list of all modules:

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6.2 MCL Driver

6.2.1 Detailed Description

Data Structures

• struct Mcl_ConfigType

This type contains the Mcl Configuration. More...

Macros

• #define MCL_DET_INIT

API service ID for Mcl_Init function.

• #define MCL DET DEINIT

API service ID for Mcl_DeInit function.

• #define MCL_E_UNINIT

All API's having pointers as parameters shall return this error if called with with a NULL value.

• #define MCL_E_PARAM_POINTER

All API's having pointers as parameters shall return this error if called with with a NULL value.

• #define MCL_E_INVALID_INSTANCE

All API's called with wrong instance shall return this error.

• #define MCL E INVALID CHANNEL

All API's called with wrong channel shall return this error.

• #define MCL E INVALID COMMAND

All API's called with wrong instance shall return this error.

All API's called with wrong read parameter shall return this error.

• #define MCL E INVALID STATE

All API's called in wrong sequence shall return this error.

• #define MCL E INCONSISTENCY

All API's called while hardware has error status shall return this error.

• #define MCL E TIMEOUT

All API's called with a timeout value shall return this error if execution is not finished in the allocated timeframe.

• #define MCL E PROTECTED

If DET error reporting is enabled, the MCL will check if registers are protected.

• #define MCL E INIT FAILED

If VariantPreCompile is used, the configuration pointer shall have a $NULL_PTR$ value. If VariantPostBuild is used, the configuration pointer shall be different from $NULL_PTR$. And in case of violate will return $MCL_E_INIT_ \leftarrow FAILED$.

Enum Reference

• enum Mcl ReturnType

This type contains the Mcl Return Type.

Function Reference

- void Mcl_Init (const Mcl_ConfigType *const ConfigPtr)

 This function initializes the Mcl Driver.
- void Mcl_DeInit (void)

This function deinitializes the Mcl Driver.

6.2.1.1 MISRA-C:2012 violations

6.2.2 Data Structure Documentation

6.2.2.1 struct Mcl_ConfigType

This type contains the Mcl Configuration.

The Mcl Configuration structure contains pointers to the Ip's configuration structure. Based on the available support, specific configurations shall be stored.

Definition at line 289 of file Mcl_Types.h.

6.2.3 Macro Definition Documentation

6.2.3.1 MCL_DET_INIT

#define MCL_DET_INIT

API service ID for Mcl Init function.

Parameters used when raising an error/exception

Definition at line 155 of file CDD_Mcl.h.

6.2.3.2 MCL_DET_DEINIT

#define MCL_DET_DEINIT

API service ID for Mcl_DeInit function.

Parameters used when raising an error/exception

Definition at line 221 of file CDD_Mcl.h.

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6.2.3.3 MCL_E_UNINIT

#define MCL_E_UNINIT

All API's having pointers as parameters shall return this error if called with with a NULL value.

Definition at line 303 of file CDD_Mcl.h.

6.2.3.4 MCL_E_PARAM_POINTER

#define MCL_E_PARAM_POINTER

All API's having pointers as parameters shall return this error if called with with a NULL value.

Definition at line 310 of file CDD_Mcl.h.

6.2.3.5 MCL_E_INVALID_INSTANCE

#define MCL_E_INVALID_INSTANCE

All API's called with wrong instance shall return this error.

Definition at line 316 of file CDD_Mcl.h.

6.2.3.6 MCL_E_INVALID_CHANNEL

#define MCL_E_INVALID_CHANNEL

All API's called with wrong channel shall return this error.

Definition at line 322 of file CDD_Mcl.h.

6.2.3.7 MCL_E_INVALID_COMMAND

#define MCL_E_INVALID_COMMAND

All API's called with wrong instance shall return this error.

Definition at line 328 of file CDD_Mcl.h.

6.2.3.8 MCL_E_INVALID_PARAMETER

#define MCL_E_INVALID_PARAMETER

All API's called with wrong read parameter shall return this error.

Definition at line 334 of file CDD_Mcl.h.

6.2.3.9 MCL_E_INVALID_STATE

#define MCL_E_INVALID_STATE

All API's called in wrong sequence shall return this error.

Definition at line 340 of file CDD_Mcl.h.

6.2.3.10 MCL_E_INCONSISTENCY

#define MCL_E_INCONSISTENCY

All API's called while hardware has error status shall return this error.

Definition at line 346 of file CDD_Mcl.h.

6.2.3.11 MCL_E_TIMEOUT

#define MCL_E_TIMEOUT

All API's called with a timeout value shall return this error if execution is not finished in the allocated timeframe.

Definition at line 353 of file CDD_Mcl.h.

6.2.3.12 MCL_E_PROTECTED

#define MCL_E_PROTECTED

If DET error reporting is enabled, the MCL will check if registers are protected.

Definition at line 359 of file CDD_Mcl.h.

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6.2.3.13 MCL_E_INIT_FAILED

```
#define MCL_E_INIT_FAILED
```

If VariantPreCompile is used, the configuration pointer shall have a NULL_PTR value. If VariantPostBuild is used, the configuration pointer shall be different from NULL_PTR. And in case of violate will return MCL_E_INIT_ \leftarrow FAILED.

Definition at line 366 of file CDD Mcl.h.

6.2.4 Enum Reference

6.2.4.1 Mcl_ReturnType

```
enum Mcl_ReturnType
```

This type contains the Mcl Return Type.

The Return Type give information for the execution of interfaces.

Definition at line 259 of file Mcl_Types.h.

6.2.5 Function Reference

6.2.5.1 Mcl_Init()

This function initializes the Mcl Driver.

This service is a non reentrant function that shall initialize the Mcl driver. The initialization is applied for the enabled IPs, configured statically.

Parameters

in	ConfigPtr	Pointer to the configuration structure.
----	-----------	-----------------------------------------

Returns

void

6.2.5.2 Mcl_DeInit()

```
void Mcl_DeInit (
     void )
```

This function deinitializes the Mcl Driver.

This service is a non reentrant function that shall deinitialize the Mcl driver. The deinitialization is applied for the enabled IPs, configured statically.

Returns

void

6.3 DMA IP Driver

6.3.1 Detailed Description

6.4 FLEXIO IP Driver

6.4.1 Detailed Description

Enum Reference

- enum Flexio_Mcl_Ip_TimerPolarityType
- enum Flexio_Mcl_Ip_PinPolarityType
- $\bullet \ \ enum \ Flexio_Mcl_Ip_PinConfigType$
- enum Flexio_Mcl_Ip_TriggerPolarityType
- enum Flexio_Mcl_Ip_TriggerSourceType
- enum Flexio Mcl Ip TimerModeType
- enum Flexio_Mcl_Ip_TimerOutputType
- $\bullet \ \ enum \ Flexio_Mcl_Ip_TimerDecrementType$
- enum Flexio_Mcl_Ip_TimerResetType
- enum Flexio_Mcl_Ip_TimerDisableType
- enum Flexio_Mcl_Ip_TimerEnableType
- \bullet enum Flexio_Mcl_Ip_TimerStopType
- enum Flexio_Mcl_Ip_TimerStartType

6.4.2 Enum Reference

${\bf 6.4.2.1 \quad Flexio_Mcl_Ip_TimerPolarityType}$

enum Flexio_Mcl_Ip_TimerPolarityType

Enumerator

FLEXIO_TIMER_POLARITY_POSEDGE	Shift on positive edge of Shift clock
FLEXIO_TIMER_POLARITY_NEGEDGE	Shift on negative edge of Shift clock

Definition at line 123 of file Flexio_Mcl_Ip_HwAccess.h.

6.4.2.2 Flexio_Mcl_Ip_PinPolarityType

enum Flexio_Mcl_Ip_PinPolarityType

Enumerator

FLEXIO_PIN_POLARITY_HIGH	Pin is active high
FLEXIO_PIN_POLARITY_LOW	Pin is active low

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Definition at line 131 of file Flexio_Mcl_Ip_HwAccess.h.

$6.4.2.3 \quad Flexio_Mcl_Ip_PinConfigType$

enum Flexio_Mcl_Ip_PinConfigType

Enumerator

FLEXIO_PIN_CONFIG_DISABLED	Shifter pin output disabled
FLEXIO_PIN_CONFIG_OPEN_DRAIN	Shifter pin open drain or bidirectional output enable
FLEXIO_PIN_CONFIG_BIDIR_OUTPUT	Shifter pin bidirectional output data
FLEXIO_PIN_CONFIG_OUTPUT	Shifter pin output

Definition at line 138 of file Flexio_Mcl_Ip_HwAccess.h.

${\bf 6.4.2.4 \quad Flexio_Mcl_Ip_TriggerPolarityType}$

enum Flexio_Mcl_Ip_TriggerPolarityType

Enumerator

FLEXIO_TRIGGER_POLARITY_HIGH	Trigger is active high
FLEXIO_TRIGGER_POLARITY_LOW	Trigger is active low

Definition at line 171 of file Flexio_Mcl_Ip_HwAccess.h.

${\bf 6.4.2.5}\quad {\bf Flexio_Mcl_Ip_TriggerSourceType}$

enum Flexio_Mcl_Ip_TriggerSourceType

Enumerator

FLEXIO_TRIGGER_SOURCE_EXTERNAL	External trigger selected
FLEXIO_TRIGGER_SOURCE_INTERNAL	Internal trigger selected

Definition at line 178 of file Flexio_Mcl_Ip_HwAccess.h.

${\bf 6.4.2.6}\quad {\bf Flexio_Mcl_Ip_TimerModeType}$

enum Flexio_Mcl_Ip_TimerModeType

Enumerator

FLEXIO_TIMER_MODE_DISABLED	Timer Disabled.
FLEXIO_TIMER_MODE_8BIT_BAUD	Dual 8-bit counters baud/bit mode.
FLEXIO_TIMER_MODE_8BIT_PWM	Dual 8-bit counters PWM mode.
FLEXIO_TIMER_MODE_16BIT	Single 16-bit counter mode.
FLEXIO_TIMER_MODE_16BIT_DIS	Single 16-bit counter disable mode.
FLEXIO_TIMER_MODE_8BIT_DUAL	Dual 8-bit counters word mode.
FLEXIO_TIMER_MODE_8BIT_DUAL_PWM	Dual 8-bit counters PWM low mode.
FLEXIO_TIMER_16BIT_INPUT_CAPTURE_MODE	Single 16-bit input capture mode.

Definition at line 185 of file Flexio_Mcl_Ip_HwAccess.h.

${\bf 6.4.2.7} \quad {\bf Flexio_Mcl_Ip_TimerOutputType}$

enum Flexio_Mcl_Ip_TimerOutputType

Enumerator

FLEXIO_TIMER_INITOUT_ONE	Timer output is logic one when enabled, unaffected by timer
	reset.
FLEXIO_TIMER_INITOUT_ZERO	Timer output is logic zero when enabled, unaffected by timer
	reset.
FLEXIO_TIMER_INITOUT_ONE_RESET	Timer output is logic one when enabled and on timer reset.
FLEXIO_TIMER_INITOUT_ZERO_RESET	Timer output is logic zero when enabled and on timer reset.

Definition at line 198 of file Flexio_Mcl_Ip_HwAccess.h.

${\bf 6.4.2.8}\quad {\bf Flexio_Mcl_Ip_TimerDecrementType}$

 $\verb"enum Flexio_Mcl_Ip_TimerDecrementType"$

Enumerator

$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	Decrement counter on FlexIO clock, Shift clock equals Timer output.
	Decrement counter on Trigger input (both edges), Shift clock equals Timer output.
FLEXIO_TIMER_DECREMENT_PIN_SHIFT_ PIN	Decrement counter on Pin input (both edges), Shift clock equals Pin input.
	Decrement counter on Trigger input (both edges), Shift clock equals Trigger input.

Definition at line 207 of file Flexio_Mcl_Ip_HwAccess.h.

${\bf 6.4.2.9 \quad Flexio_Mcl_Ip_TimerResetType}$

enum Flexio_Mcl_Ip_TimerResetType

Enumerator

FLEXIO_TIMER_RESET_NEVER	Timer never reset.
FLEXIO_TIMER_RESET_PIN_OUT	Timer reset on Timer Pin equal to Timer Output.
FLEXIO_TIMER_RESET_TRG_OUT	Timer reset on Timer Trigger equal to Timer Output.
FLEXIO_TIMER_RESET_PIN_RISING	Timer reset on Timer Pin rising edge.
FLEXIO_TIMER_RESET_TRG_RISING	Timer reset on Trigger rising edge.
FLEXIO_TIMER_RESET_TRG_BOTH	Timer reset on Trigger rising or falling edge.

Definition at line 216 of file Flexio_Mcl_Ip_HwAccess.h.

${\bf 6.4.2.10 \quad Flexio_Mcl_Ip_TimerDisableType}$

 $\verb"enum Flexio_Mcl_Ip_TimerDisableType"$

Enumerator

FLEXIO_TIMER_DISABLE_NEVER	Timer never disabled.	
FLEXIO_TIMER_DISABLE_TIM_DISABLE	Timer disabled on Timer N-1 disable.	
FLEXIO_TIMER_DISABLE_TIM_CMP	Timer disabled on Timer compare.	
FLEXIO_TIMER_DISABLE_TIM_CMP_TRG_	Timer disabled on Timer compare and Trigger Low.	
LOW		
FLEXIO_TIMER_DISABLE_PIN	Timer disabled on Pin rising or falling edge.	
FLEXIO_TIMER_DISABLE_PIN_TRG_HIGH	Timer disabled on Pin rising or falling edge provided	
	Trigger is high.	
FLEXIO_TIMER_DISABLE_TRG_Timer disabled on Trigger falling edge.		

Definition at line 227 of file Flexio_Mcl_Ip_HwAccess.h.

${\bf 6.4.2.11}\quad {\bf Flexio_Mcl_Ip_TimerEnableType}$

enum Flexio_Mcl_Ip_TimerEnableType

Enumerator

FLEXIO_TIMER_ENABLE_ALWAYS	Timer always enabled.
FLEXIO_TIMER_ENABLE_TIM_ENABLE	Timer enabled on Timer N-1 enable.
FLEXIO_TIMER_ENABLE_TRG_HIGH	Timer enabled on Trigger high.
FLEXIO_TIMER_ENABLE_TRG_PIN_HIGH	Timer enabled on Trigger high and Pin high.
FLEXIO_TIMER_ENABLE_PIN_POSEDGE	Timer enabled on Pin rising edge.
FLEXIO_TIMER_ENABLE_PIN_POSEDGE_TRG↔	Timer enabled on Pin rising edge and Trigger high.
_HIGH	
FLEXIO_TIMER_ENABLE_TRG_POSEDGE	Timer enabled on Trigger rising edge.
FLEXIO_TIMER_ENABLE_TRG_EDGE	Timer enabled on Trigger rising or falling edge.

Definition at line 239 of file Flexio_Mcl_Ip_HwAccess.h.

$6.4.2.12 \quad {\bf Flexio_Mcl_Ip_TimerStopType}$

enum Flexio_Mcl_Ip_TimerStopType

Enumerator

FLEXIO_TIMER_STOP_BIT_DISABLED	Stop bit disabled.
FLEXIO_TIMER_STOP_BIT_TIM_CMP	Stop bit is enabled on timer compare.
FLEXIO_TIMER_STOP_BIT_TIM_DIS	Stop bit is enabled on timer disable.
FLEXIO_TIMER_STOP_BIT_TIM_CMP_DIS	Stop bit is enabled on timer compare and disable.

Definition at line 252 of file Flexio_Mcl_Ip_HwAccess.h.

${\bf 6.4.2.13 \quad Flexio_Mcl_Ip_TimerStartType}$

enum Flexio_Mcl_Ip_TimerStartType

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Enumerator

FLEXIO_TIMER_START_BIT_DISABLED	Start bit disabled.
FLEXIO_TIMER_START_BIT_ENABLED	Start bit enabled.

Definition at line 278 of file Flexio_Mcl_Ip_HwAccess.h.

6.5 FTM IP Driver

6.5.1 Detailed Description

6.6 TRGMUX IP Driver

6.6.1 Detailed Description

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