**FAST UNIVERSITY**
**CS DEPARTMENT**

# DLD-LAB FINAL PROJECT (BSCS)

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# Report:

## Introduction & Objectives:

Our project is on **6-Bit Random Number Generator**. We are required to make a circuit which can generate a 6-Bit Binary Number. And we must show the output both in binary and decimal representation.

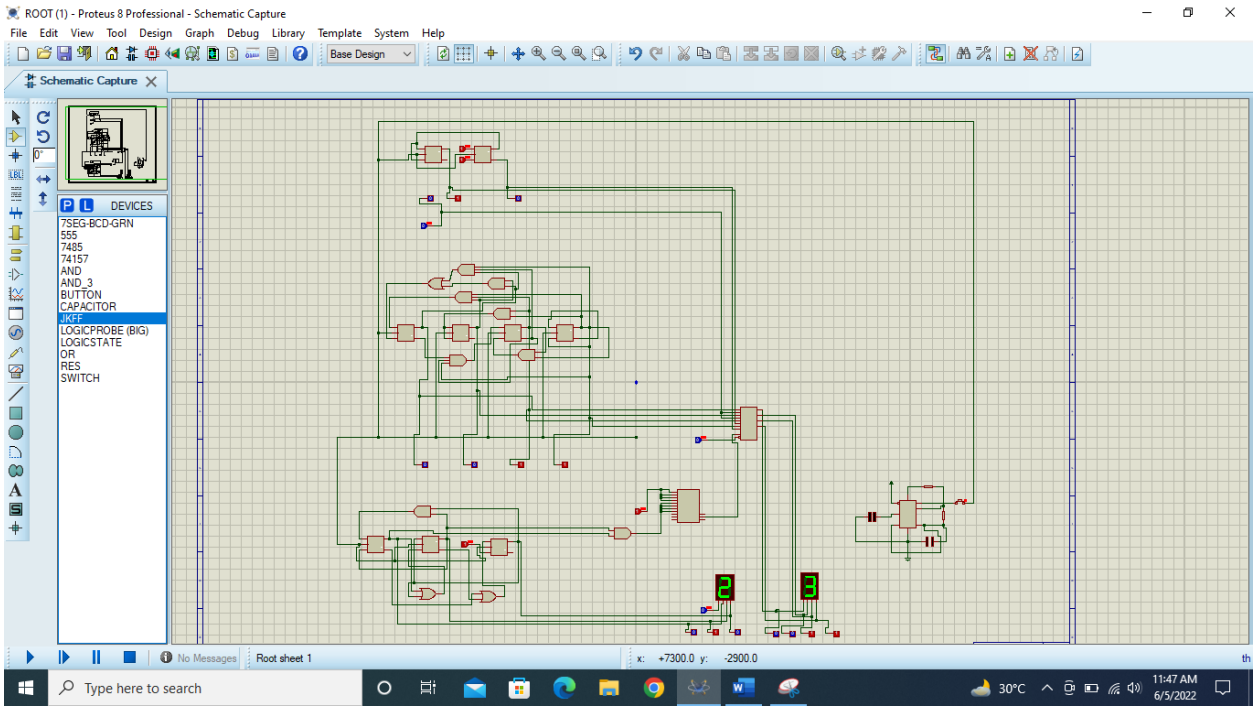
$2^6 = 64$. So, the number must be in the range from 0-63 and the decimal value can't exceed 63.

## Components:

We used the following components for our required circuit:

- **555 timer I.C**
- **Resistors.**
- **Capacitors.**
- **Push button.**
- **Quadruple 2 to 1 line MUX. (74157)**
- **4-bit magnitude comparator (7485)**
- **7-Seg-BCD common Cathode.**

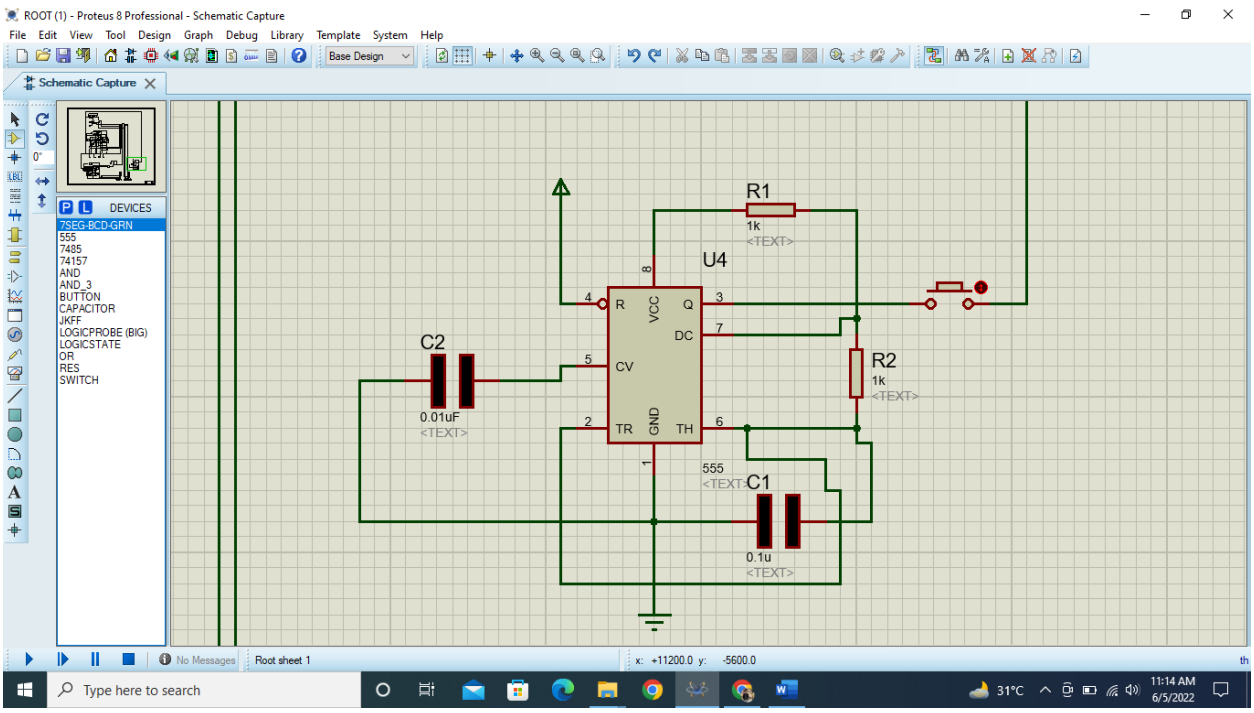
- Decoder (7448).
- JK FF (7473)
- Led's.
- And Gate I.C (7408).
- Or Gate I.C (7432).
- Battery 9V.
- Regulator.




# Explanation:

## 1- Usage of 555 timer I.C:

We used a 555 timer I.C to generate the clock pulse. A push button is attached to the 555 timer I.C. So, that whenever the push button is pressed, a random is generated and displayed on the Led's in binary and on 7-Segmented led displays.

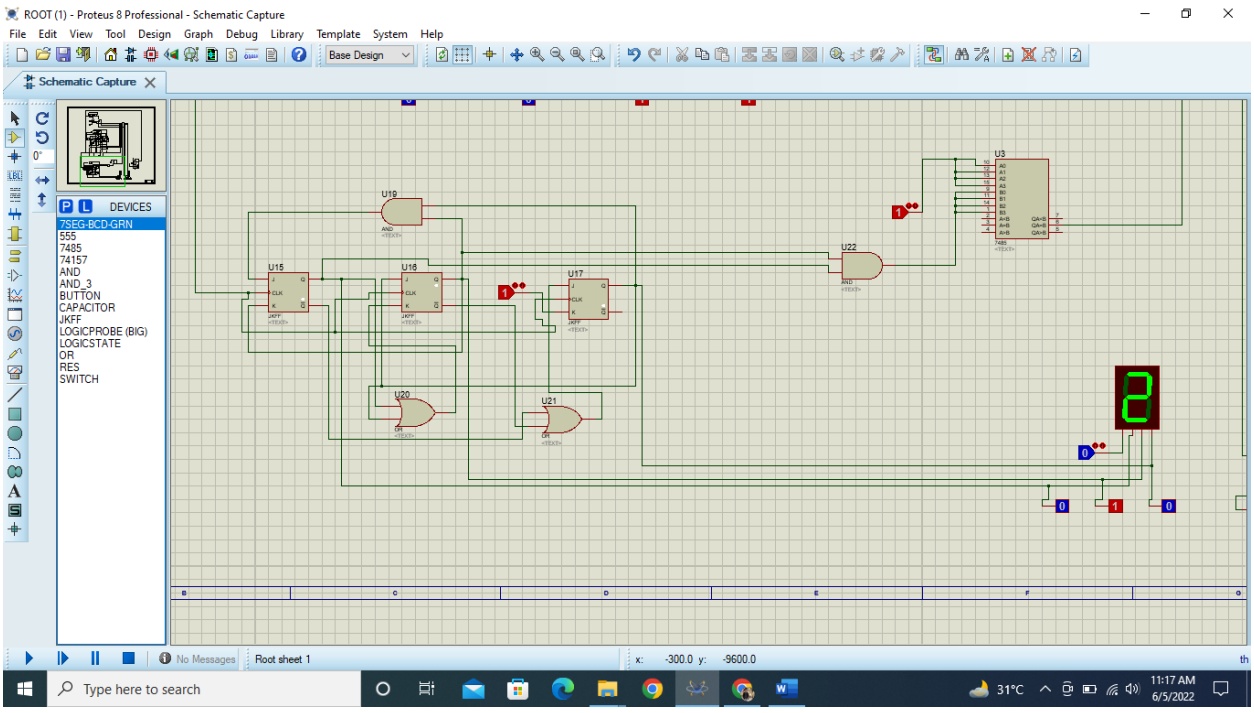



## 2-Making of Counters:

We need to make a counter that generate numbers between a desired range. So, for that purpose we used jkff's. We made the state table, wrote the present states and next states. And then found the values of j and k for the flipflops using characteristics. Then finally we used K-map and found the simplified expression for each input of flipflop.

For making a counter between **0-6**, the simplified expressions we found are:

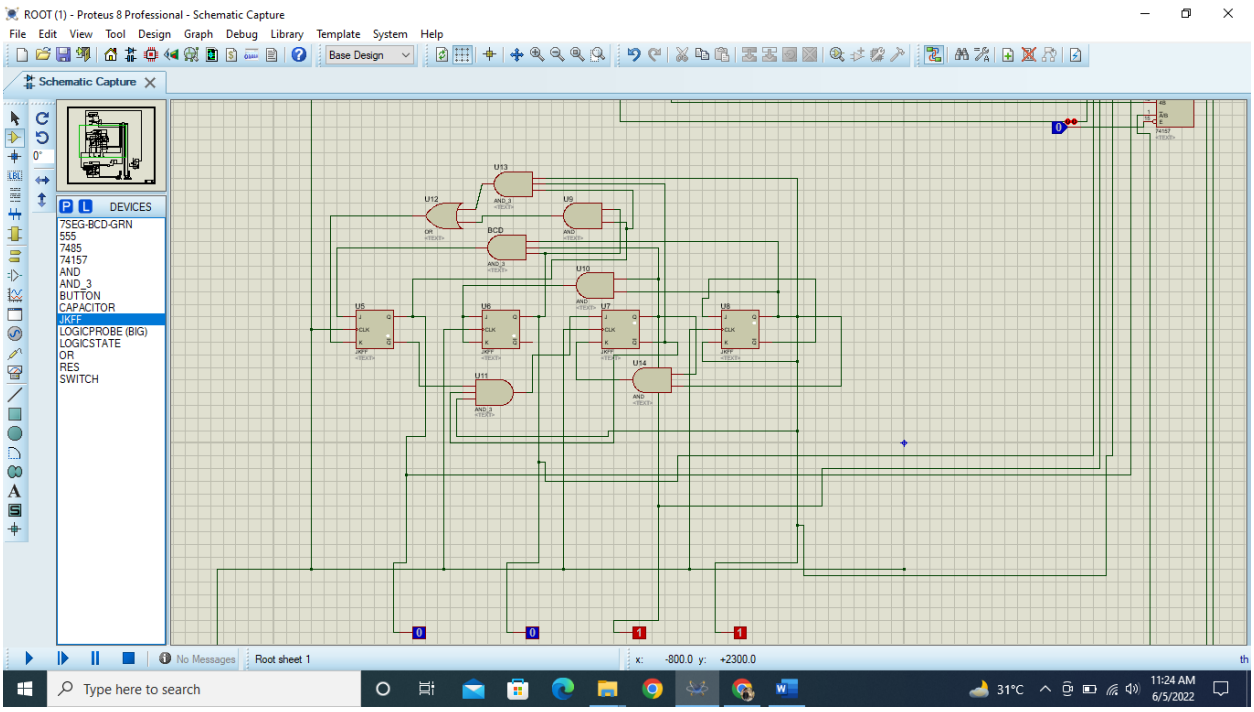
$J_A = Q_B.Q_C$ $K_A = Q_B$ $J_B = Q_C$ $K_B = Q_A + Q_C$ $J_C = Q'_A + Q'_B$ $K_C = 1$




Now the next thing is to make the counter for **0-9**, for that the expressions we found out are:

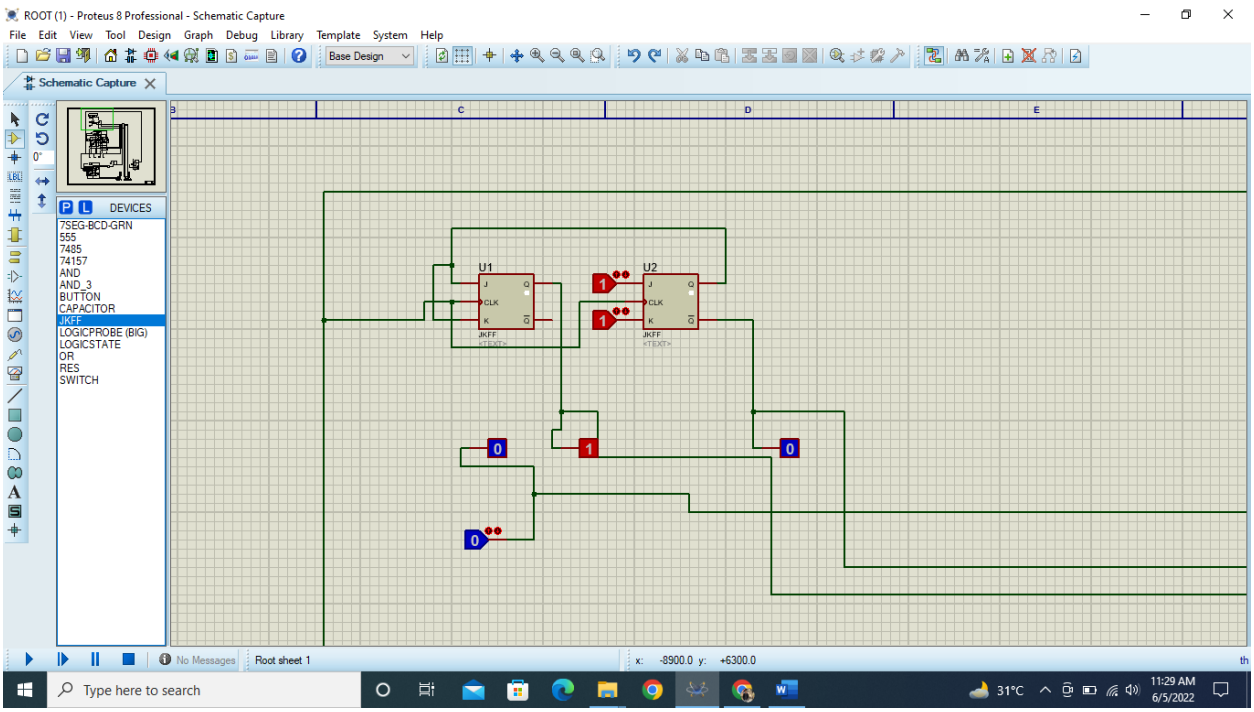
$J_A = Q_B . Q_C . Q_D$ $K_A = Q_A.Q_B + Q_A.Q'_C . Q_D$ $J_B = Q_C.Q_D$ $K_B = Q_C.Q_D$

$J_C = Q'_A.Q'C.Q_D$ $K_C = Q_C.Q_D$ $J_D = Q'_D$ $K_D = Q_D$



Our final problem is that when 6 gets generated on the tenth place then we must limit the unit place to 0-3. So, for that we made another counter of 0-3. For which the simplified expressions are:

$J_A = K_A = Q_B$ $J_B = K_B = 1$




## 3-Comparator and Multiplexer:

We used a 4-bit comparator to check whether the output generated at tenth place is between 0-5 or only 6, by giving it a pre-defined input. If the number is generated between 0-5 then the unit place must be between 0-9. So, the condition A=B is not satisfied and input at the multiplexer is 0. So, it selects all the A lines which is 0-9 and pass it to the decoders to display it in the 7-segmented displays.

If the number at the tenth place generated is 6. Then the A=B output line of comparator is 1. And the lines selected at the multiplexer is of the circuit (0-3) ones.

Based on the output of A=B line of comparator the unit place is selected.