

# HY330 – VLSI Digital systems

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## Exercise set 1

The purpose of this set of exercises is to design a CMOS inverter in MAGIC program and then the same model that was designed, to be simulated in NGSPICE to extract real delay values such as inertia delay and rise-fall time.

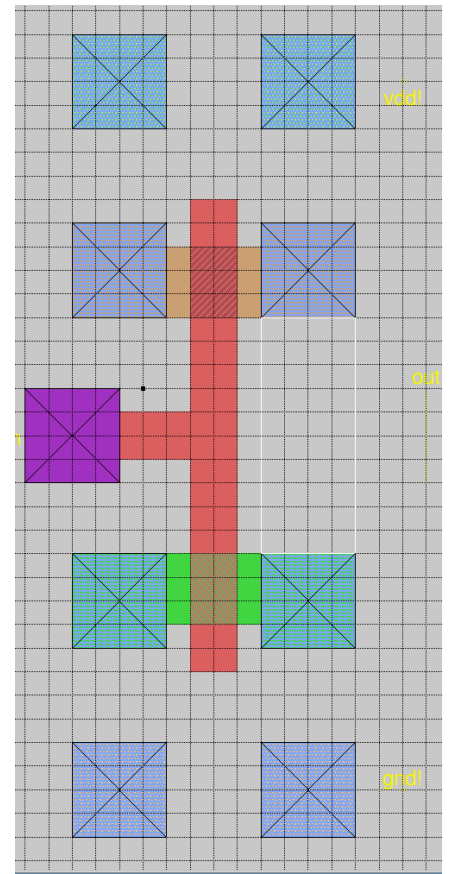
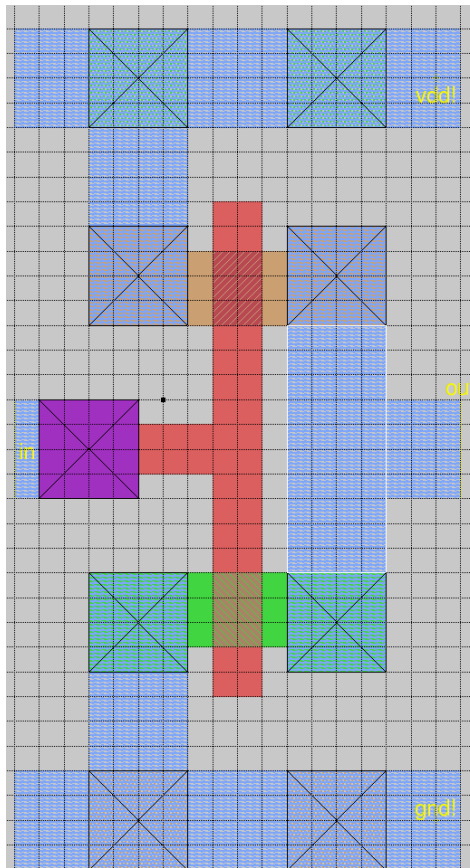
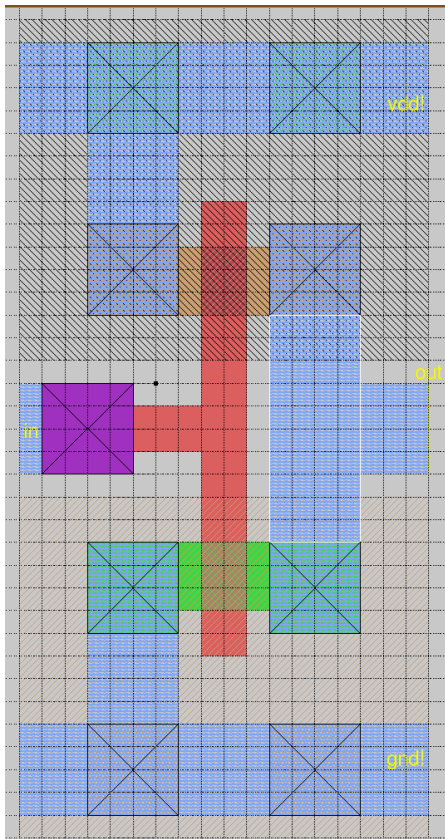
### Exercise 1

In Exercise 1, the goal is to design the CMOS inverter in MAGIC with the following limitations / specifications:

- Power lines 4 $\mu\text{m}$  wide ,with labels *vdd* ,*gnd*
- P and N type wells for the transistors
- Substrate contacts of the 2 transistors
- Labels in the inputs and outputs, labeled *in* and *out* respectively

In addition, the inverter implementation technology is MOSIS SCMOS 0.25 $\mu\text{m}$ .

Down below images of the design:



The photos also show the inverter with some levels removed each time as we go to the right (With greater clarity and more detail can be seen the drawing in the image and the mag file that will be included in the deliverable file).

From the pictures it is easy to see:

- Contacts have been selected to connect substrates (psubstratepcontact, nsubstratencontact) 4x4, the minimum dimension allowed.
- The same happened with the pdcontact and ndcontact contacts that we connect to the source and drain of the transistor pmos and nmos respectively.
- A polysilicon and metal 1 contact is used because we must have an input or an output of the circuit only of metal 1
- The inverter is completely symmetrical in terms of horizontal dimension and therefore we expect to see differences in its ascent and descent times (due to differences between PMOS and NMOS).

Then, we extract the model we designed through the ext2spice command and since there was no design error the extraction was successful and the models obtained were correct. In the models other than the analytical dimensions of the transistors we also have values for the inverter input and output capacitors.

The result down below :

```
M1 out in vdd vdd CMOSP w=3u l=2u
```

```
+ ad=19p pd=18u as=19p ps=18u
```

```
M2 out in gnd gnd CMOSN w=3u l=2u
```

```
+ ad=19p pd=18u as=19p ps=18u
```

```
C0 out gnd 2.1F
```

```
C1 in gnd 5.3F
```

## Exercise 2

In Exercise 2 we continue with the results from Exercise 1 and do a simulation at NGSPICE to find the required times.

The **Inverter\_simulation.txt** file contains in detail the implementation of the circuit with the values for  $V_{dd} = 2.5V$  and  $V_{in} = (pulse) 0-2.5V$ .  $T_{rise, fall} = 200ps$  are used for  $V_{in}$  with a width of 8ns.

A sufficiently large pulse width was selected for the simulation so that we can see a complete rise in voltage  $V_{dd}$  and the difference between the times counted is clear.

In addition, these cards were used in the code:

**.include** to include the MOSIS models and the inverter we created in MAGIC.

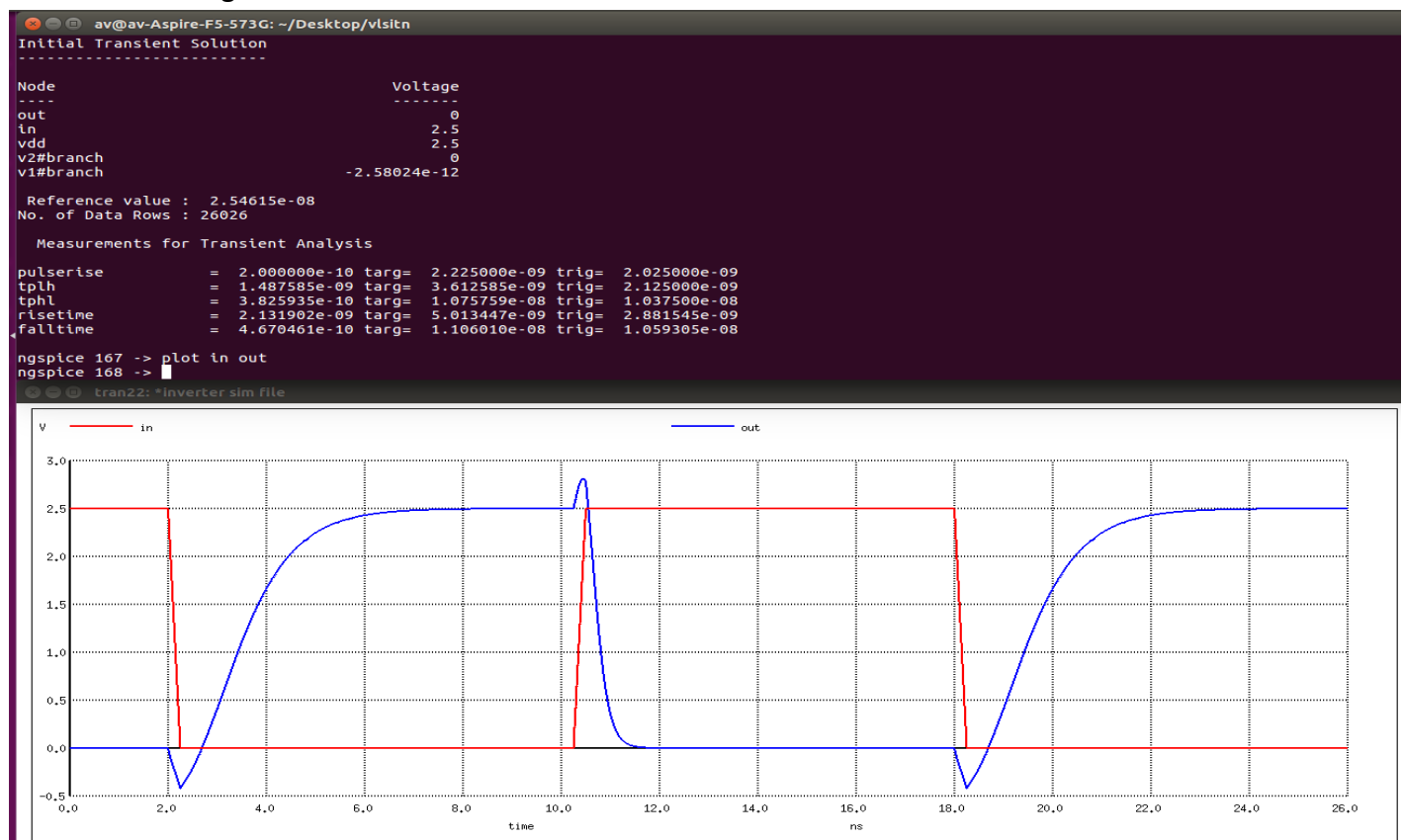
**.control** to set values to print the output file containing the waveforms.

**.measure** to measure the time values required.

**.ic** to set initial conditions in the circuit since we have capacitors at the input and output (although they are not needed)

**.probe** to plot the values of in and out.

Below is the image with the simulation results:



From the image and the measurements it seems that the rise time is much longer than the fall time (the same happens in the respective propagation delay)

This is due to the size of the PMOS transistor which is the same as the NMOS. Since the mobility of the holes is much smaller than that of the electrons we result in a much smaller current being conducted. The PMOS charges the capacitor at the output much slower than it is discharged by the NMOS and so we observe these waveforms with asymmetric times.

There are also some "spikes" in the fall and rise of the inverter value when changing the input voltage, which is due to the parasitic capacities present in the circuit.

Down below some time measurements

$t_{\text{rise}}$	2.13ns
$t_{\text{fall}}$	0.46ns
$t_{\text{plh}}$	1.48ns
$t_{\text{phl}}$	0.38ns

## Conclusion

Based on the design and options at MAGIC and our theoretical knowledge, it was predicted that the inverter would have time differences in the 1st exercise.

Indeed in the 2nd exercise the hypotheses were confirmed and we observed the different times in NGSPICE.

The simulation code, MAGIC files, and images are included in the folder that contains this report.