HY330 –VLSI Digital systems

Exercise set 2

8/11/2019

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Exercises 1,2,3 will use MOSIS-TSMC 0.25μm process transistor models at SPICE level 3.

PMOS and NMOS have W=3μm, L=2μm and Vdd = 2.5V.

If somewhere there is a difference in a voltage or dimension then it will be stated.

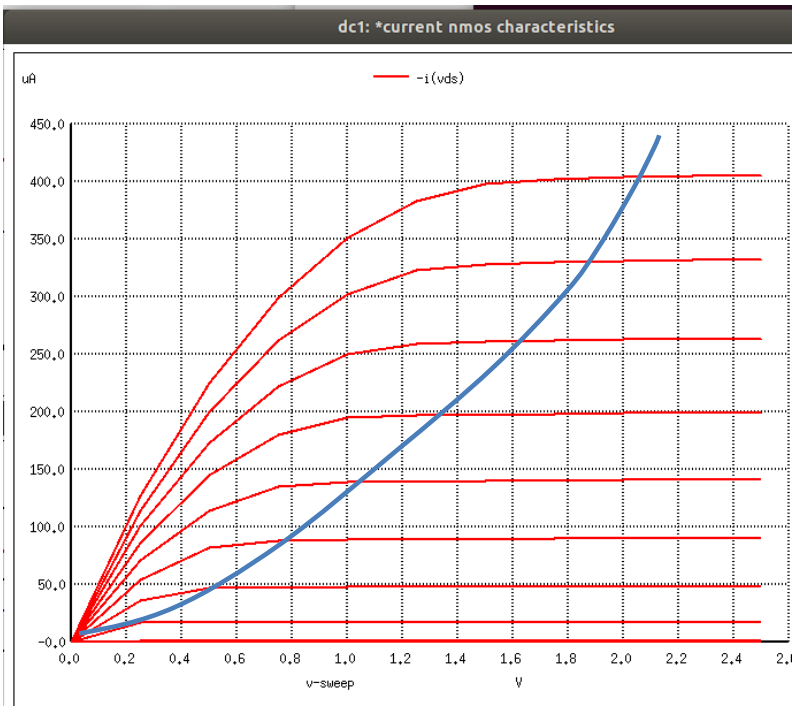
Exercise 1

Ids/(Vds, Vgs) Plots

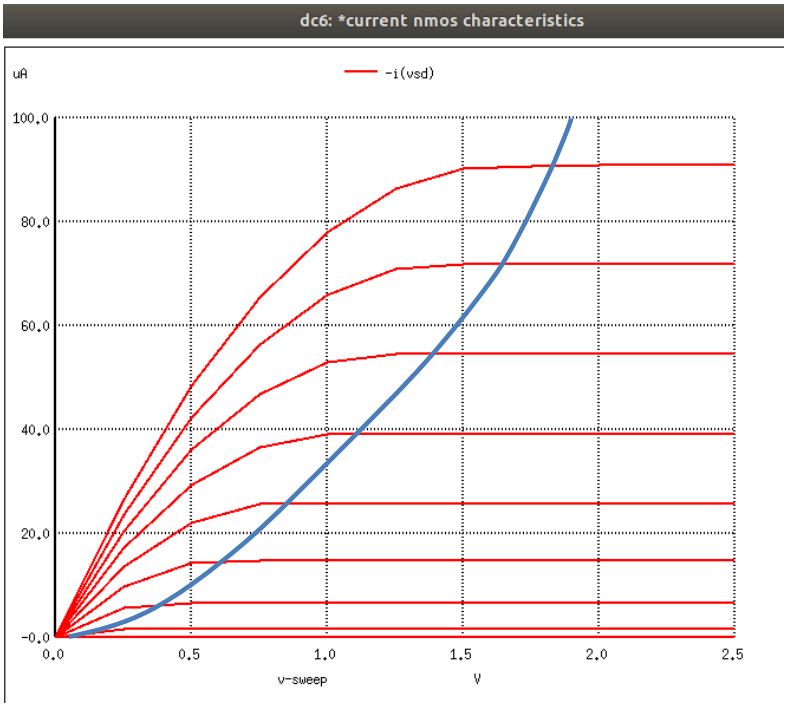
α) In this part we want to do static DC analysis on NMOS and PMOS transistors.

Initially the current characteristics for the various values of V_{GS} for NMOS and V_{SG} for PMOS relativ to V_{DS} and V_{SD} respectively.

For the NMOS:



For the PMOS



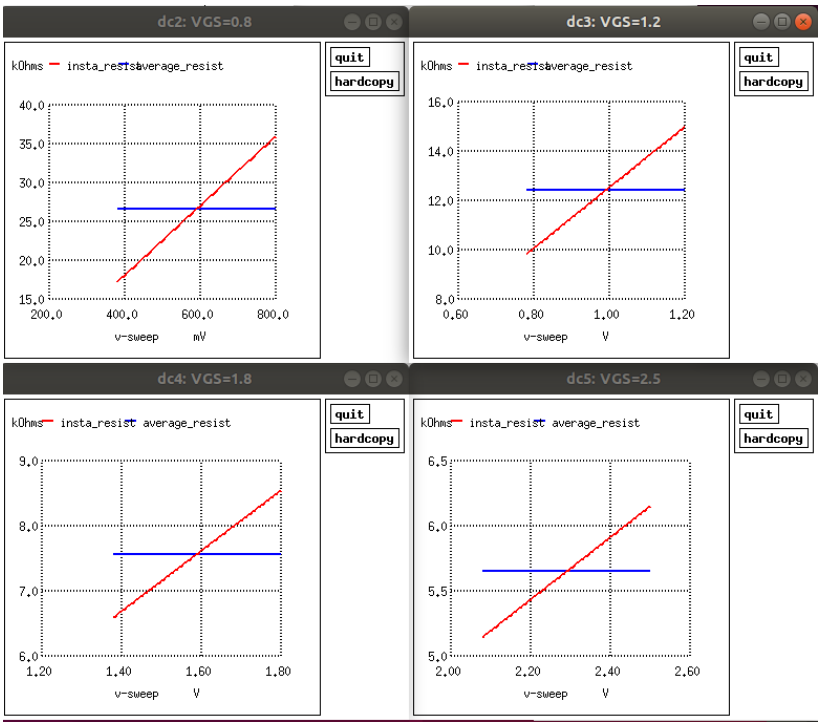
It seems that the current driven by the NMOS is in any case several times greater than the current of the PMOS, which is due to the greater mobility of the electrons than that of the holes.

In addition we can see that the distances between the plots do not have a constant distance between them , but constantly increasing which is due to the quadratic dependence toVGS when we are in the saturation region.

Finally, the points of intersection of the plot with the blue line in each shape is the point where we have the entrance to the saturation region. (meaning the (V_{GS}-V_T) point).

β) For the next part we have to measure the instantaneous resistance and the equivalent resistance (or average resistance) in the saturation region for each transistor.

For the NMOS:



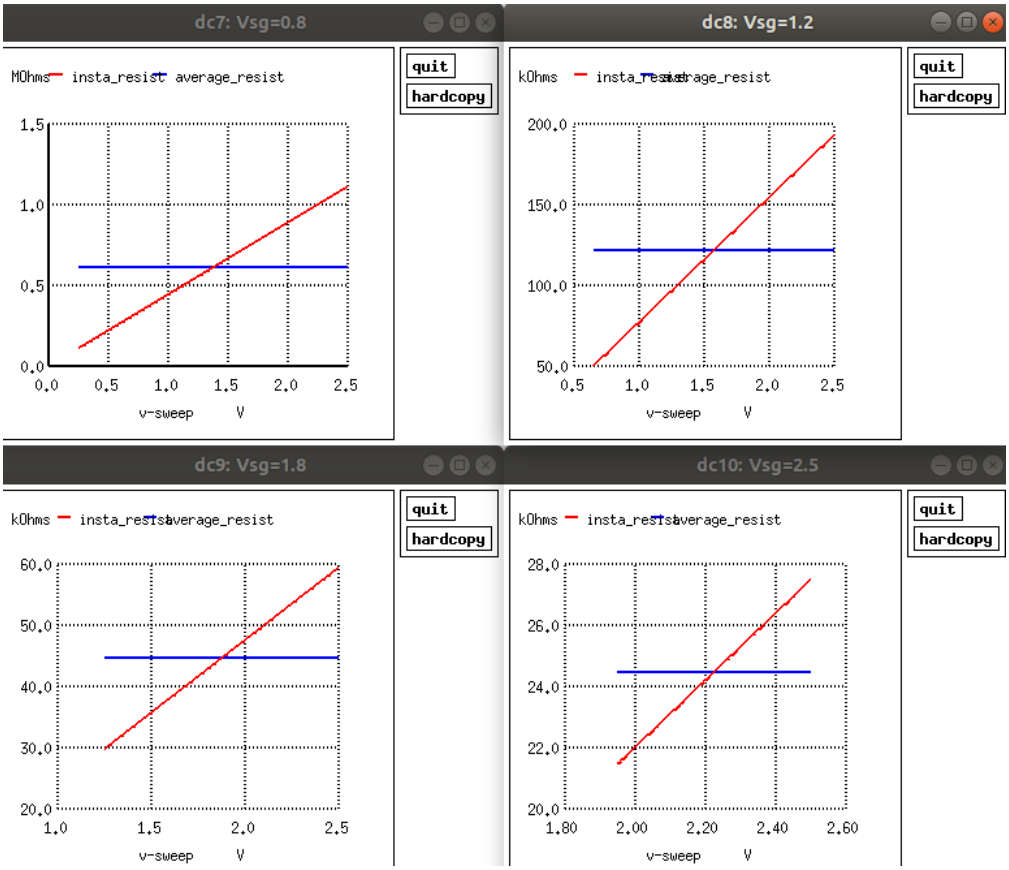
The average resistances are:

- 5.64κΩ for 2.5V
- 7.57κΩ for 1.8V
- 12.40κΩ for 1.2V
- 26.59κΩ for 0.8V

The increase in resistance seems to be linear, which is confirmed by the fact that in the saturation region the current is almost constant for changes in V_{DS} ($R = V_{DS}/I_{DS}$ => $R = \alpha * V_{DS}$ where $\boldsymbol{\alpha}$ constant).

In addition as V_{GS} the current that the transistor can conduct increases (since the dependence in the saturation region is only from V_{GS}) therefore the resistance decreases (instant and average).

Down below the plots for the PMOS:



The average resistances arre:

- 24.48κΩ for 2.5V
- 44.62κΩ for 1.8V
- 121.81κΩ for 1.2V
- 611.74κΩ for 0.8V

We see similar results in PMOS with the only difference being that we have much higher resistance due to the lower constant K_P (the mobility of the holes is less than that of the electrons), resulting in less current and then a larger resistance.

Finally, at 0.8V where we approach the threshold voltage we see a very sharp increase in resistance.

Equivalent Resistance RC Transistor

In this part we want to find the equivalent resistance to NMOS and PMOS by charging a capacitor and discharging respectively.

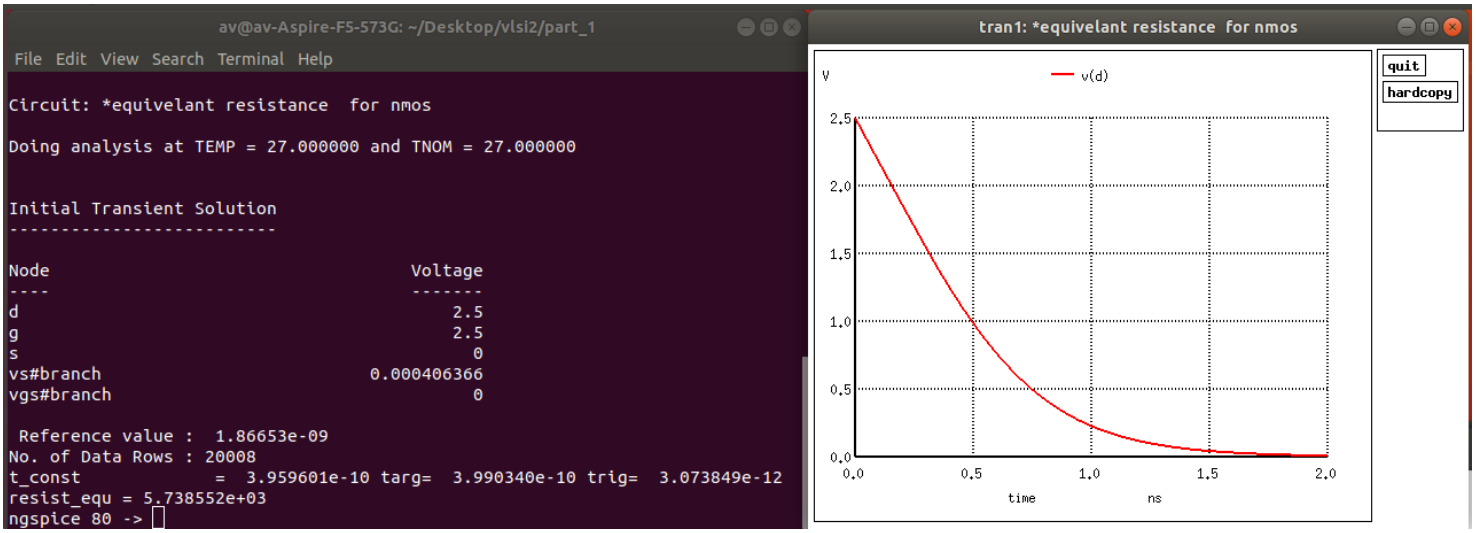
To achieve this we use the equation $t = ln2*R*C$,whete C the capacitance we charge, R the equivelant resistance and t the time for the capacitor to go from 100% ->50% in voltage level (or 0% ->50%) .

So if we do a transient simulation then since we can know the time, the capacity C is known and $ln2 \cong 0.69$ the equation becomes:

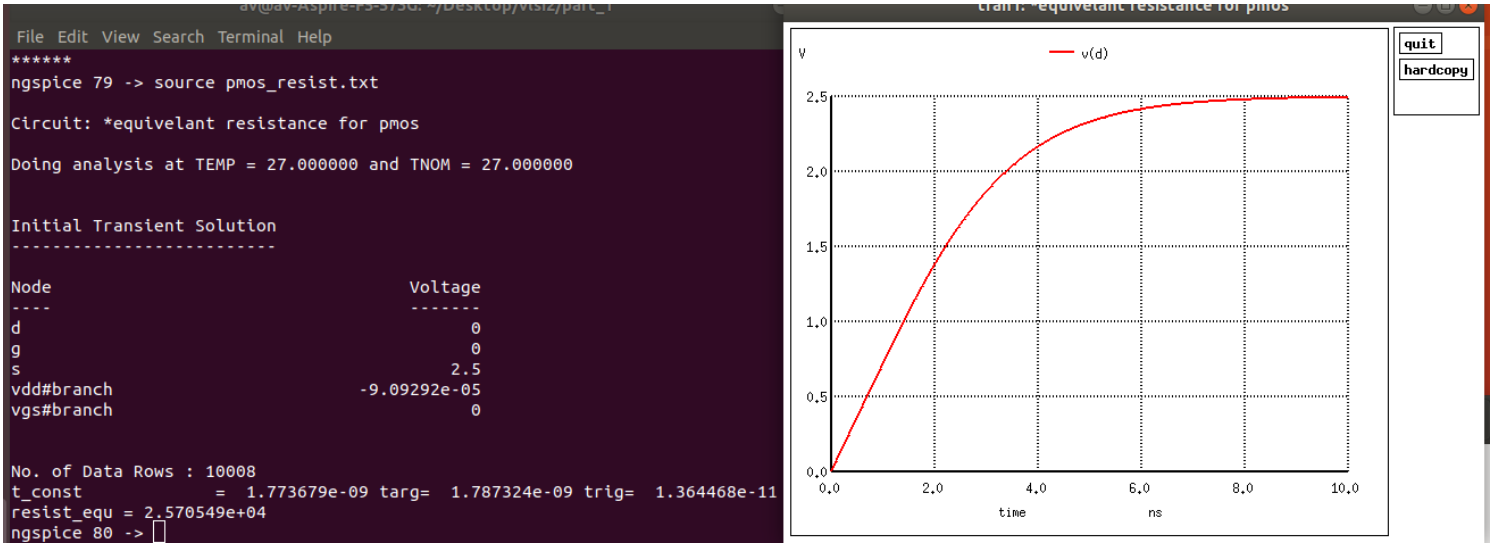
$$R_{eq} = \frac{t}{0.69 * 0.1p}$$

Down below the results of the simulation:

For NMOS



Για PMOS



As shown in the terminals of the two images the equivalent resistance for the NMOS is **5.73kΩ** and for the PMOS is **25.70kΩ**. The result is logical since the resistance of the PMOS must be higher because the constant K_p of the PMOS is about 5-6 times smaller than that of the NMOS.

Compared to the previous part, the resistance is very close to the average resistance for the saturation region (στην περίπτωση των 2.5V). This is because when discharging and charging the capacitor , we measure up to 50%, which is a value very close to the saturation region for each transistor.

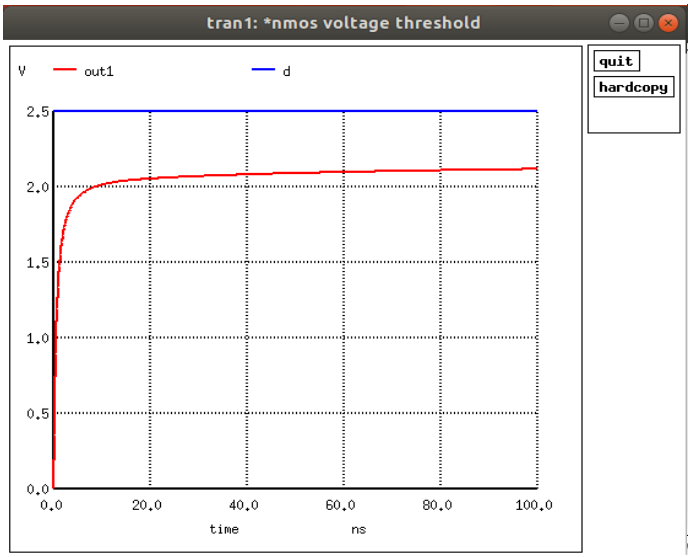
As a result, the current remains constant, if not constant - high enough for the resistance to be very close to the average resistance of the transistor in the saturation region.

Exercise 2

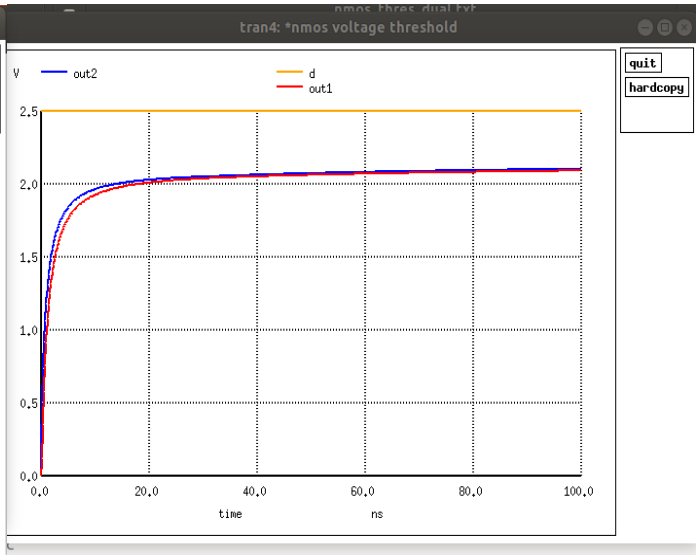
In this exercise we will try to charge a capacitor with NMOS and discharge it with PMOS to see the voltage drop phenomenon.

The NMOS results:

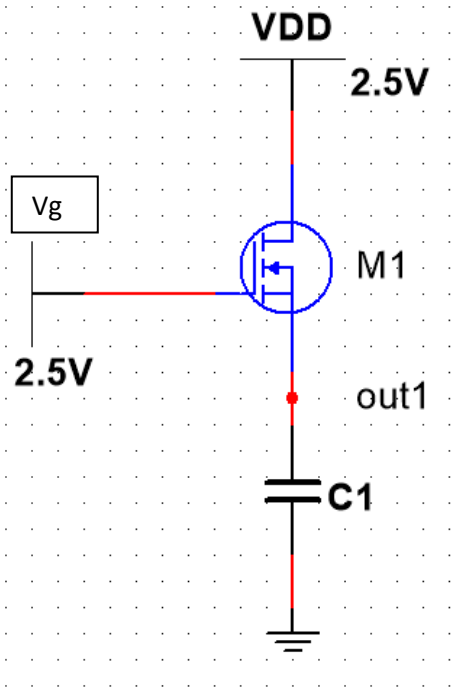
For one NMOS

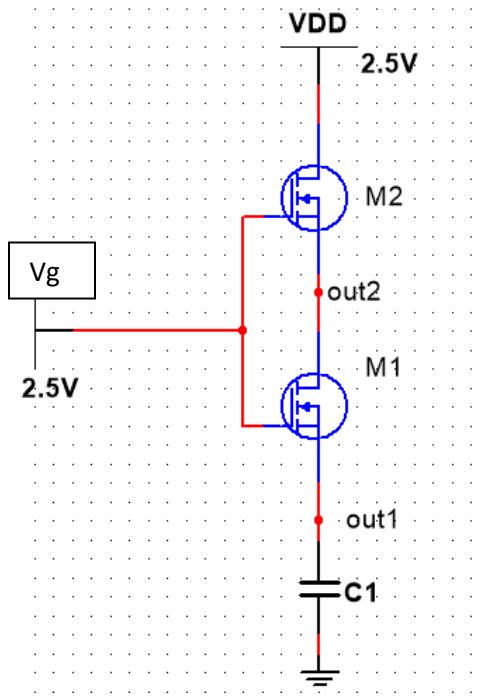


For 2 NMOS in series



And the connecticity diagrams:

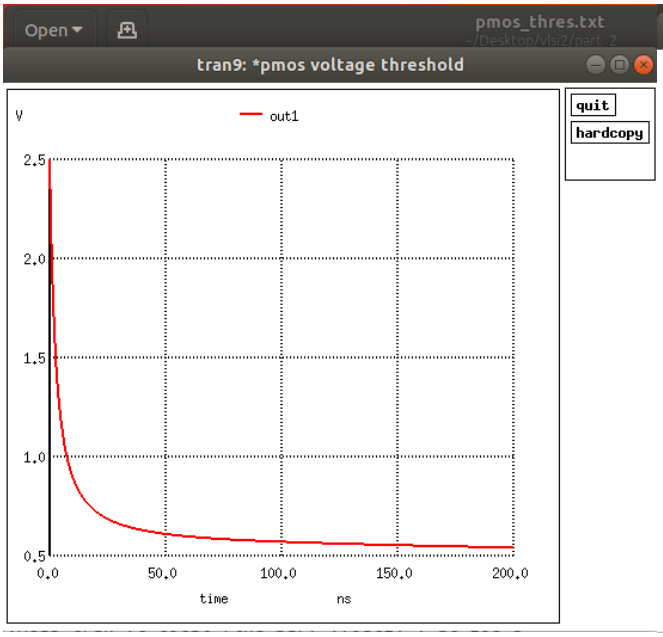




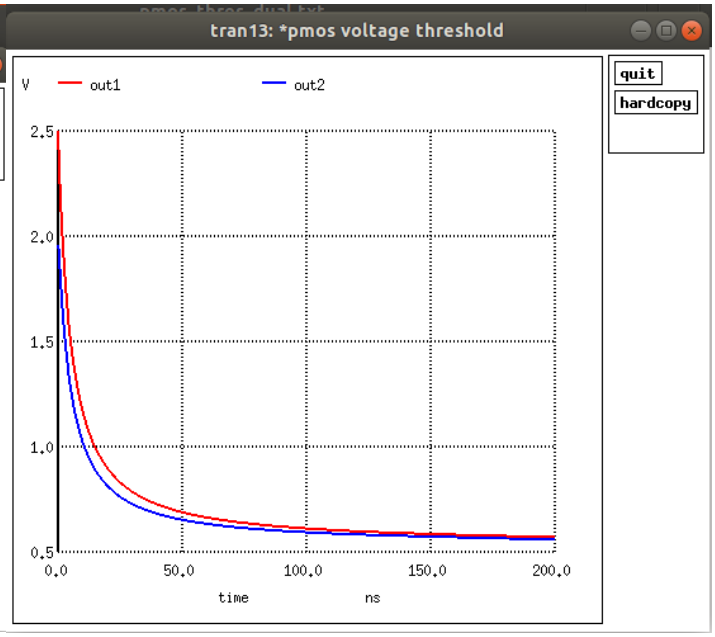
As can be seen in each case the voltage drop tends towards the NMOS threshold voltage (0.42V) . Specifically in the single NMOS the drop is 0.41V at 50ns and in both it is 0.43V at 50ns again (at the out1 node in each figure).

The PMOS results:

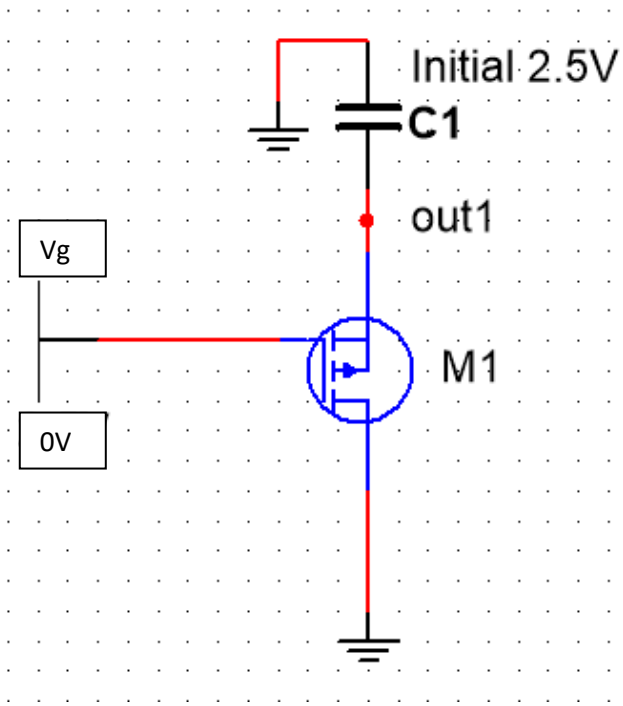
For one PMOS

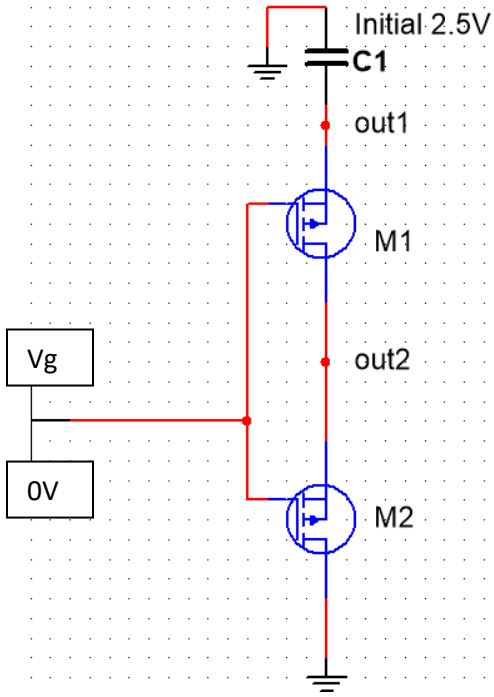


For 2 PMOS in series



And the connecticity diagrams:





Similar results are observed for PMOS (threshold voltage is 0.55 in magnitude). Specifically in the single PMOS the drop is 0.57V at 100ns and in both it is 0.58V at 100ns again (at the out1 node in each figure, so the voltage drops are actually negative).

In general, in all 4 cases because the voltage at the node out1 and out2 is variable then Vgs will also be variable and will start decreasing for NMOS and increasing at PMOS respectively, until it reaches the threshold voltage of each transistor.

When the transistors reach their threshold voltage then they turn off and we have the voltage level of the capacitor to remain constant at V_{DD} -V_{TN} for the NMOS and $|V_{TP}|$ for the PMOS.

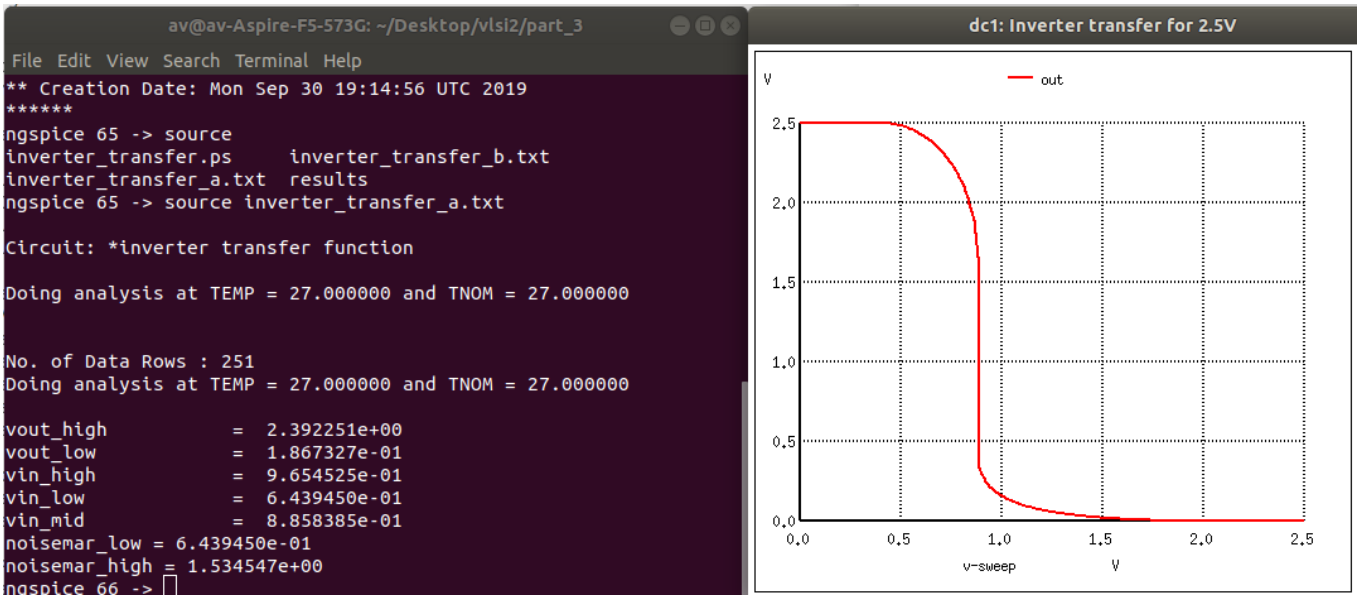
This explains the phenomenon voltage drop in NMOS and PMOS transistors.

Exercise 3

Transfer function Vout/Vin

In this part we want to do a DC analysis so as to export the voltage transfer characteristic of a CMOS inverter .

The results down below:



Based on the image and the results of the measurements we have an asymmetric transfer function and the noise margins have a large difference between themselves.

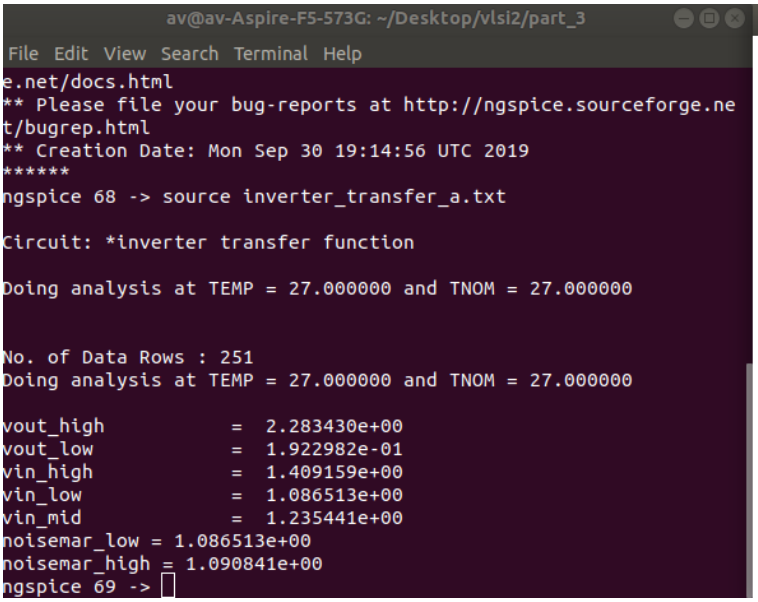
V_{OH}	2.392
V_{OL}	0.186
V_{IH}	0.965
V_{IL}	0.643
V_{M}	0.885
NM_{L}	0.643
NM_{H}	1.534

The results for the characteristic values of the inverter

This is because the transistors are the same size but the PMOS can conduct less current than the NMOS because the hole mobility is less than that of the electrons. This results in a faster discharge of the output capacitor than charging, hence the characteristic curve to be so.

To correct this we can change the width dimension of the PMOS transistor and increase it until we see symmetrical noise margins.

This will happen due to the linear dependence of the current that a transistor can conduct with the W / L ratio. So if we increase the channel width we will also increase the W / L ratio and correct the characteristic of the inverter.



V_{OH}	2.283
V_{OL}	0.192
V_{IH}	1.409
V_{IL}	1.086
V_{M}	1.235
NM_{L}	1.086
NM_{H}	1.090

The results for the characteristic values of the inverter with the width changed

Above are the results for PMOS with a width of 17u relative to the startring 3u (almost 6 times larger).

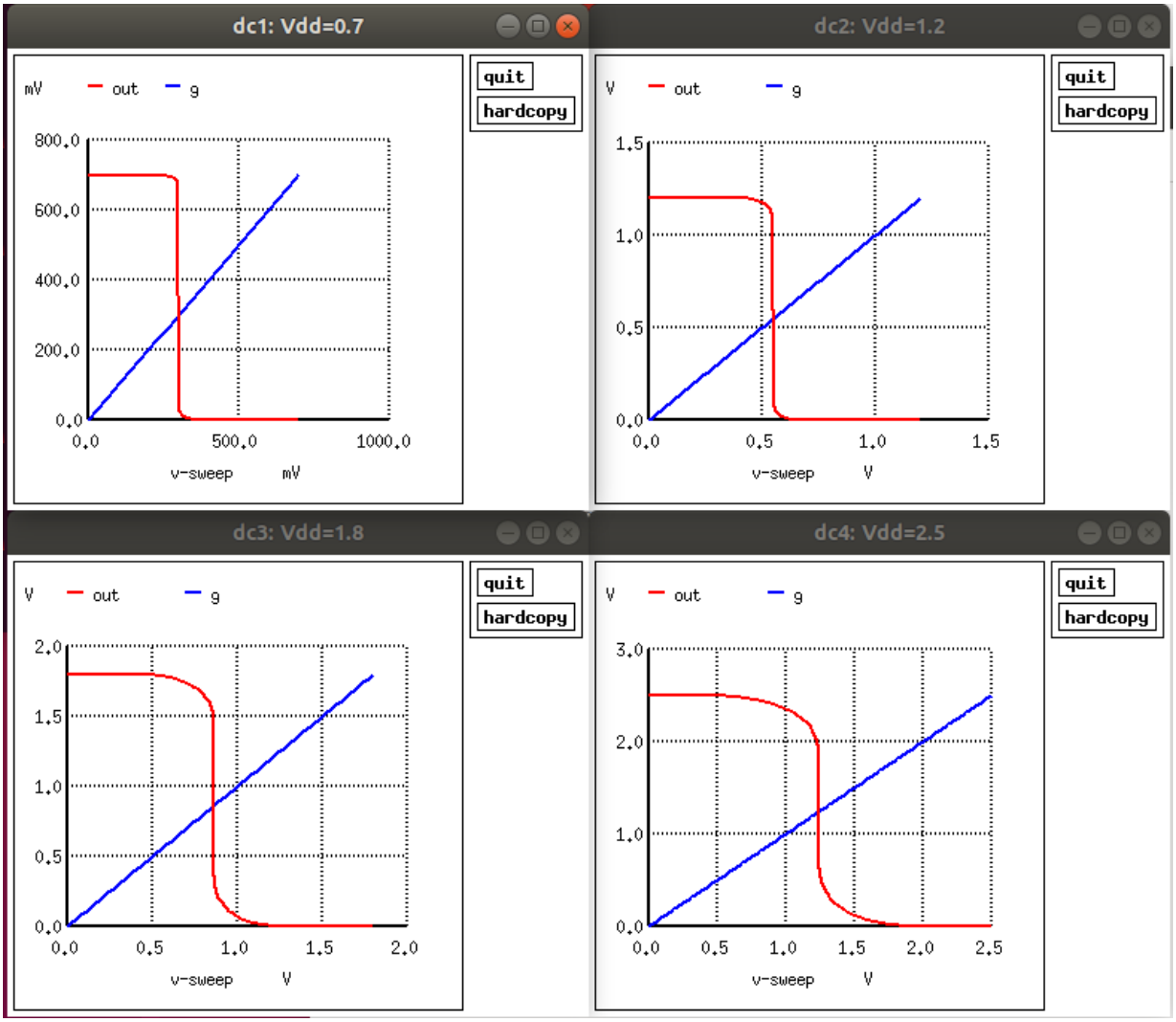
As it seems the voltage transfer characteristic has become completely symmetrical, the same for the noise margins but also the central point V_M .

Voltage scaling and Transfer function

Now, using the symmetric inverter (17u for the PMOS) from before we change V_{DD} και V_{IN} to 0.7V, 1.2V , 1.8V, 2.5V each time and check the noise margins,the average current and average power.

To achieve this in ngspice we use a control structure, **foreach**, which is repeated for each value we set to V_{DD} and V_{IN}. Within this structure we make the measurements in the noise margins, the current and power.

The results down below:



As can be seen with the gradual decrease of the voltage we have the phenomenon that the graph of the inverter becomes more and more abrupt and in a sense ‘digitized’ to 0 and 1 without intermediate states.

In addition from the shapes and the results of the measurements we see a gradual shift to the left of the curve resulting in the reduction of NM_L and increase of NM_H.

Παρακάτω τα αποτελέσματα για κάθε μέτρηση:

Vdd Value	**0.7**	**1.2**	**1.8**	**2.5**
NM_L	2.80e-01	5.14e-01	7.73e-01	1.08e+00
NM_H	3.90e-01	6.26e-01	8.43e-01	1.09e+00
Μέσο Ρεύμα	6.40e-10	2.23e-07	4.74e-06	1.90e-05
Μέση Ισχύς	4.48e-10	2.67e-07	8.53e-06	4.75e-05

As can be seen from the figure, low noise margins decrease and highs increase, but overall the desired inverter operating range is larger This is easily seen if we calculate the ratio $(NM_L+ NM_H)/V_{DD}$ where for 0.7V it is 95% while for 2.5V it is 86%.

Also, we have a smaller current and since the voltage always remains constant we have less power for each reduction of V_{DD} because we are getting closer and closer to the threshold voltage of each transistor.

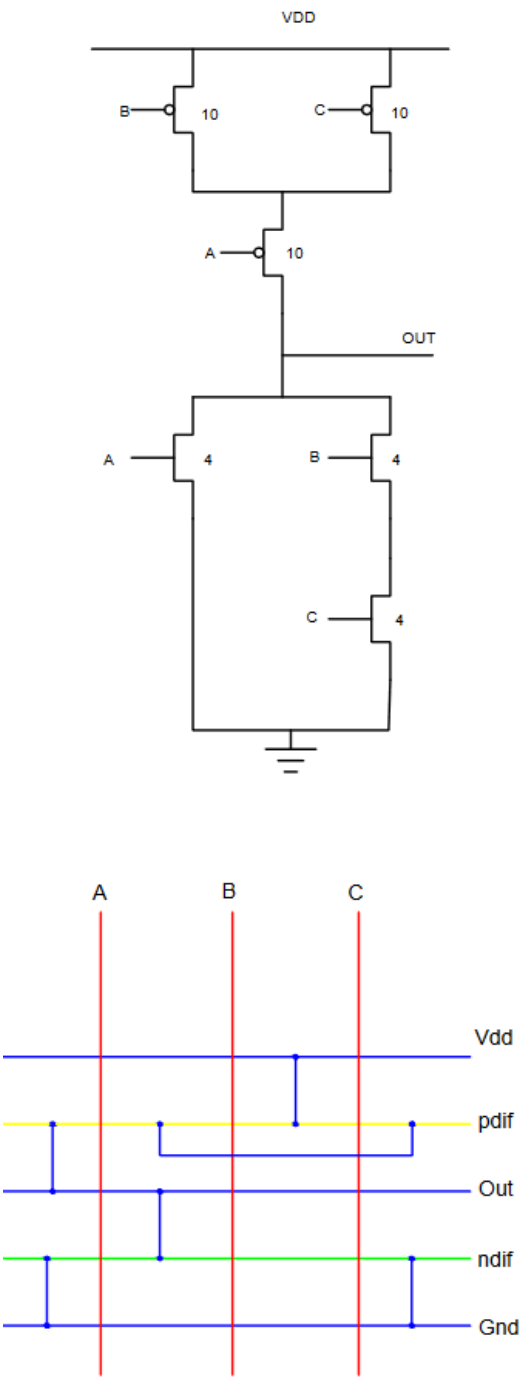
(In folder part_3, in the file results.txt the results of the measurements are stored)

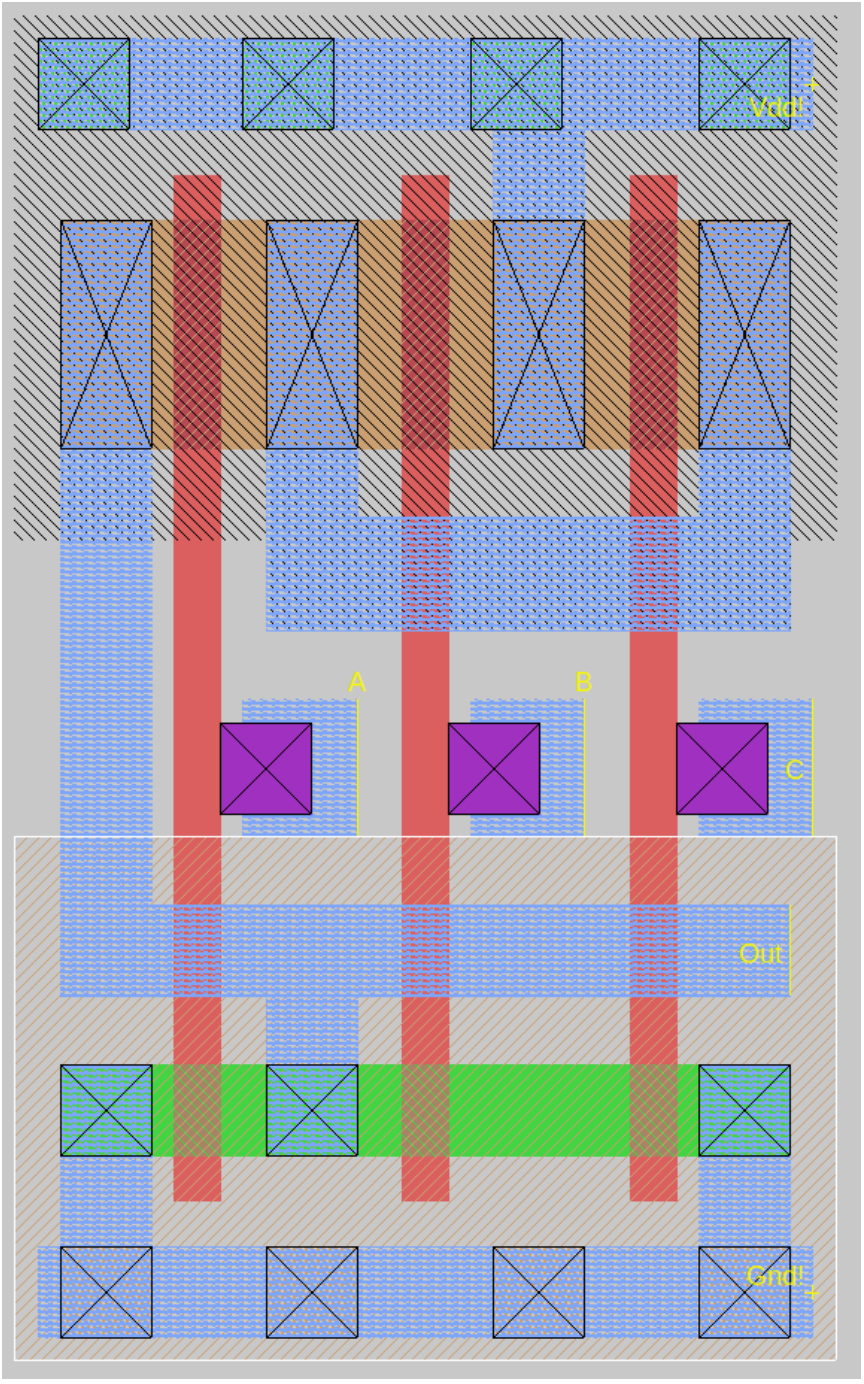
Exercise 4

Schematic, Line diafragms, Plan and definition of transistor sizes

Below we have the schematic diagram and plan for each binary function given to us.

For AOI21:





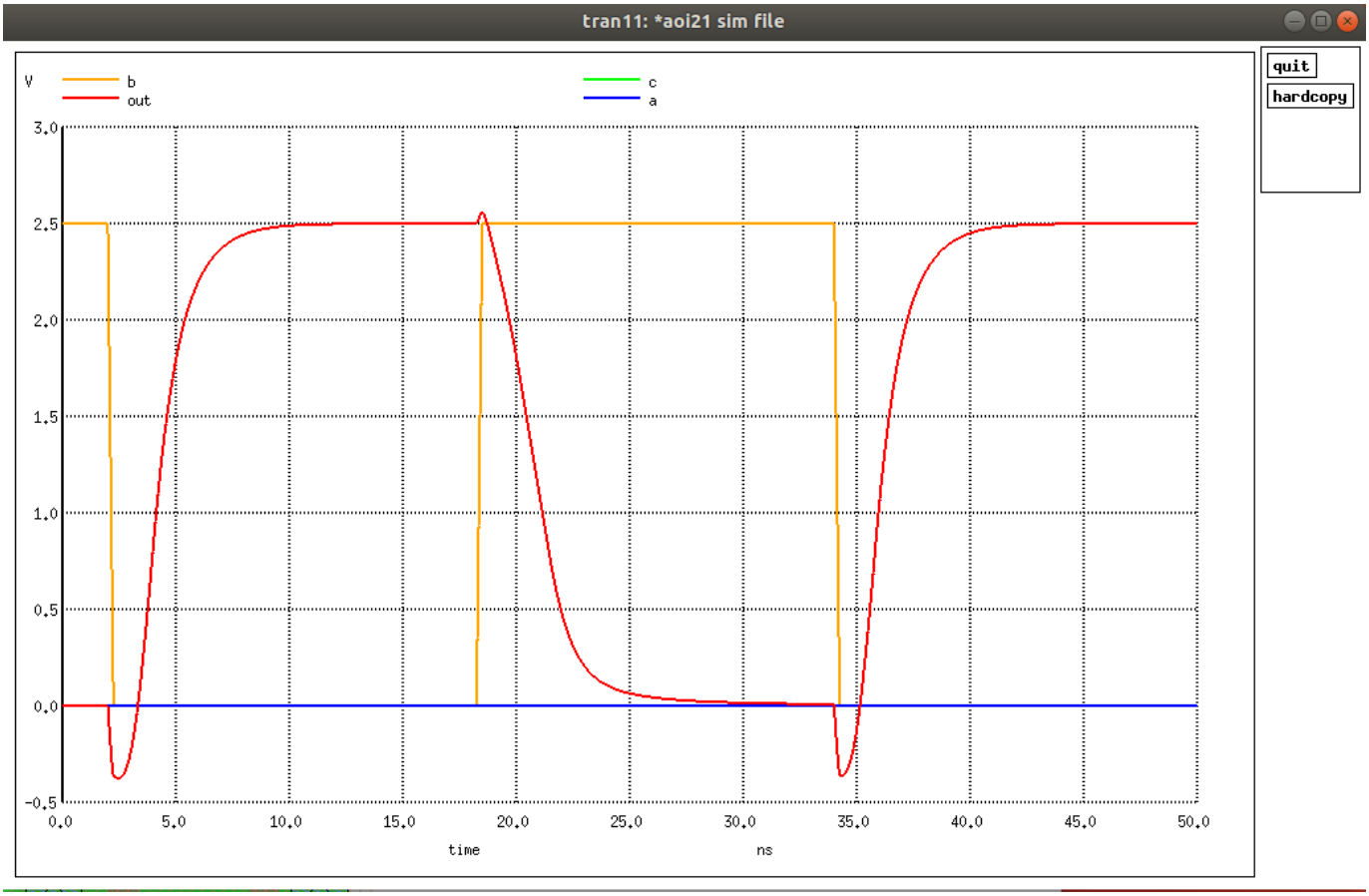
As it seems, the ratio 4 has been chosen for NMOS. The worst path is B-> C which has a resistance of 26 for a ratio of 1, so solving the ratio we have a = 26 / 6.5 = 4. Since we have found the worst path then for path A is set there as a ratio of 4, since we do not gain anything if we reduce the transistor. On the contrary we benefit since we do not lose in area, we have a smaller resistance and charge the output capacity faster.

We do the same for PMOS, with the only difference being that 31 / 6.5 does not produce an integer and it is not in our interest to change the width of the transistor. To satisfy the ratio we can approach the resistance of 6.5 kΩ if we make the ratio 5 so we have 31/5 = 6.2kΩ which is very close to the desired, changing only the

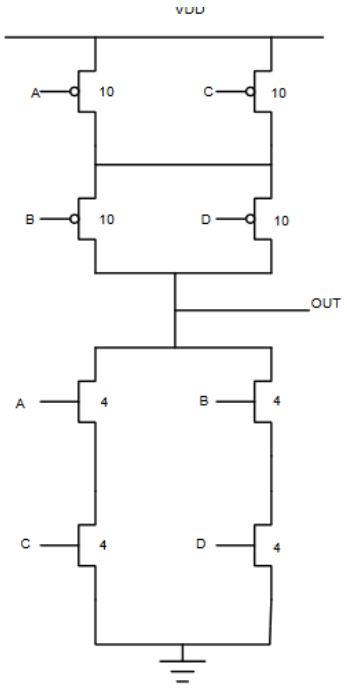
width of the PMOS. So respectively with the NMOS we will operate in multiples of 5 and since we have a worse path with two transistors, then we put a ratio of 10 in all.

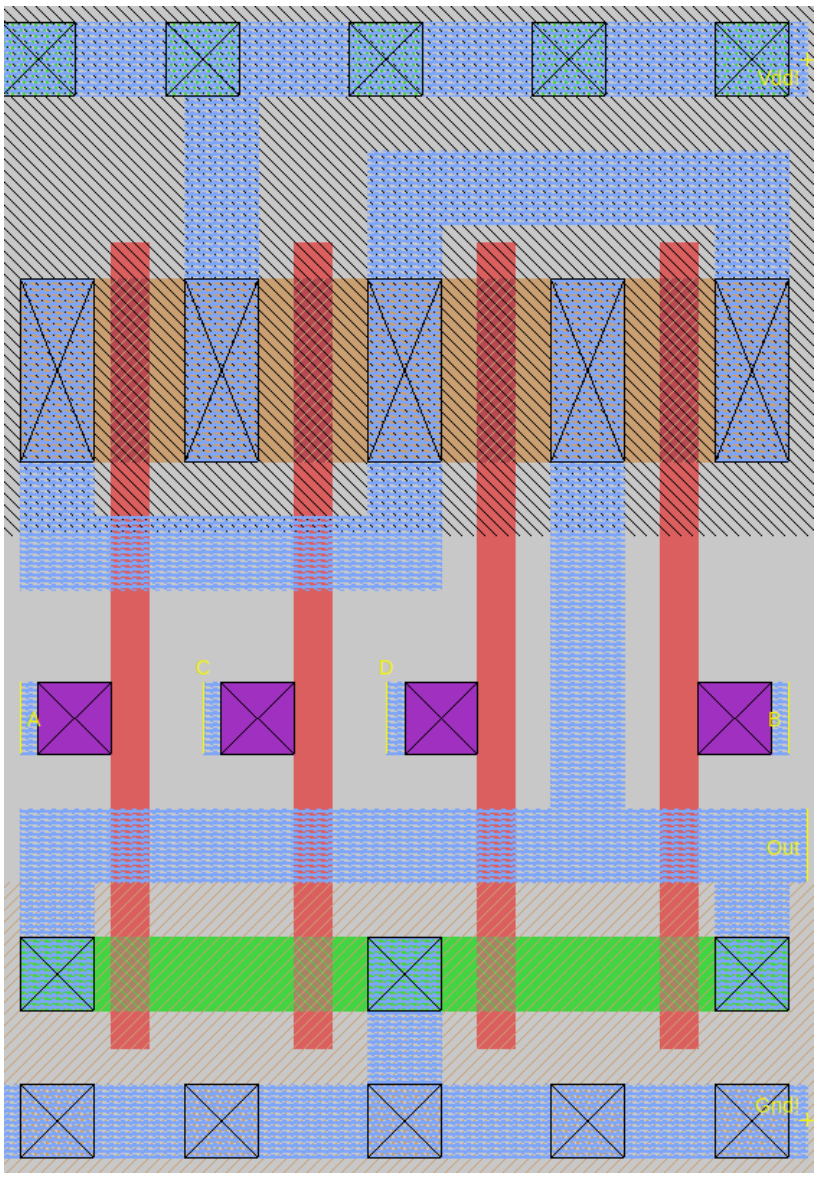
With the same reasoning we do for the reasons for the other functions.

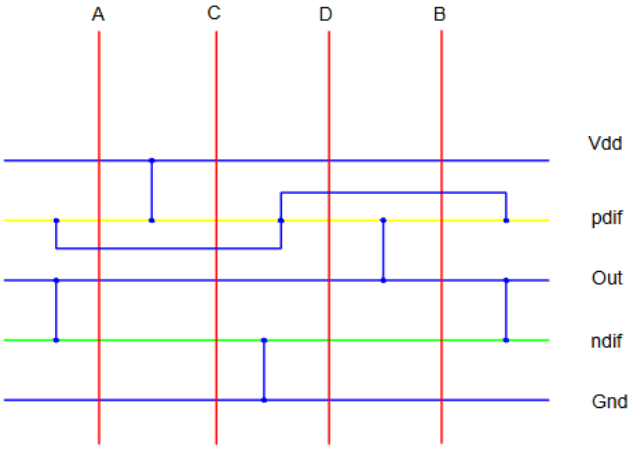
In the input simulation we have a constant A = 0, and a simultaneous pulse B = 1-> 0, C = 1-> 0 and we must see a transition to the output from 0 to 1 and vice versa.



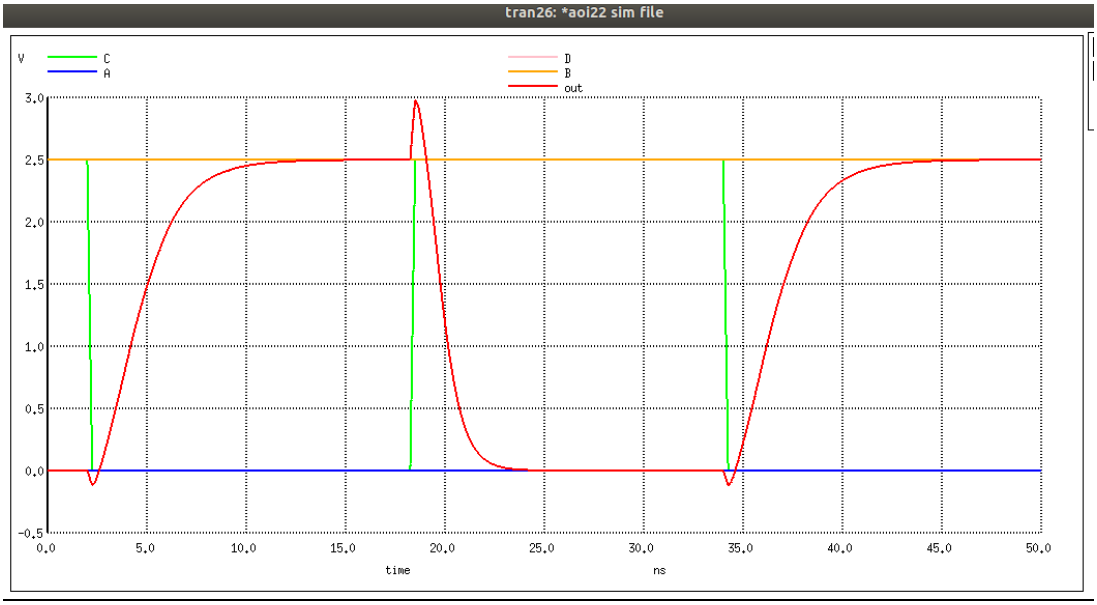
For AOI22:







In the input simulation we have constants A = 0 and B = 1, and simultaneous pulse C = 1-> 0, D = 1-> 0 and we must see a transition at the output from 0 to 1 and vice versa.

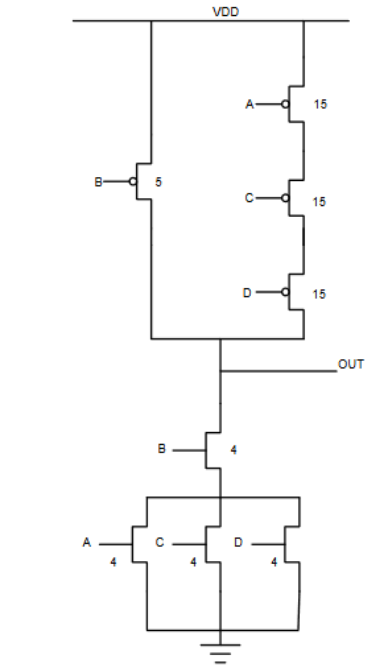


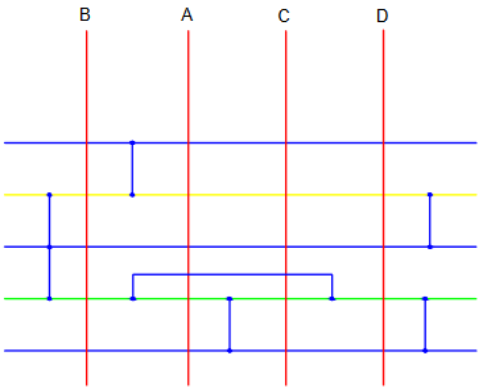
For OAI31:

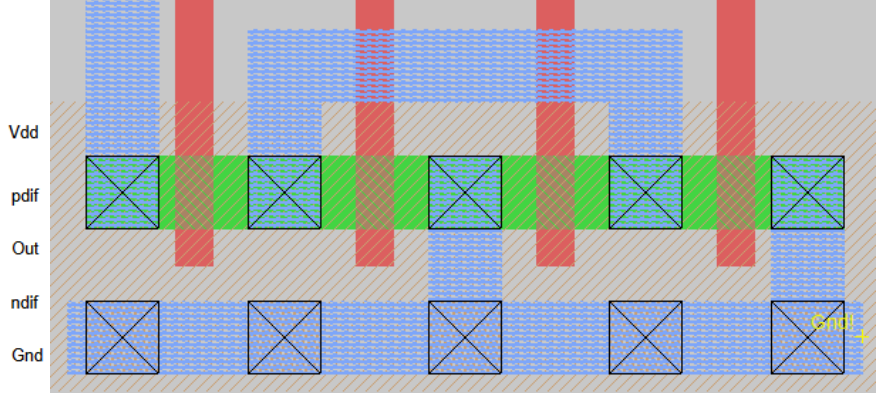
For this gate to reduce the number of transistors we have made some simplifications, in particular:

$f_{oai31} = (ab+b(c+d))' = (b(c+d+a))'$

In this way we have, from 5 transistors in each network, 4 transistors.

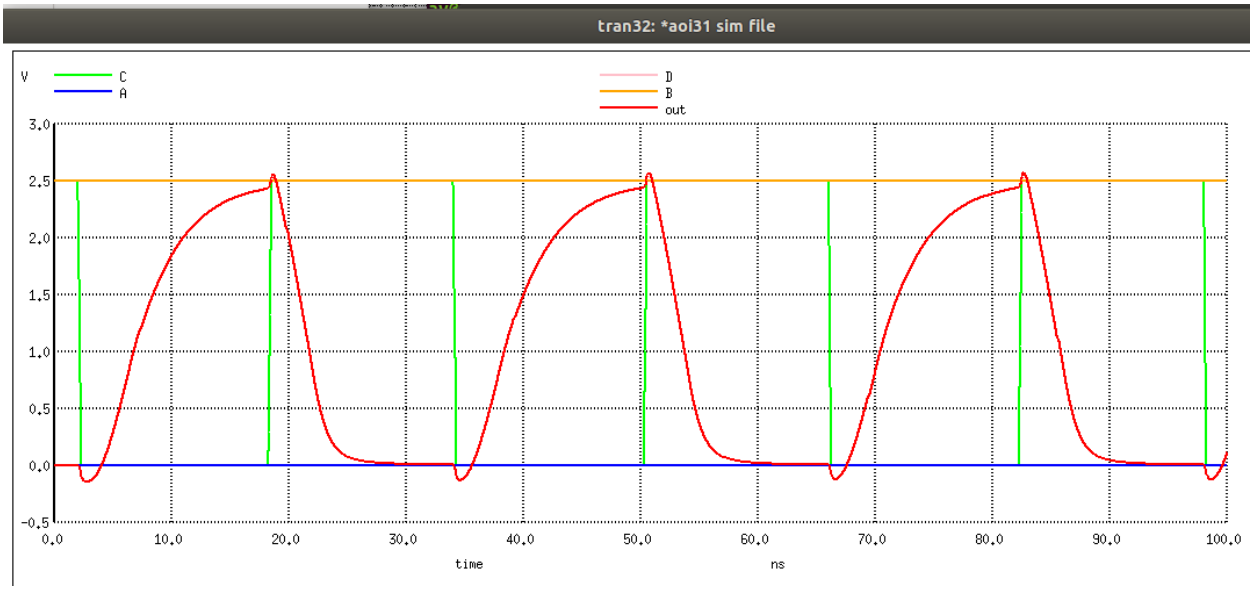






In this gate to have a smaller output capacity we reduce the ratio of PMOS A, although we do not gain in area.

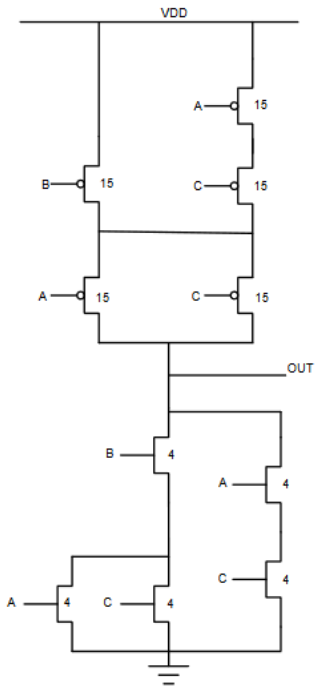
In the input simulation we have constants A = 0 and B = 1 and D = 0, simultaneous pulse C = 1-> 0 and we must see a transition to the output from 0 to 1 and vice versa.

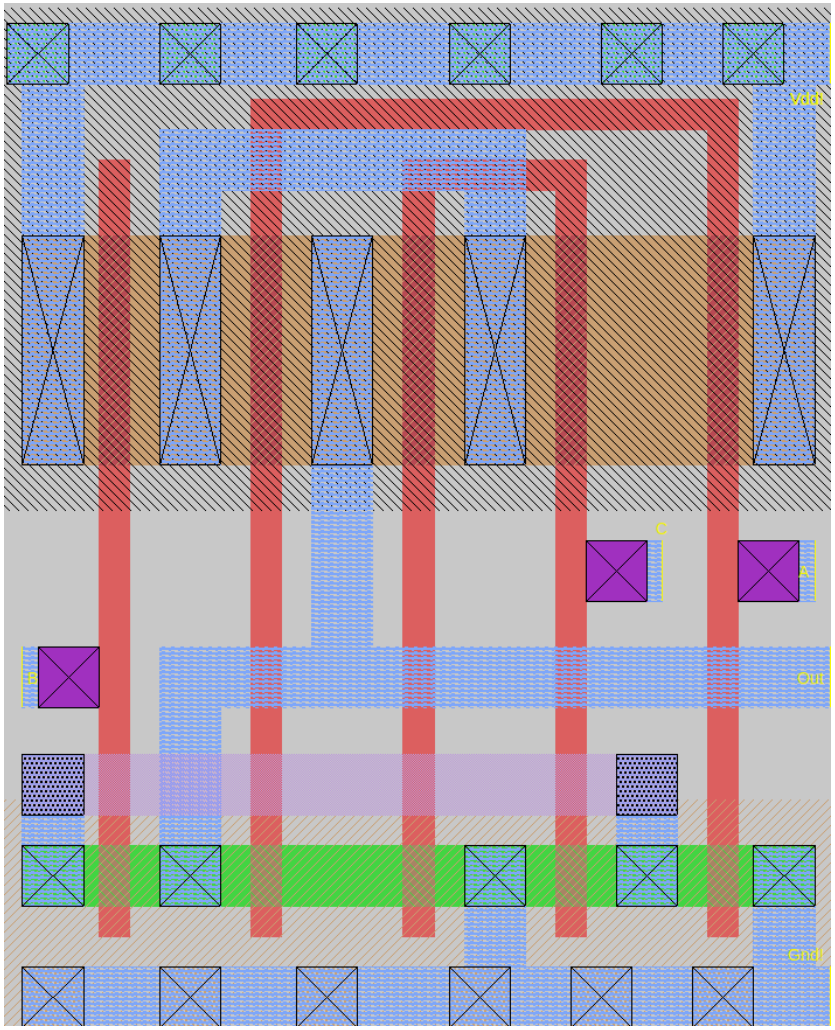


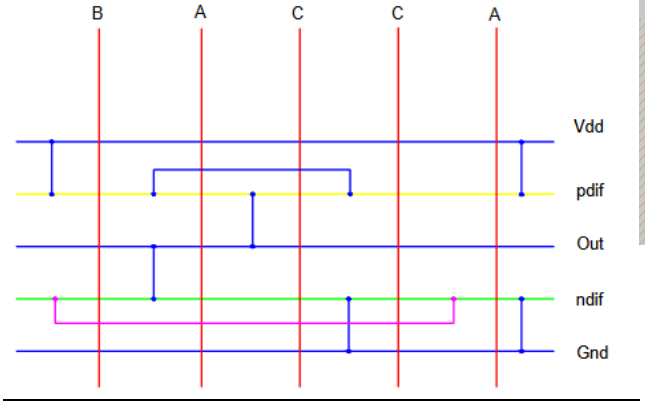
For maj:

We simplify again as in OAI31 ->f_{maj} = (ac+bc+ab)'= (b(a+c)+ac)'

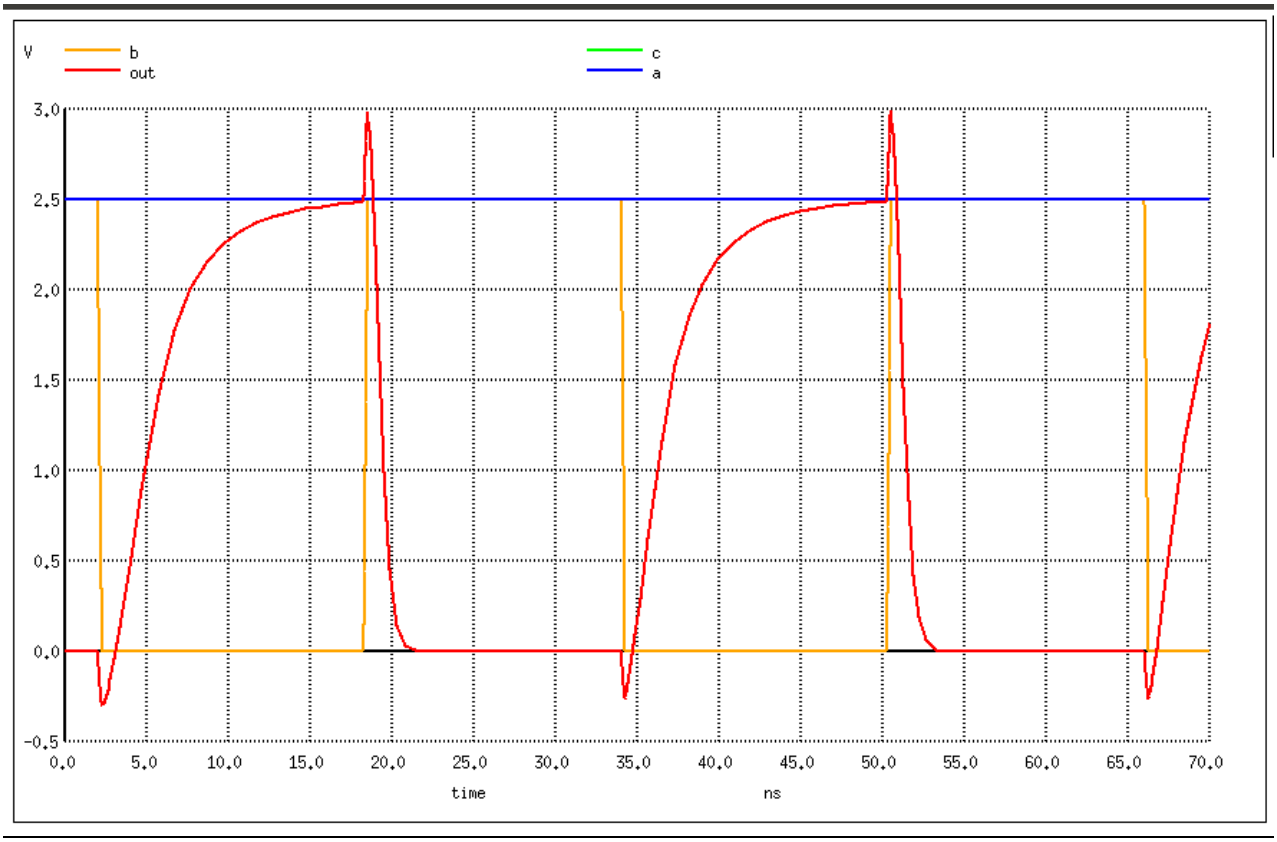
In this way we have, from 6 transistors in each network, 5 transistors.





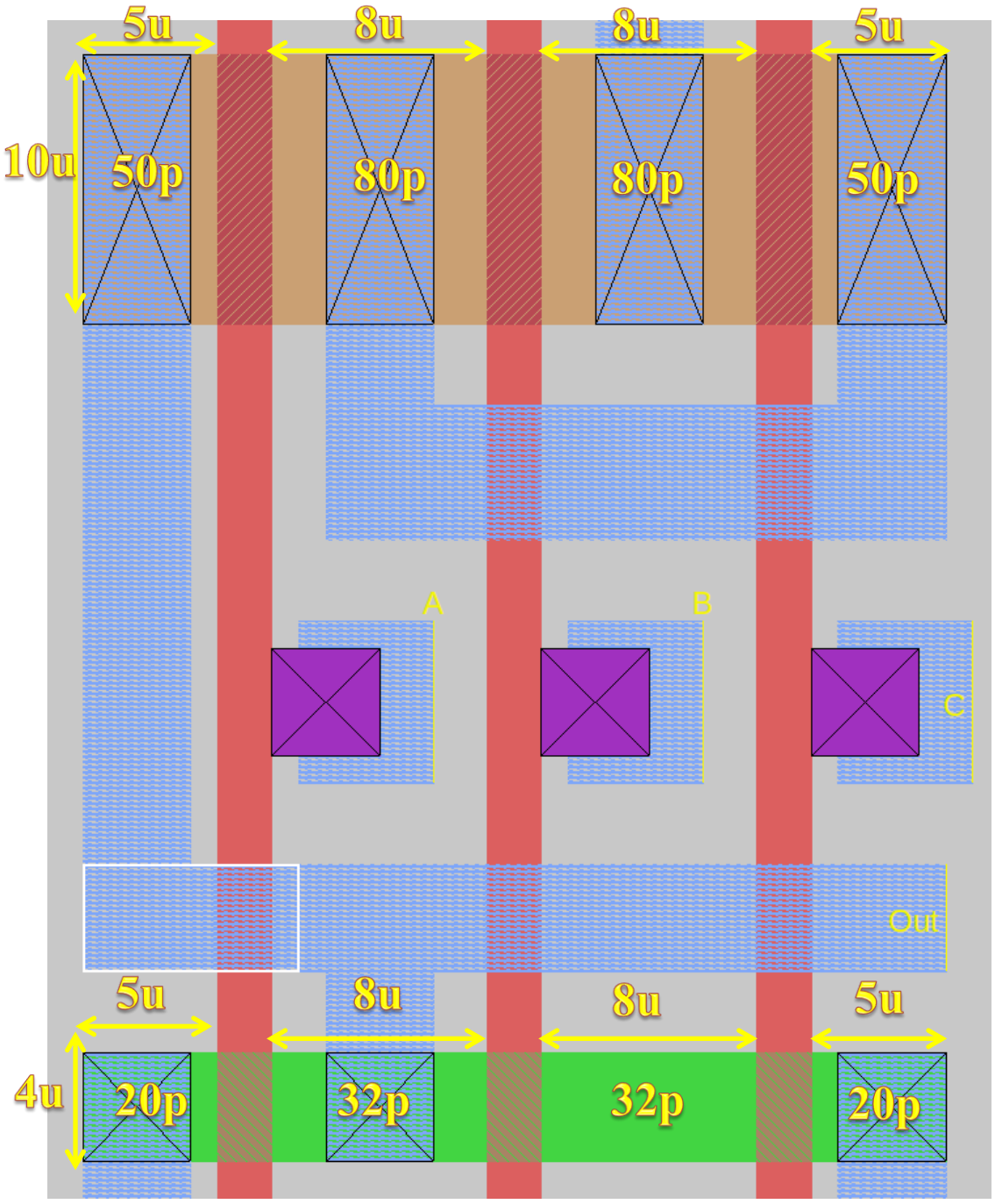


In the input simulation we have constant A = 0, and simultaneous pulse C = 1-> 0, B = 1-> 0 and we must see a transition at the output from 0 to 1 and vice versa.



Capacitance analysis

We return to the gate AOI21 and we have its plan in magic with dimensions and areas to find the capacities at the exit:



So for PMOS :

P_P = 10u+5u+5u =20um (without the dimension resting on the gate).

A_P = 5u *10u = 50um^2 .

And the NMOS :

P_N = 8u+8u =16um (without the dimension resting on the gate).

A_N = 8u *4u = 32um^2 .

The rest that do not rest on the metal **out** we ignore since we only ask for the capacities that appear at the output.

So for PMOS:

$C_{P,diff} = C_{bottom} + C_{sw} = K_{pj}*C_j * A_P + K_{pjsw}*C_j * P_P$

$= 2 * 0.79 *(10^{-15}/10^{-12}) *50*10^{-12} + 0.28 * 0.86 *(10^{-15}/10^{-6}) *20*10^{-6} =$ **83.816 Ff**

And the NMOS :

$C_{N,diff} = C_{bottom} + C_{sw} = K_{nj}*C_j * A_N + K_{njsw}*C_j * P_N$

$= 2 * 0.57 *(10^{-15}/10^{-12}) *32*10^{-12} + 0.28 * 0.61 *(10^{-15}/10^{-6}) *16*10^{-6} =$ **39.2128 Ff**