CSSE4010 - 2023 Semester 2 Lab 1
PRAC 1

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Lab Session attended:
Wednesday 26 July 2022, 10am - 12am
Wednesday 3 August 2022, 10am - 12am

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1 Introduction

The purpose of this practical exercise is to acquire a fundamental understanding of Vivado and learn how to code in Vivado. The main objective is to design a system consisting of two AND gates and one OR gate, with a self-checking testbed to detect errors in the system.

2 Design Description

This represents a design involving two AND gates and a single OR gate, incorporating four inputs and generating three outputs.

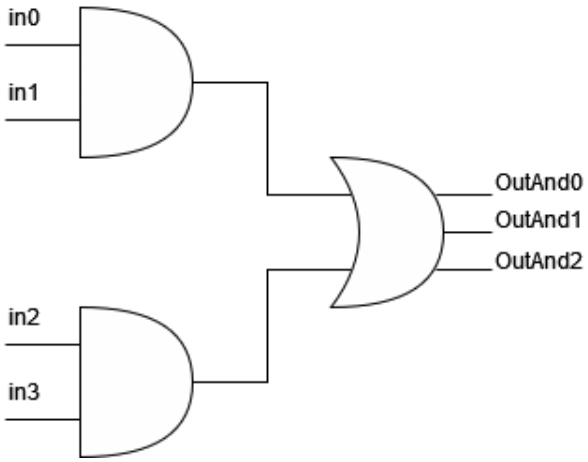

Figure 1: Block diagram of the designe

3 Simulation Results

The first simulation aimed to test a basic AND gate with two inputs and one output. The results of this simulation are displayed below.

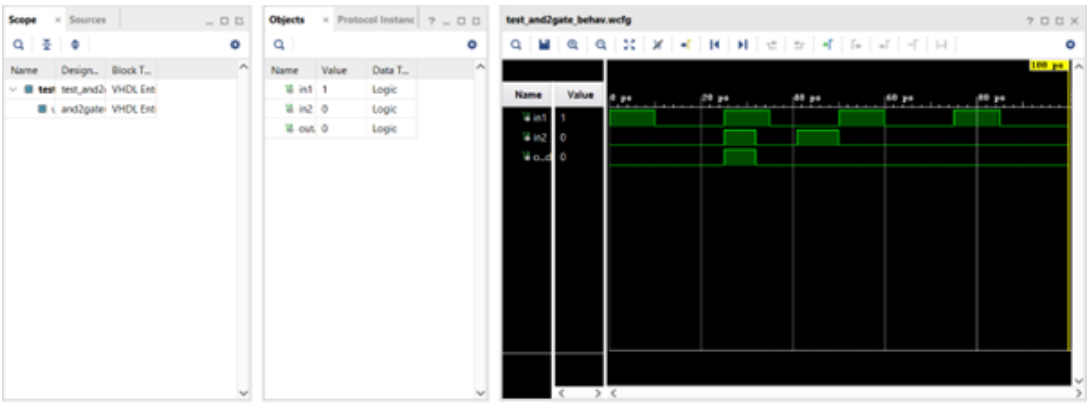

Figure 2: Simulation of one AND gate

The second simulation involved simulating two AND gates and one OR gate with 4 inputs and 3 outputs.

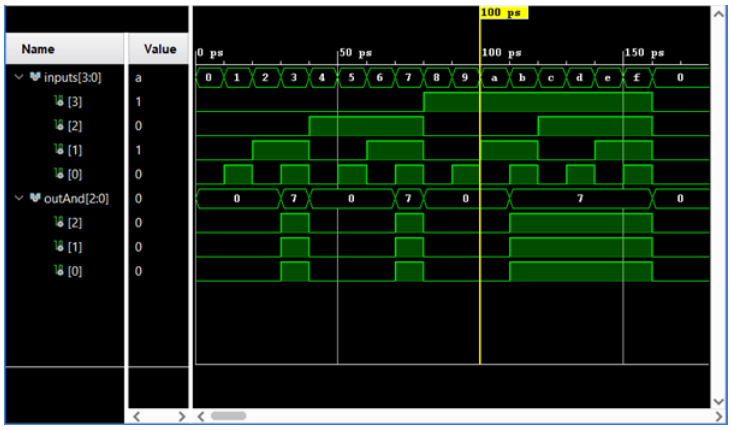

Figure 3: Simulation of two AND gates and one OR gate

In the third simulation, a gate delay of 2 ps is incorporated to analyze the effects of this alteration. The modification is represented as follows: "outAnd <= in1 and in2 after 2 ps;".

Figure 4: Simulation of two AND gates and one OR gate with gate delay

In the fourth simulation, we test how well the testbed can catch mistakes by purposely making a change in the design. For example, we switch the line "outAnd <= in1 and in2;" to "outAnd <= in1 or in2;", and then we check what happens with the testbed's output.

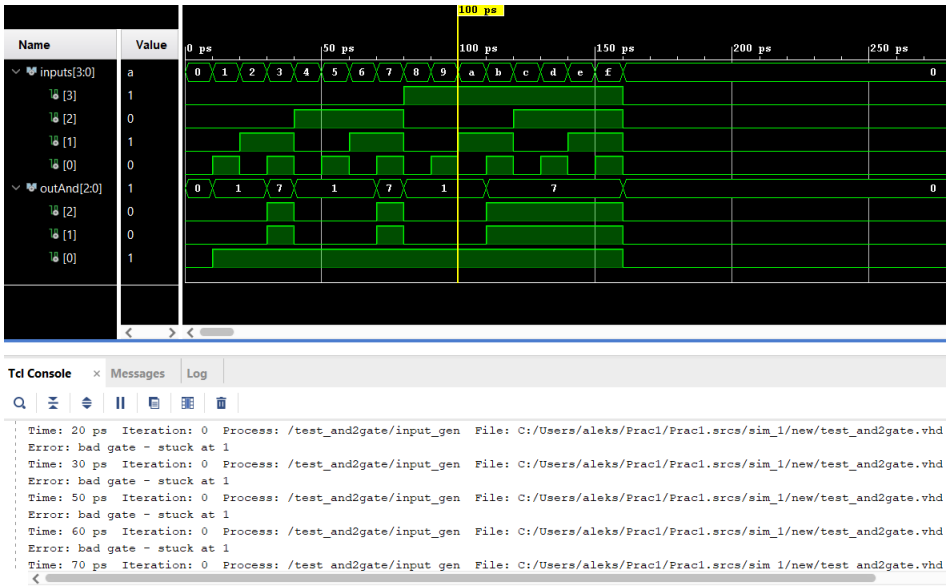

Figure 5: Simulation of two AND gates and one OR gate with an error to test the testbed

As observed, the testbed generates numerous error messages due to these modifications, and the incorrectness of the code is shown in the simulation results.

4 Synthesis/Implementation Results

Here is a summary that reports the consumption of FPGA resources through synthesis.

Summary

Resource	Utilization	Available	Utilization %
LUT	1	63400	0.00
IO	7	210	3.33

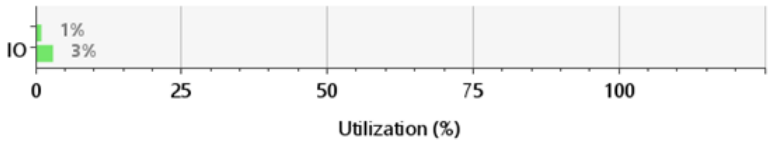

Figure 6: Synthesis report

5 Discussion and Conclusion

Through this prac, I have managed to design and test a design with two AND gates and one OR gate, consisting of four inputs and three outputs. I have successfully created a self-checking testbed that detects errors. Additionally, I have gained knowledge on how to use Vivado and developed a basic understanding of coding within Vivado.