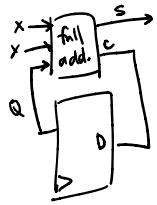
Homework 1 : FSM & SystemVerilog Review

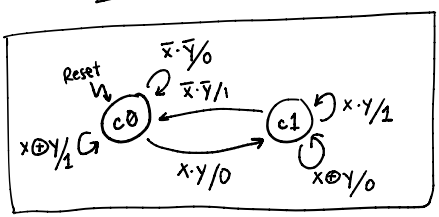
1.



State Encodings

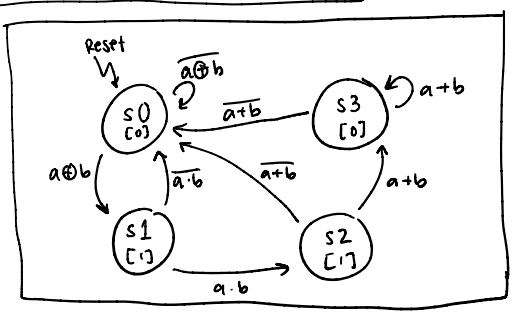
c0 : carry = 0 output: S (sum)

c1 : carry = 1



2. Implemented in SystemVerilog

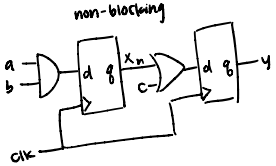
3.



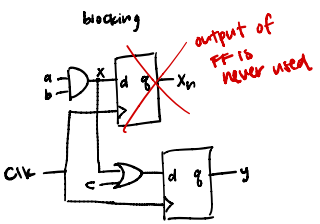
4.

Circuit 1:

non-blocking

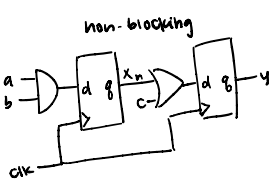


blocking



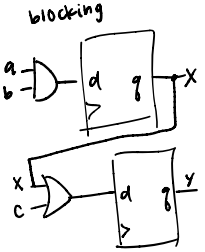
Circuit 2:

non-blocking



(same bc RHSs all get evaluated at the same time before getting assigned to x & y; so, order doesn't matter)

blocking



first clk cycle X has no value, but all other clk cycles X has the value from the previous clock cycle

Total Time Spent:

→ 6-7 hours

→ Moderate (mostly easy, but a bit of difficulty with P4)