BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
II SEMESTER 2009-2010
ES C263 MICROPROCESSOR PROGRAMMING AND INTERFACING
COMPREHENSIVE EXAMINATION (CLOSED BOOK)
PART-A

DURATION:60 MIN **11/05/2010** **MM:50**

ID No:	**NAME:**	**SEC:**

Note: Part-A has to be answered in the question paper itself. You can do rough work at the end of Part-B answer sheet. Each question carries 5 marks.

Q1. What is the physical address generated by the instruction, **MOV [DI-8],BL** ? Assume that the DS register contains 200H and DI contains 30H. Also write the machine code (in hex) for the instruction.

Physical Address:
Machine Code:

Q2. A translation table resides in memory with the starting address of 0800H. How does **XLAT** instruction know where the table is? If register AL contains 04, what is the result of XLAT?

Address	**Memory Data**
00800	40
00801	41
00802	42
00803	43
00804	44

Table location:
Result of XLAT:

Q3. The two instructions **ADD AX,1** and **INC AX,** both increase the value of register AX by 1, but one instruction executes faster than the other. Identify with justification.

Q4. What is the result of MUL CL if AL contains 20H and CL contains 80H? What is the result of IMUL CL if AL and CL contain 20H and 80H respectively?

Result of MUL: **Result of IMUL:**

Q5. A JCXZ instruction is used to skip over the AGAIN loop whenever CX equals 0. If the JCXZ instruction were absent and the AGAIN loop enters with CX equal to 0, how many times would the loop execute?

```
DOLOOP: JCXZ SKIPLOOP
AGAIN: ADD AX,3
       LOOP AGAIN
SKIPLOOP:----
```

No. of times the loop executes:

Q6. Will the following piece of code generate the overflow flag? Justify.

```
MOV AL,70H
MOV BL,60H
ADD AL,BL
INTO
```

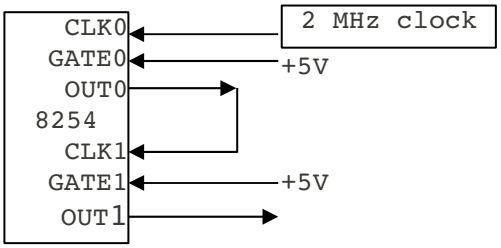
ANS:

Q7. A circuit containing 32KB of RAM is to be interfaced with an 8088-based system, so that the first address of the RAM is 48000H. What is the entire range (memory map) of RAM addresses? Using a single NAND gate decoder and a few inverters, draw the schematic to generate the chip select (active-low) signal for the RAM.

Q8. How many slave devices are required if ICW3 in a master 8259 contains 10010010? What would be the unique cascade code(s) that would be programmed in the ICW3 of slave device(s)?

No. of slave device(s):
ICW(s):

Q9. The figure shows the cascading of two 8254 counters, counter0 and counter1, both working in mode 2. The count value of 50,000 and 160 is loaded in counter0 and counter1 respectively. What is the frequency of the signal at OUT1?



Frequency at OUT1:

Q10. Complete the following timing diagram for the 8237 DMA write operation.