BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI
II SEMESTER 2010-2011
ES C263 MICROPROCESSOR PROGRAMMING AND INTERFACING
TEST II (OPEN BOOK)

TIME: 50 Min. **31/03/11** **MM: 60**

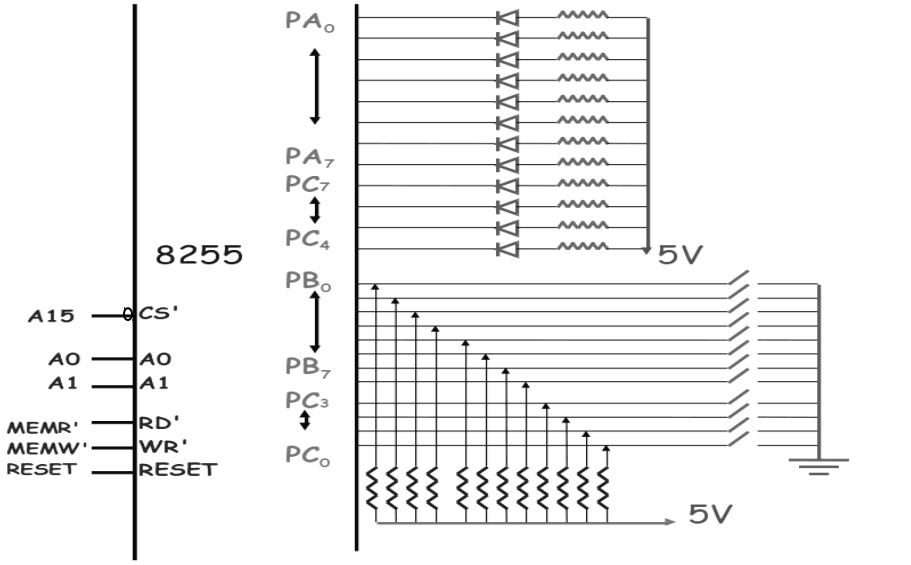
Note: The question paper contains three questions.

Q1. Design a memory system consisting of 32KB of SRAM and 32KB of EPROM, using the specifications given below and interface it with 8088 CPU. **(20)**

Device	**Address Range**	**Size**	**Control signals**
SRAM	00000_H to $07FFF_H$	16K x 4	OE', WE', CS1' and CS2
EPROM	$F8000_H$ to $FFFFF_H$	16K x 8	OE', CS'

Device	**Type**	**Number**
74LS138	3 x 8 decoder	2
7400	Quad 2-I/p NAND gate (IC has four NAND gates, each having two inputs)	1

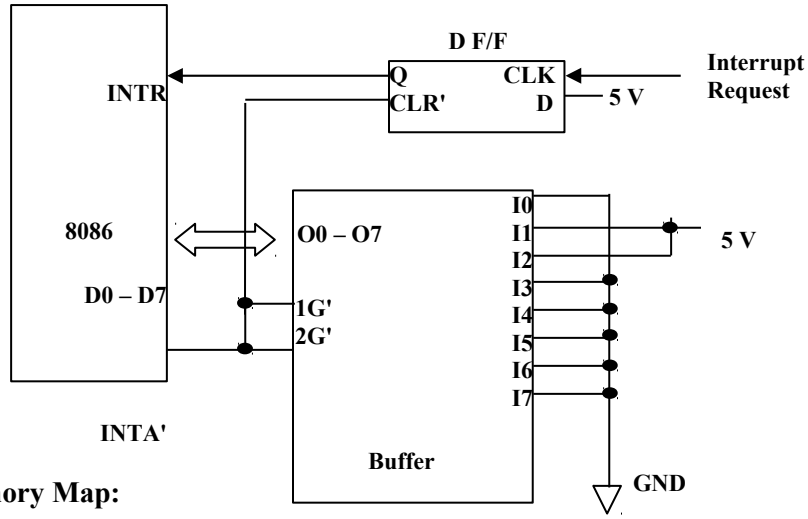
Q2. Using memory mapped I/O interfacing scheme, write an ALP that initializes the 8255, as per the figure given below and reads port PC_L and displays the status at port PA. The base address of 8255 is 8000_H. **(10)**



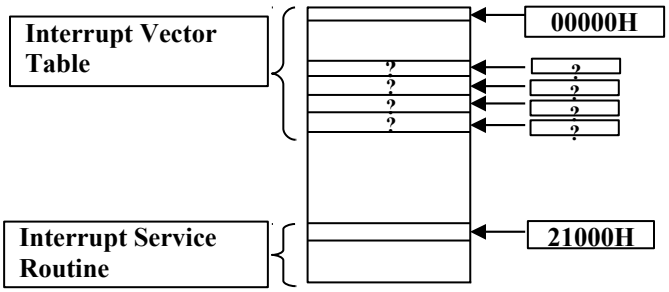
Interface to the I/O Devices

Q3.(a) In the circuit shown below, the interrupting device interrupts the microprocessor each time the interrupt-request input signal transitions from 0 to 1.

(i) What is the value of the interrupt type number sent to the microprocessor? **(2)**
(ii) Fill in the eight entries (shown as ?) in the memory map. **(8)**



Memory Map:



(b) A 256 KB RAM memory is composed of eight 32 KB RAMs. The address range for the devices are as follows: (i) 00000 TO 07FFF (ii) 08000 TO 0FFFF (iii) 10000 TO 17FFF (iv) 18000 TO 1FFFF (v) 20000 TO 27FFF (vi) 28000 TO 2FFFF (vii) 30000 TO 37FFF (viii) 38000 TO 3FFFF

Using a single decoder (74LS138) and one logic gate, show ONLY the decoding logic used to enable the eight devices. **(10)**

(c) An ADC-0808 has its V_{REF} set to +6V. What is the resolution of the input voltage signal applied to it? If V_{IN} = 6V, 0V and 3V, what is the digital output computed by ADC for each of these values? Draw the timing waveform for the ADC-0808. (the timing waveform should include CLK, EOC, SOC, OE, ALE, D0-D7). **(10)**