

# Bo Zhang

**Address:** 1859 Shirley Ln B6, Ann Arbor, MI, 48105, USA  
**Homepage:** <http://www-personal.umich.edu/~gcbo>

**Phone:** (+1) 734-546-5863  
**Email:** gcbo@umich.edu

## OBJECTIVE

---

Seeking a full-time position of RTL Design/Verification starting in March. 2016

## EDUCATION

---

**University of Michigan, Ann Arbor - MI, USA**

Master in **Electrical Engineering - GPA: 3.8/4.0**

Sep. 2014 - Dec. 2015

Relevant courses: Computer Architecture(EECS470) Operating System(EECS482) Microarchitecture(EECS573)  
Embedded System(EECS461) Computer Vision(EECS598) Solid-State Device(EECS423)

**Shanghai Jiao Tong University, - Shanghai, China**

Bachelor in **Electrical Engineering - GPA: 3.76/4.0 , Valedictorian**

2010 - 2014

Relevant courses: Computer Organization Logic Design Programming and Intro. Data Structures  
Semiconductor Devices Design of Microprocessor Based Systems

## WORK EXPERIENCE

---

**National Instruments, Austin, TX**

Summer 2015

**RTL Hardware Engineer Intern**

- Created an interface between Digital Input Module and FPGA Chassis using VHDL
- Developed test benches and scripts verifying interface design on both IP level and SoC level
- Developed plug-in VIs in Labview and tested on real hardware of Digital Input Module

## SKILLS

---

**Languages:** System Verilog, VHDL, C/C++, Matlab, bash script, assembly, Linux command

**Applications:** Synopsys VCS, ModelSim, Xilinx, Simulink, Labview

## COURSE PROJECT

---

**RTL Design of Out-of-order Microprocessor in System Verilog(EECS470)**

Winter 2015

- Implemented a synthesizable 4-way super-scalar out-of-order P6 processor
- Responsible for implementing LSQ for data forwarding, functional units, reservation station, renaming table
- Developed test bench for both IP level and SoC level verification
- Developed a bash-script to auto run all testcases and compare output, which reduced debugging time a lot

**RTL Design of Synthesizable 5-stages in-order Pipelined Processor in Verilog(EECS470)**

Winter 2015

- Modeled and simulated the processor in Synopsys synthesis tool
- Designed and tested data hazard and control hazard detection module

**Multi-threaded Secure Network File Server(EECS482)**

Fall 2015

- Implemented a network file server with socket programming, client-server system, hierarchical file system and security protocols
- Enabled clients using file server to interact with it via encrypted network messages
- Used c++11 thread lock to support safety and concurrency

**Smart Car with an Adaptive Cruise Control of Visual and Haptic Feedback(EECS461)**

Winter 2015

- Created a Simulink module that models a simple car with CAN bus and adaptive cruise control system
- Implemented an automatic steering controller using a PID implementation to keep the vehicle at the center of the road

**Fabrication and Test of IC Devices on an 8 inch Silicon Wafer(EECS423)**

Fall 2014

- Fabricated and tested poly-silicon gate, MOSFET, diode, capacitor, inverter, etc. on a 8 inch wafer
- Hands-on experience with RCA Clean, Photolithography, Dry and Wet Etching, Plasma Ashing, Thermal Treatments, Chemical Vapor Deposition (CVD) and Physical Vapor Deposition (PVD)
- Modeled and simulated the different semiconductor fabrication steps using Silvaco

**Face Detection Based on Adaboost Algorithm in Matlab(EECS598)**

Fall 2014

- Trained a single Adaboost classifier with 50 weak-learners on provided data
- Selected and visualized 50 Haar-like features out of 50,000
- Achieved more than 99% accuracy of face detection for trained data and 95% for untrained data

## LEADERSHIP

---

**Mentor** of CEDO Peer-Mentoring Program in University of Michigan

Fall 2015

- Shared academic and work experience and guided freshman protegee for the whole semester

**Valedictorian** of Shanghai Jiao Tong University Undergraduate Commencement

June 2014

- Delivered a valedictorian speech to over 3000 audience on 2014 Undergraduate Commencement of SJTU