Bo Zhang

Address: 4106 Yosemite Street, Cedar Park, TX, USA 78613 **Phone**: (+1) 734-546-5863
LinkedIn: https://www.linkedin.com/in/bo-zhang-92364586/ **Email**: gcbo@umich.edu

EDUCATION

University of Michigan, Ann Arbor - MI, USA
Master in **Electrical Engineering** - **GPA: 3.8/4.0** Sep. 2014 - Dec. 2015
Relevant courses: Computer Architecture, Operating System, Microachitecture, Embedded System, Computer Vision, Solid-State Device
Shanghai Jiao Tong University, - Shanghai, China
Bachelor in **Electrical Engineering** - **GPA: 3.76/4.0** , **Valedictorian** 2010 - 2014
Relevant courses: Computer Organization, Logic Design, Programming and Intro to Data Structures, Semiconductor Devices, Design of Microprocessor Based Systems

WORK EXPERIENCE

AMD, Austin, TX Nov 2017 - Present
Sr. APU/CPU Power and Performance Engineer
- Project performance for AMD's next generation low power mobile APU, and high-end desktop CPU
- Debug performance issues and conduct competitive analysis
- Perform pre-silicon performance analysis, SOC simulation, and power & performance optimization
- Test, validate and correlate new modeling

Oracle, Austin, TX April 2016 - Oct 2017
CPU Performance Analysis Engineer
- Use Java microbenchmarks to evaluate performance on both SPARC and x86 servers
- Investigate and solve performance issues on SPARC HW and SW
- Write direct assembly test verifying performance features of new SPARC processor
- Verify new SPARC core performance boost on FPGA platform
- Work on improving Java performance on Linux-SPARC platform with SW fix
- Tune default Hotspot JVM flag setting for T8 SPARC

National Instruments, Austin, TX May 2015 - Aug 2015
Hardware Engineer Intern
- Created an interface between Digital Input Module and FPGA Chassis using VHDL
- Developed test benches and scripts verifying interface design on both IP level and SoC level
- Developed plug-in VIs in Labview and tested on real hardware of Digital Input Module

SKILLS

Languages: Java, Scala, System Verilog, VHDL, C/C++, Matlab, bash script, perl, assembly
Applications: Synopsys VCS, ModelSim, Xilinx, Simulink, Labview

COURSE PROJECT

RTL Design of Out-of-order Microprocessor in Verilog Winter 2015
- Implemented a synthesizable 4-way super-scalar out-of-order P6 processor
- Responsible for implementing LSQ for data forwarding, functional units, reservation station, renaming table
- Developed test bench for both IP level and SoC level verification

Multi-threaded Secure Network File Server Fall 2015
- Implemented a network file server with socket programming, client-server system, hierarchical file system and security protocols
- Enabled clients using file server to interact with it via encrypted network messages
- Used c++11 thread lock to support safety and concurrency