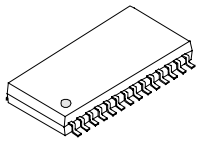
UTC LAG668 LINEAR INTEGRATED CIRCUIT

RADIO AND CASSETTE RECORDER CIRCUIT



SOP-28

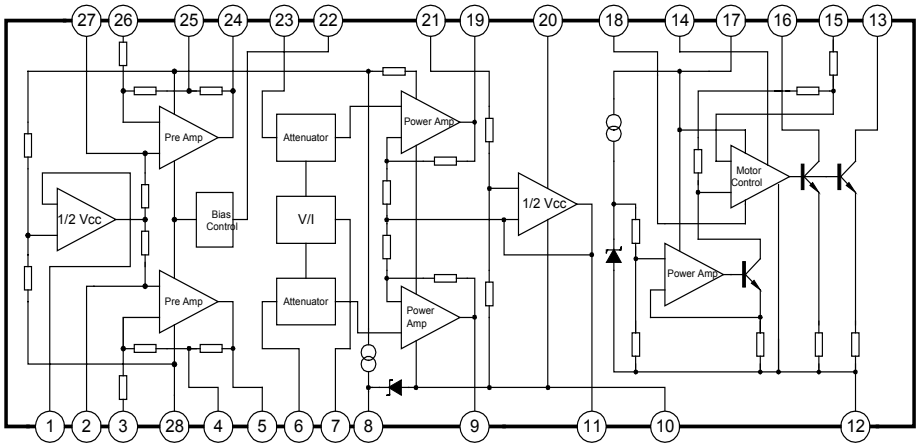
DESCRIPTION

The UTC LAG668 is a monolithic integrated circuit, designed for portable radio cassette.

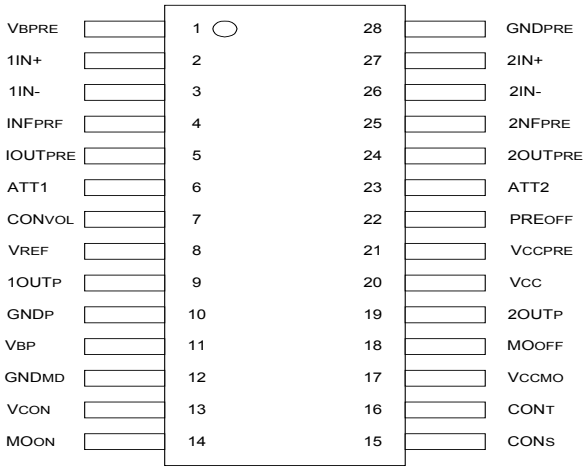
FEATURES

*1-Chip IC for headphone stereo

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NO.	SYMBOL	DESCRIPTION	PIN NO.	SYMBOL	DESCRIPTION
1	VBPRE	Pre Amp Bias Voltage	15	CONS	Speed Control
2	1 IN+	Channel 1 “+” Input	16	CONT	Torqul Control
3	1 IN -	Channel 1 “-” Input	17	VCCMO	Motor Power Control
4	1 NFPRE	Feedback 1	18	MOOFF	Motor Forced Stop
5	1 OUTPRE	Pre Amp Output 1	19	2 OUTP	Power Amp Output 2
6	ATT 1	Attenuator 1	20	VCC	Supply Voltage
7	CONVOL	Volume Control	21	VCCPRE	Supply Voltage
8	VREF	Reference Voltage	22	PREOFF	Pre Amp Off
9	1 OUTP	Power Amp Output 1	23	ATT 2	Attenuator 2
10	GNDP	Power GND	24	2 OUTPRE	Pre Amp Output 2
11	VBP	Power Amp Bias Voltage	25	2 NFPRE	Feedback 2
12	GNDMD	Motor GND	26	2 IN-	Channel 2 “-” Input
13	VCON	Motor Control Voltage	27	2 IN+	Channel 2 “+” Input
14	MOON	Motor Forced Start	28	GNDPRE	Pre GND

ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc	-0.3~+7.5	V
Power Dissipation	Pd	750	mW
Operating Voltage	Vop	2~5	V
Operating Temperature	Topr	-20~+65	°C
Storage Temperature	Tstg	-40~+125	°C

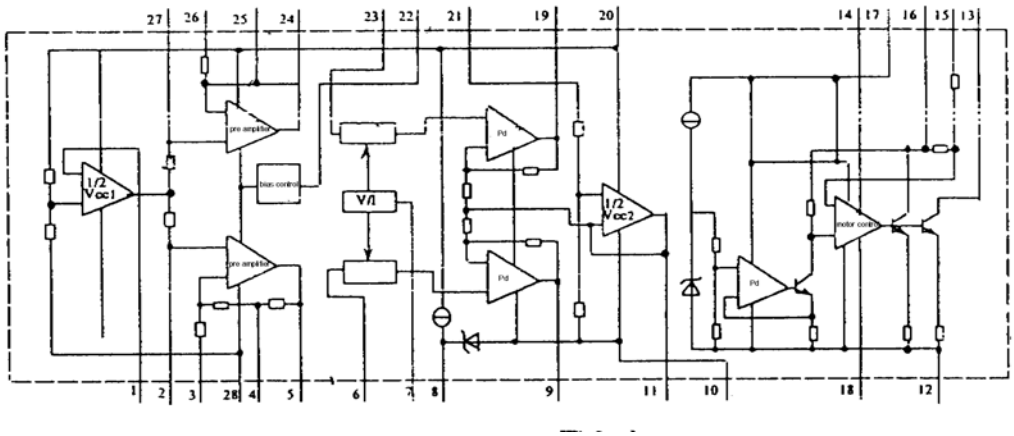
AMPLIFIER ELECTRICAL CHARACTERISTICS(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current	Icc	Vin=0V, IM=0mA		18	25	mA
PRE-AMPLIFIER						
Open Loop Gain	Gvo	Vo=-10dBm, RL=∞		72		dB
Close Loop Gain	Gvc	Vo=-10dBm	40	42	44	dB
Maximum Output Voltage	Vom	THD=10%	0.45	0.6		Vrms
Total Harmonic Distortion	THD	Vout=100mVrms		0.05	0.5	%
Output Noise Voltage	Von	Vin=0, Rg=2.2k, BPF(30~20k)		150	300	μVrms
Input Impedance	Zin	Vout=-10dBm	18	22		kΩ
Cross Talk between CH	CT	Rg=2.2k, Vout=-10dBm	30			dB
Output Voltage when Pre-Off	Vooff	Vin=100mVrms			-50	dB
Output Impedance when Pre-Off	Rooff			10		kΩ
Input Impedance when Pre-Off	Rloff			10		kΩ
Attenuator						
Maximum Input Voltage	Vimax		0.2			Vrms
Maximum Attenuation	Vamax	Vcont=Min	66			dB
Attenuation Error	Vaerr	Vcont=Max		0		dB
Input Impedance	Zia		200			kΩ
Control Ternimal Input Impedance	Zicot		100			kΩ
Power Amplifier						
Voltage Gain	GV	Pout=5mW	36	38	40	dB
Channel Voltage Difference	ΔGV	Vcont=Max		0	3	dB
Maximum Output Power I	Pom 1	THD=10%, RL=32Ω	20	28		mW
Maximum Output Power II	Pom 2	THD=10%, RL=16Ω	30			mW
Total Harmonic Distortion	THD	Pout=5mW		0.5	2	%
Cross Talk between CH	CT	Pout=5mW	20	30		dB
Output Noise Voltage	Von	Rg=2.2k, Vcont=Max		1	2	mVrms
Ripple Rejection	RR	Vcc=3V, 100Hz, 100mVp-p	31	37		dB
Pre + Pulse Boost + Power Noise	Vnto	Vin=0V, Rg=2.2k, Vcont=Max*		3	6	mVrms

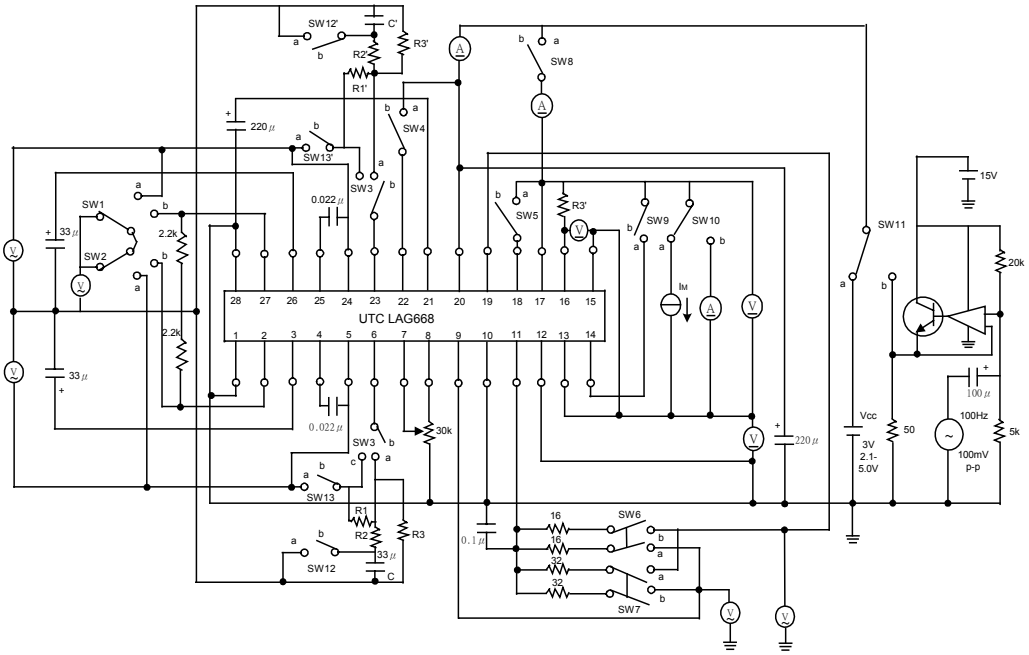
*Vcc=3V, f=1kHz, RL=16Ω, unless otherwise specified.

MOTOR ELECTRICAL CHARACTERISTICS(Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Consumption	IMC			3	5	mA
Starting Current	IMS		500			mA
Reference Voltage	Vref		0.72	0.8	0.87	V
Reference Voltage Change I	Vref 1	Vcc=2.1~5V		0.05		%/V
Reference Voltage Change II	Vref 2	Im=25~250mA		0.01		%/mA
Reference Voltage Change III	Vref 3	Ta=-10~50°C		0.01		%/°C
Current Factor	K		32	38	43	
Current Factor Change I	K 1	Vcc=2.1~5V		0.5		%/V
Current Factor Change II	K 2	Im=25~250mA		0.05		%/mA
Current Factor Change III	K 3	Ta=-10~50°C		0.02		%/°C
Saturation Voltage at Forced ON	VCEsa	IM=200mA, Pin 14=Vcc			0.6	V
Input Impedance at Forced ON Pin	Rion			5.6		KΩ
Leakage Current at Forced OFF	IML				200	μA
Input Impedance at Forced OFF Pin	Ricon			33		KΩ



TEST CIRCUIT 1



NOTE1 : SW12,SW12
R1,R'=33kΩ
R2,R2'=5.1kΩ
R3,R3'=200kΩ
R2,R2,=5.1kΩ
C1,C'=0.1μF

NOTE2 : See figure 1/2 for SW

TEST CIRCUIT 2

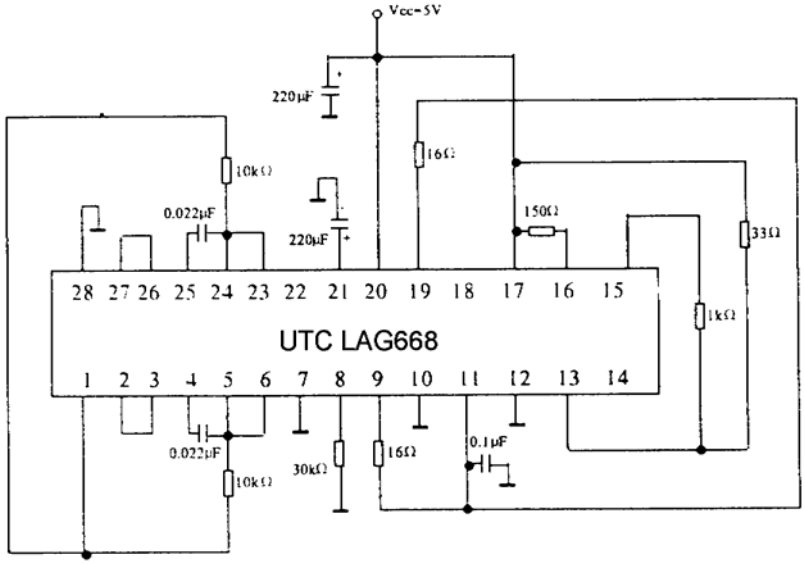


FIGURE 1

Item	Symbol	SW No.													TEST CONDITION
		1	2	3,3'	4	5	6	7	8	9	10	11	12,12'	13,13'	Vcc=3V,f=1kHz,RL=16Ω
AMP															
Supply Current	Icc	c	c	a	b	b	a	b	b	b	a	a	a	a	Im=0mA
Pre AMP															
Open Loop Gain	Gvo	b	b	b	b	b	a	b	b	b	a	a	b	b	Vo=244mV
Maximum Output Voltage	Vom	b	b	b	b	b	a	a	b	b	a	a	b	b	THD=10%
Total Harmonic Distortion	THD	b	b	b	b	b	a	b	b	b	a	a	b	b	Vo=400mV
Output Noise Voltage	Von	c	c	b	b	b	a	b	b	b	a	a	b	b	B.P.F.(30-20kHz)
Cross Talk between CH	CT	b-c	c-b	b	b	b	a	b	b	b	a	a	b	b	Vo=244mV
Output Voltage when Pre-Off	Vooff	b	b	b	a	b	a	b	b	b	a	a	b	b	Vin=100mV
Attenuator															
Maximum Input Voltage	Vimax	a	a	c	a	b	a	b	b	b	a	a	b	a	Vr=Min, THD=10%,
Maximum Attenuation	Vamax	a	a	c	a	b	a	b	b	b	a	a	b	a	
Power AMP															
Voltage Gain	GV	a	a	c	a	b	a	b	b	b	a	a	b	a	Pout=5mV
Channel Voltage Difference	△GV	a	a	c	a	b	a	b	b	b	a	a	b	a	VR=MAX
Maximum Output Power I	Pom 1	a	a	c	a	b	b	a	b	b	a	a	b	a	RL=32Ω,THD=10%
Maximum Output Power II	Pom 2	a	a	c	a	a	a	b	b	b	a	a	b	a	RL=16Ω,THD=10%

FIGURE 2

Item	Symbol	SW No.													TEST CONDITION
		1	2	3,3'	4	5	6	7	8	9	10	11	12,12'	13,13'	
POWER AMP															
Total Harmonic Distortion	THD	a	c	c	a	b	a	b	b	b	a	a	b	a	Pout=5mV
Cross Talk between CH	CT	a-c	c-a	c	a	b	a	b	b	b	a	a	b	a	Pout=5mV
Output Noise Voltage	Von	c	c	c	b	b	a	b	b	b	a	a	b	a	VR=MIN
Ripple Rejection	RR	c	c	b	a	b	a	b	b	b	a	a	b	b	VR=MAX
Pre + Pulse Boost + Power Noise	Vnto	c	c	a	b	b	a	b	b	b	a	a	b	a	VR=MAX, BB ON
Motor															
Current Consump-tio n	IMC	c	c	a	a	b	a	b	a	b	a	a	a	a	Im=0mA
Starting Current	IMS	c	c	a	a	b	a	b	a	b	a	a	a	a	
Reference Voltage	Vref	c	c	a	a	b	a	b	a	b	a	a	a	a	Im=100mA
Reference Voltage Change I	Vref 1	c	c	a	a	b	a	b	a	b	a	a	a	a	Im=100mA,Vcc=2.1-5V
Reference Voltage Change II	Vref 2	c	c	a	a	b	a	b	a	b	a	a	a	a	Vcc=3V,Im=25-250mA
Saturation Voltage at Forced ON	VCEsa	c	c	a	a	b	a	b	a	b	a	a	a	a	Im=200mA
Input Impedance at Forced OFF Pin	Ricon	c	c	a	a	a	a	b	a	b	a	a	a	a	

*Note: a=ON, b=OFF