Notes on Spice Simulations

These notes are intended to help you do the Spice simulation work required for the class project.

Xcede+ Connector Model

The connector to be used in the project is the Amphenol Xcede+ connector. The connector is offered in two versions: a standard back/midplane version and an orthogonal midplane version. For the project, the available sizes are:

- 4x8 Midplane
- 4x8 Orthogonal
- 6x8 Midplane
- 6x12 Midplane
- 6x12 Orthogonal

There are different models for each of these versions These are s-parameter models in Touchstone file format. The Touchstone files, Spice TDR test files, and connector elements modeled for these connectors are:

4x8 Midplane

```
o XCedePlus_4pr_97ohm_1p85mm_With_Extra_GND_2mm_Sig_3mm_GND_Wipe.s32p o xcede 4x8mp test.sp
```

o Models a daughter card plug joined to a midplane socket

4x8 Orthogonal

```
o Orthogonal rev12 Full Final.s24p
```

- o xcede 4x8ortho test.sp
- o Models a daughter card socket to midplane socket pair to daughter card socket connector stack

6x8 Midplane

- o Models a daughter card plug joined to a midplane socket

• 6x12 Midplane

```
o Xcede_plus_6pr_85ohm_1p85mm_20120503_Extra_GND_2mm_Sig_3mm_GND_Wipe.s48p
```

o xcede_6x12ortho_test.sp o Models a daughter card plug joined to a midplane socket

6x12 Orthogonal

```
o XCedeplus_100ohm_2p68_Ortho_2mm_Sig_3mm_GND_Wipe_EF_GHpairs_Only_20144301_IdEM.s32p
```

o xcede 6x8mid.sp

o Models a daughter card plug joined to a midplane socket

The characters after the dot indicate the number of ports. For example, the .s32p file extension means "s-parameters, 32 ports". The comment banner at the head of each model file gives a connection map; for the 4x8 midplane connector, it looks like this:

| Terminated Wafer | Wafer A | Wafer B | Terminated Wafer |
|---|--|--|--|
| GND | GND | GND | GND |
| TERMINATED-Z0 | GND | Port 15 Pin H) | GND |
| TERMINATED-Z0 | Port 31(Pin H) | Port 13(Pin G) | TERMINATED-Z0 |
| GND | Port 29(Pin G) | GND | TERMINATED-Z0 |
| GND | GND | GND | GND |
| TERMINATED-Z0 | GND | Port 11(Pin F) | GND |
| TERMINATED-Z0 | Port 27(Pin F) | Port 9 (Pin E) | TERMINATED-Z0 |
| GND | Port 25(Pin E) | GND | TERMINATED-Z0 |
| GND | GND | GND | GND |
| TERMINATED-Z0 | GND | Port 7 Pin D) | GND |
| TERMINATED-Z0 | Port 23(Pin D) | Port 5 (Pin C) | TERMINATED-Z0 |
| GND | Port 21(Pin C) | GND | TERMINATED-Z0 |
| GND | GND | GND | GND |
| TERMINATED-Z0 | GND | Port 3(Pin B) | GND |
| TERMINATED-Z0 | Port 19(Pin B) | Port 1(Pin A) | TERMINATED-Z0 |
| GND | Port 17(Pin A) | GND | TERMINATED-Z0 |
| _ | GND | | |
| BACKPLANE SIDE OF | CONNECTOR, NODE(PI | N LOCATION): | GND |
| Terminated Wafer | CONNECTOR, NODE(PI | Wafer B | Terminated Wafer |
| | CONNECTOR, NODE(PI | | :: |
| Terminated Wafer | CONNECTOR, NODE(PI | Wafer B | Terminated Wafer |
| Terminated Wafer | CONNECTOR, NODE(PI Wafer A GND | Wafer B | Terminated Wafer GND GND |
| Terminated Wafer GND TERMINATED-Z0 | CONNECTOR, NODE(PI Wafer A GND | Wafer B GND Port 16 Pin H) | Terminated Wafer GND GND |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) | Wafer B GND Port 16 Pin H) Port 14(Pin G) | Terminated Wafer GND GND TERMINATED-Z0 |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 GND | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) Port 30(Pin G) | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND | Terminated Wafer GND GND TERMINATED-Z0 TERMINATED-Z0 GND |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 GND GND | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) Port 30(Pin G) GND | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND | Terminated Wafer GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) Port 30(Pin G) GND | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND Port 12(Pin F) Port 10(Pin E) | Terminated Wafer GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) Port 30(Pin G) GND GND GND | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND Port 12(Pin F) Port 10(Pin E) | Terminated Wafer GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 GND | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) Port 30(Pin G) GND GND GND Port 28(Pin F) Port 26(Pin E) | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND Port 12(Pin F) Port 10(Pin E) GND | Terminated Wafer GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND GND GND GND GND | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) GND GND GND GND Port 28(Pin F) Port 26(Pin E) GND GND | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND Port 12(Pin F) Port 10(Pin E) GND | Terminated Wafer GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) GND GND GND GND Port 28(Pin F) Port 26(Pin E) GND GND | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND Port 12(Pin F) Port 10(Pin E) GND GND Port 8 Pin D) Port 6 (Pin C) | Terminated Wafer GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND GND TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) Port 30(Pin G) GND GND Port 28(Pin F) Port 26(Pin E) GND GND Port 26(Pin E) GND Port 24(Pin D) | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND Port 12(Pin F) Port 10(Pin E) GND GND Port 8 Pin D) Port 6 (Pin C) | Terminated Wafer GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 GND TERMINATED-Z0 GND GND |
| Terminated Wafer GND TERMINATED-Z0 TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 GND GND GND GND TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 | CONNECTOR, NODE(PI Wafer A | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND Port 12(Pin F) Port 10(Pin E) GND GND Port 8 Pin D) Port 6 (Pin C) GND | Terminated Wafer GND |
| Terminated Wafer GND TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND GND TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 GND GND GND TERMINATED-Z0 | CONNECTOR, NODE(PI Wafer A | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND Port 12(Pin F) Port 10(Pin E) GND GND Port 8 Pin D) Port 6 (Pin C) GND GND GND Port 4(Pin B) | Terminated Wafer GND |
| Terminated Wafer GND TERMINATED-Z0 GND GND TERMINATED-Z0 TERMINATED-Z0 GND GND GND TERMINATED-Z0 GND TERMINATED-Z0 TERMINATED-Z0 TERMINATED-Z0 GND GND GND GND GND GND GND GN | CONNECTOR, NODE(PI Wafer A GND GND Port 32(Pin H) Port 30(Pin G) GND GND Port 28(Pin F) Port 26(Pin E) GND GND FORD GND GND GND GND GND GND GND GND GND GN | Wafer B GND Port 16 Pin H) Port 14(Pin G) GND GND Port 12(Pin F) Port 10(Pin E) GND GND Port 8 Pin D) Port 6 (Pin C) GND GND GND GND GND GND GND GN | Terminated Wafer GND |

To interpret this, note that Pin A in Wafer A on the daughter card side connects to Pin A in Wafer A on the backplane side, and similarly for the other pins in Wafers A and B. The differential pairs are A/B, C/D, E/F and G/H. But notice that there are also port numbers that are unique: Port 1 through Port 32. The odd numbers are on the daughter card side and the even numbers are on the backplane side: 1 pairs with 2, 3 pairs with 4 and so on. You can ignore the "Terminated Wafers". These simply indicate that when the model was extracted, the pins adjacent to pin ports 1–32 were terminated in the connector's reference impedance, rather than left floating. This is a more accurate representation of the connector in a real system. The Spice statement that instantiates this connector is:

```
3
           4
                5
                   6
                                   10
                                        11
                                             12
                                                  13
                                                       14
                                                           15
                                                                16
17 18 19 20 21 22 23 24
                                        27
                                             28
                                                  29
                                                                32 MNAME=s_model
                              25
                                                       30
                                                            31
```

The model definition that must accompany this is:

```
.MODEL s_model S TSTONEFILE='./XCedePlus_4pr_97ohm_1p85mm_With_Extra_GND_2mm_Sig_3mm_GND_Wipe.s32p'
```

Figure 1 below shows the port connections for this model. Connector model test bench decks for all the connectors are provided on the class website under each connector's sub-directory. These allow you to put a differential step into one of the connector pairs and observe both the output signal and the crosstalk induced at other connector ports. To change where the differential step is applied, change the port number in the Rp and Rn statements:

Rp inp
$$\frac{1}{3}$$
 50
Rn inn $\frac{1}{3}$ 50

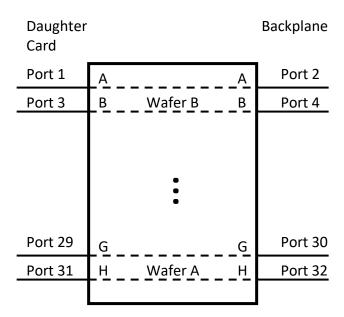


Figure 1

Then comment out the appropriate input terminating resistors. For example:

```
* Daughter Card Side Terminations *
       1 0
*R1
            rterm
*R3
       3 0
            rterm
R5
       5 0
            rterm
       7 0
R7
            rterm
       9 0
R9
            rterm
R11
      11 0
            rterm
R13
      13 0
            rterm
```

```
15 0
R15
           rterm
R17
     17 0
           rterm
R19
     19 0
           rterm
R21
     21 0
           rterm
R23
     23 0
           rterm
R25
     25 0
           rterm
R27
     27 0
           rterm
R29
     29 0
           rterm
R31
     31 0
           rterm
```

To change the Xcede connector pin connections in the channel simulation decks (see below), follow this same procedure in the included file xcede plus.inc.

Channel Simulation Templates

A generic simulation template, reference_channel_2020.sp, is on the class website. You will need to modify this template to customize it to your design. Comment fields identify the places where this should be done.

The structures of the backplane (also coplanar midplane) and orthogonal midplane channels are shown in Figure 2 and Figure 3 below.

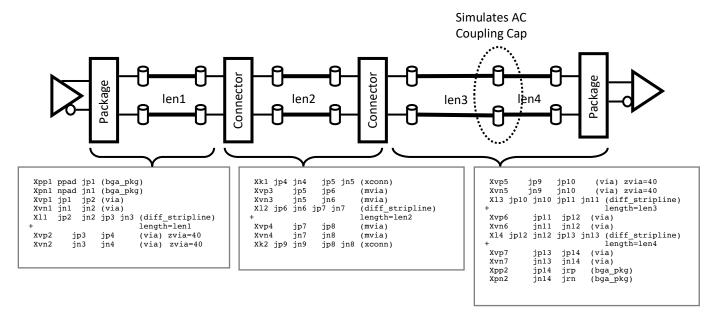


Figure 2 – Backplane Channel

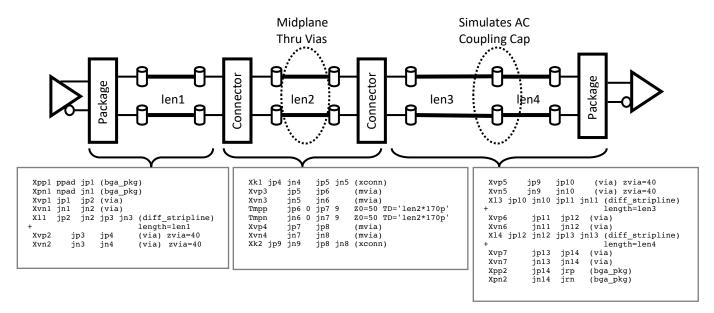


Figure 3 - Orhogonal Midplane Channel

The PRBS7 data eye simulations can be quite long (e.g. 30 minutes), so it is best to first determine the correct equalization using the single pulse simulations before running the data eye simulations with these settings.

All of the user alterable parameters are defined at the top of the .sp files, and their meanings are defined in the associated comment fields. Here is an example, taken from the diff_channel_single_pulse.sp file:

```
*************************
               User Parameter Definitions
   ADJUST THE FOLLOWING PARAMETERS TO SET SIMULATION RUN TIME
    AND TO SET DRIVER PRE-EMPHASIS LEVELS.
    PLOT THE SIGNAL rx diff TO GET THE DIFFERENTIAL RECEIVE SIGNAL.
*********************
*******************
* Transmitter Bit Rate *
* Simulation Run Time *
.PARAM simtime = '100/bps' * USE THIS RUNTIME FOR PULSE RESPONSE
*.PARAM simtime = '512/bps' * USE THIS RUNTIME FOR EYE DIAGRAM
* CTLE Settings *
* Driver Pre-emphais *
.PARAM prel = 0.00 * Driver pre-cursor pre-emphasis
.PARAM post1 = 0.00 * Driver 1st post-cursor pre-emphasis
.PARAM post2 = 0.00 * Driver 2nd post-cursor pre-emphasis
* PCB Line Lengths *
PARAM len1 = 9 * Line segment 1 length, inches
PARAM len2 = 12 * Line segment 2 length, inches
PARAM len3 = 4 * Line segment 3 length, inches
PARAM len4 = 1 * Line segment 4 length, inches
* Eye delay -- In awaves viewer, plot signal rx_diff against signal eye
            then adjust parameter edui to center the data eye.
 .PARAM edui = 0.00
                          * Eye diagram alignment delay.
                          * Units are fraction of 1 bit time.
                          * Negative moves the eye rigth.
                          * Positive moves the eye left.
*************************
*******************
```

You will have to modify the appropriate parameter to reflect your link configuration, lengths and bit rate. Also, the transient simulation control statements are at the top of the file just below the parameter definitions, and you can edit these to implement swept simulations if you wish.