COL 215 : Hardware Assignment 2

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1 Introduction

In this assignment, our objective was to implement a stopwatch, which is driven by the inbuilt clock of the Basys3 Board.

2 Design Decisions

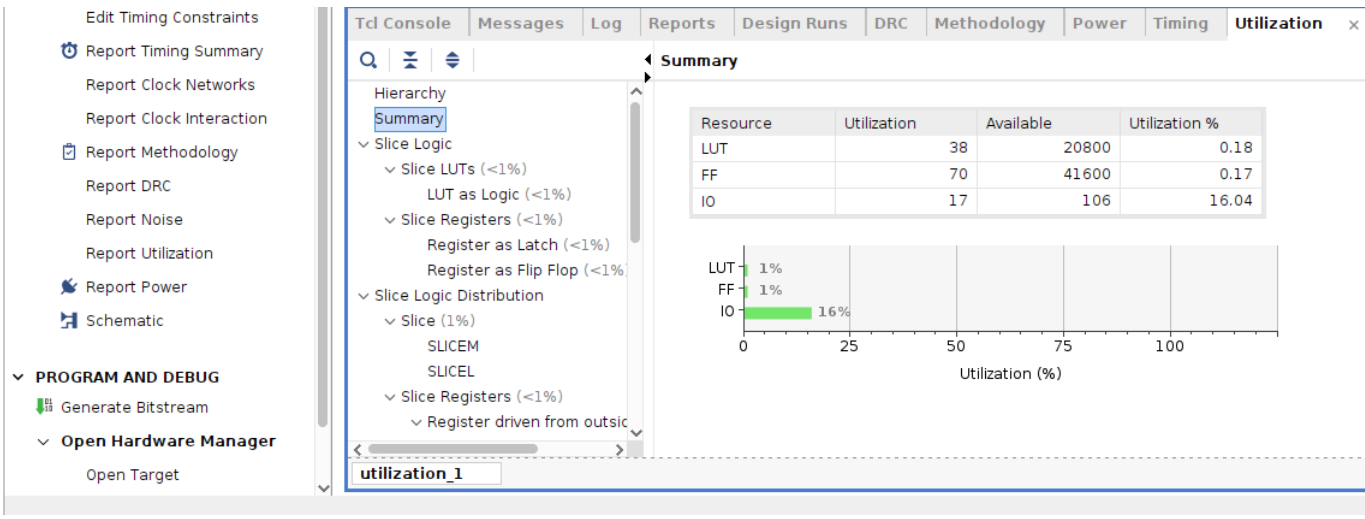
2.1 Stopwatch

First we created an integer a whose value will incremented by 1 whenever there is a $rising_edge$ of the clock and is reset to 0 after it is 10^7 . So the period of a is 1 ms.
Based on the value of a, we define an auxiliary signal x that is assigned 0 when a is 10^7 and 1 otherwise. Now period of x is 1ms and is equal to period of a. We used the rising edge of x to increment the millisecond counter, which resets to 0 after 9.
Similiarly we defined one more auxiliary signal y which is 0 when our millisecond counter is 9 and 0 otherwise. We then used the rising edge of y to drive the 2nd digit of second counter. Similarly, 1st digit of the second counter is driven by defining one more auxiliary signal and the minutes counter is driven by the second counter.

2.2 Switch Functionality

To configure switch functionality, we created two signals *enable_watch* and *reset_watch* which control the clock, *enable_watch* is 1 if and only if the clock is working, *reset_watch* is 1 if and only if clock is reset once after starting. If the clock is started after resetting, *reset_watch* is set to 0. Now all that's left is to control *enable_watch* and *reset_watch* via a process whose sensitivity list contains start,pause,continue and reset.

3 Synthesis Report



1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	39	0	0	20800	0.19
LUT as Logic	39	0	0	20800	0.19
LUT as Memory	0	0	0	9600	0.00
Slice Registers	70	0	0	41600	0.17
Register as Flip Flop	67	0	0	41600	0.16
Register as Latch	3	0	0	41600	<0.01
F7 Muxes	0	0	0	16300	0.00
F8 Muxes	0	0	0	8150	0.00

* Warning! The Final LUT count, after physical optimizations and full impleme

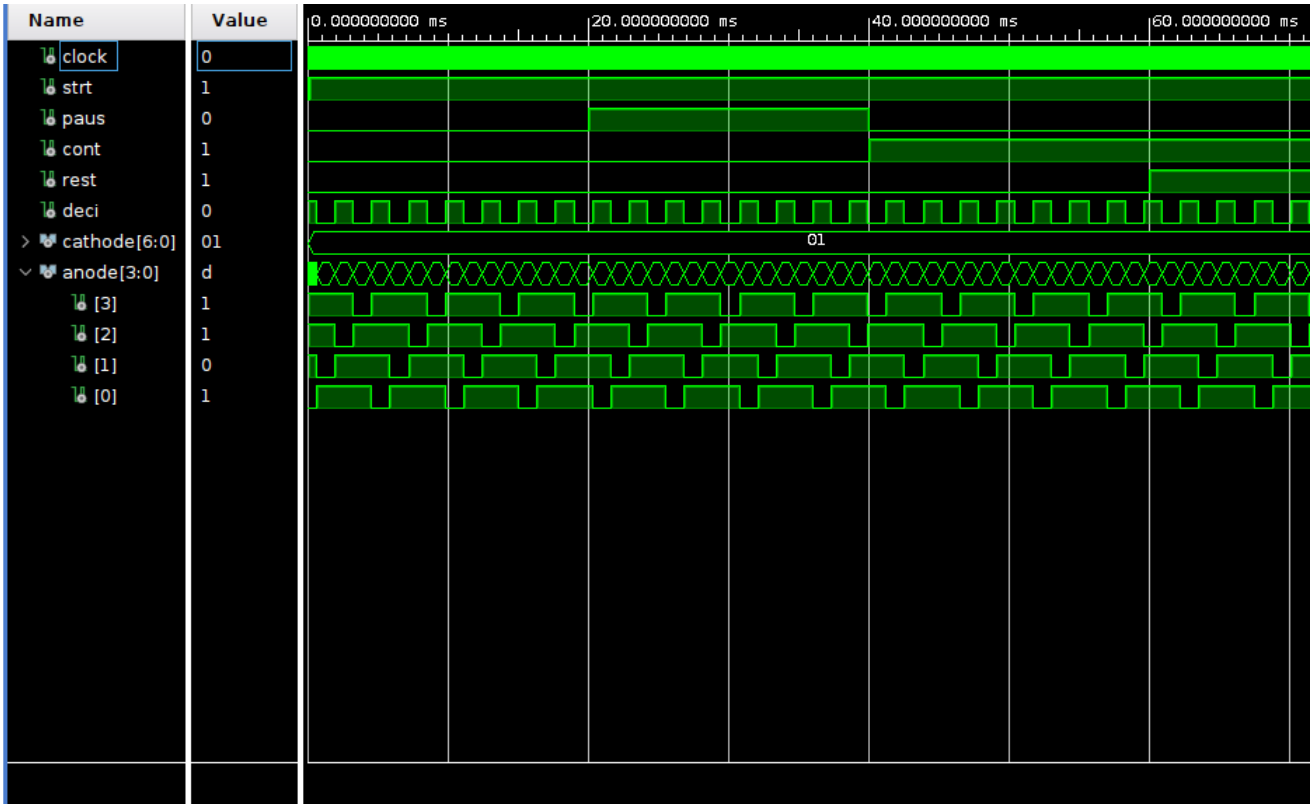
2. Memory

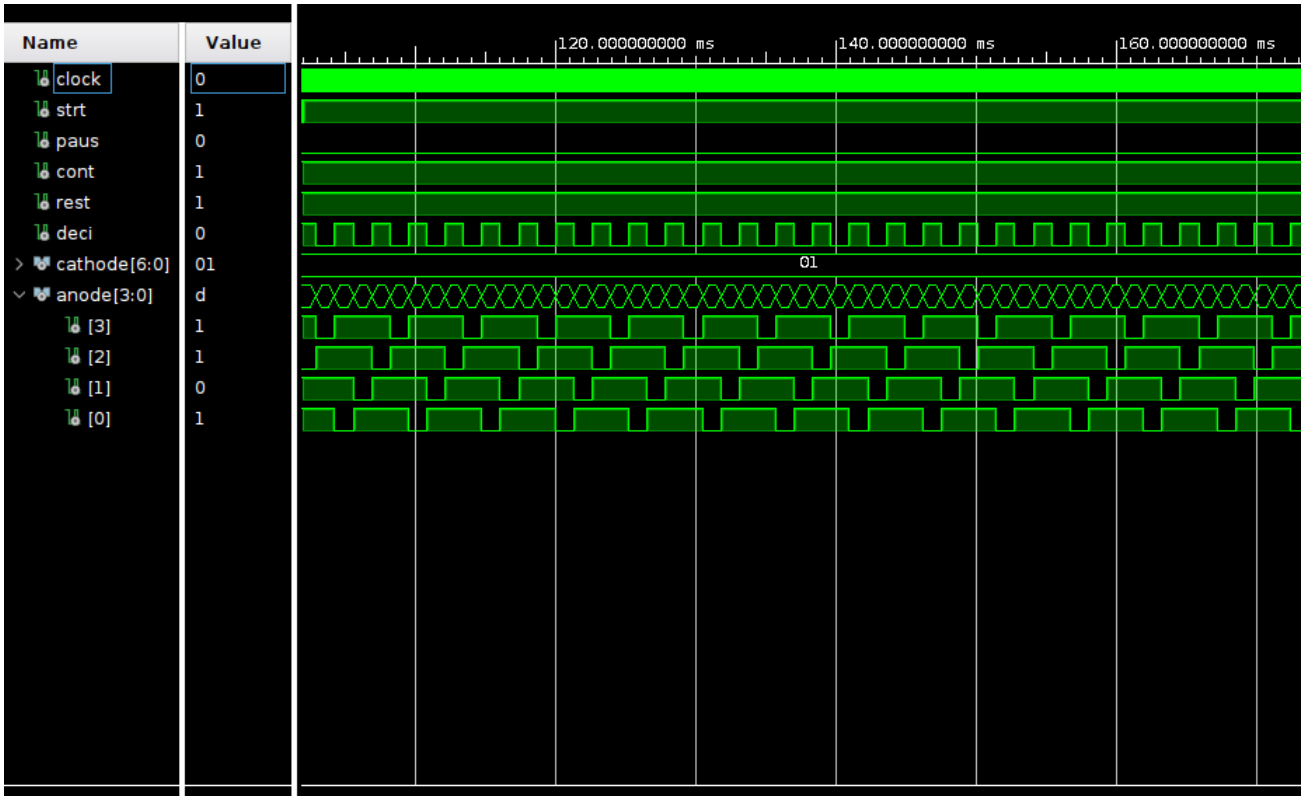
Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	50	0.00
RAMB36/FIFO*	0	0	0	50	0.00
RAMB18	0	0	0	100	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can a
or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can

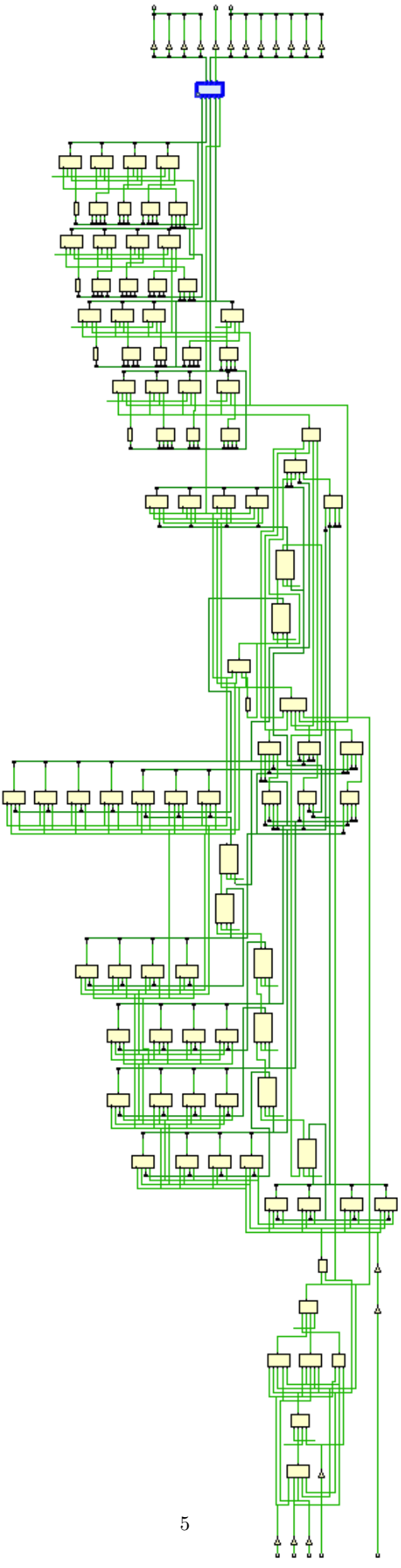
3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	90	0.00


Name
Value
clock
0
strt
1
paus
0
cont
1
rest
1
deci
0
cathode[6:0]
01
anode[3:0]
d
[3]
1
[2]
1
[1]
0
[0]
1
0.000000000 ms
20.000000000 ms
40.000000000 ms
60.000000000 ms
01


Name
Value
clock
0
strt
1
paus
0
cont
1
rest
1
deci
0
cathode[6:0]
01
anode[3:0]
d
[3]
1
[2]
1
[1]
0
[0]
1
120.000000000 ms
140.000000000 ms
160.000000000 ms
01

4 Block Diagram



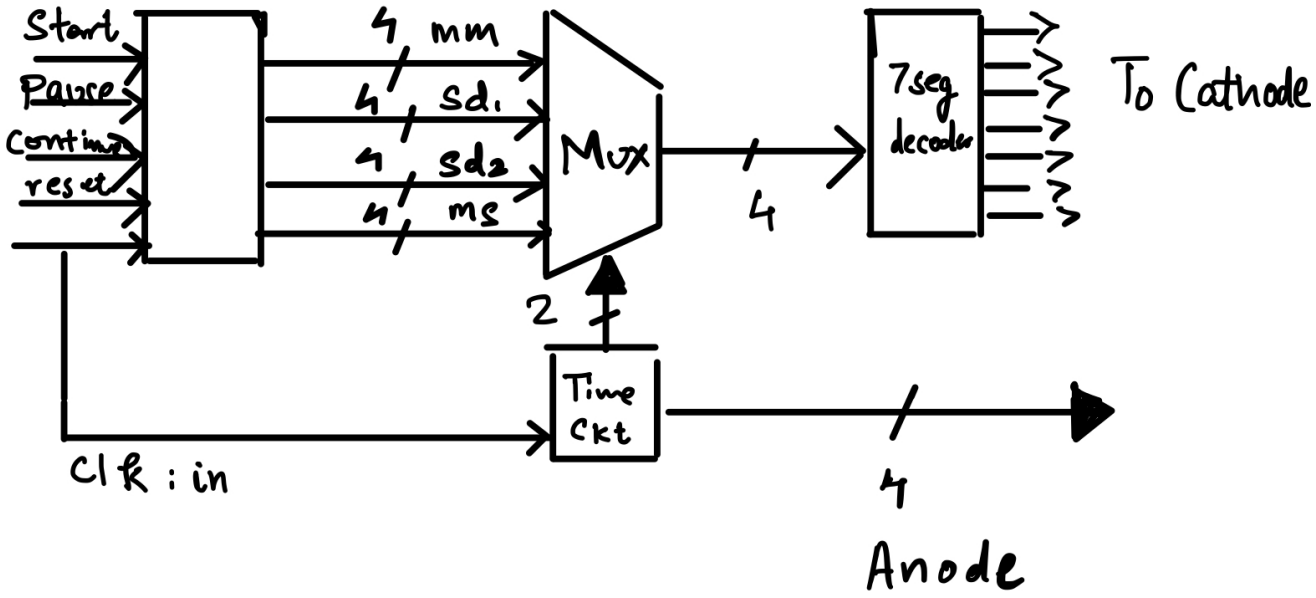


Figure 1: Schematic