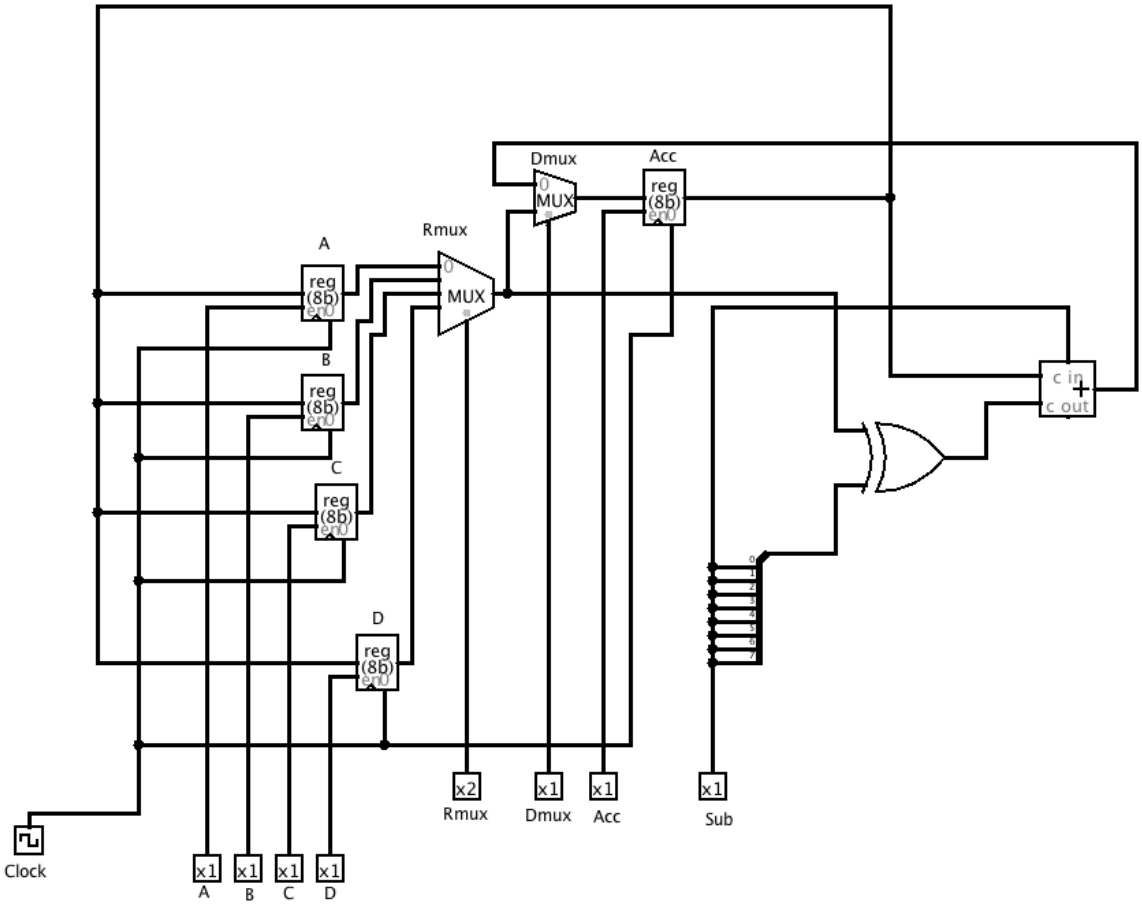
Datapath Circuit for Register Transfer with Adder



Control Code: LaLbLcLd, Rmux, Dmux, Acc, Sub (total control bits = 9 bits)

1) **a) A → Acc**
   b) B+Acc→Acc
   c) Acc-C→Acc
   d) D+Acc→Acc

2) **a) LaLbLcLd = 0000, Rmux = 00, Dmux = 1, Acc = 1, Sub = 0**
   b) LaLbLcLd = 0000, Rmux = 01, Dmux = 0, Acc = 1, Sub = 0
   c) LaLbLcLd = 0000, Rmux = 10, Dmux = 0, Acc = 1, Sub = 1
   d) LaLbLcLd = 0000, Rmux = 11, Dmux = 0, Acc = 1, Sub = 0

3) **A = 0x13 (19)**
   B = 0x5B (91)
   C = 0x3A (58)
   D = 0xF0 (-16)

4) **a) Acc = 0x13 (19)**
   b) Acc = 0x6E (110)
   c) Acc = 0x34 (52)
   d) Acc = 0x24 (36)

5) **No, because none values went outside of the 8-bit two's complement ranges of -128 to 127.**

6) **Acc = 0x24 (36)**

7) **A+B-C+D**

Time	Register Values					Control Code					Action
	A	B	C	D	Acc	LaLbLcLd	Rmux	Dmux	Acc	Sub	
0	0x13	0x5B	0x3A	0xF0	0x00						
1	0x13	0x5B	0x3A	0xF0	0x13	0000	00	1	1	0	A→Acc
2	0x13	0x5B	0x3A	0xF0	0x6E	0000	01	0	1	0	B+Acc→Acc
3	0x13	0x5B	0x3A	0xF0	0x34	0000	10	0	1	1	Acc-C→Acc
4	0x13	0x5b	0x3A	0xF0	0x24	0000	11	0	1	0	D+Acc→Acc