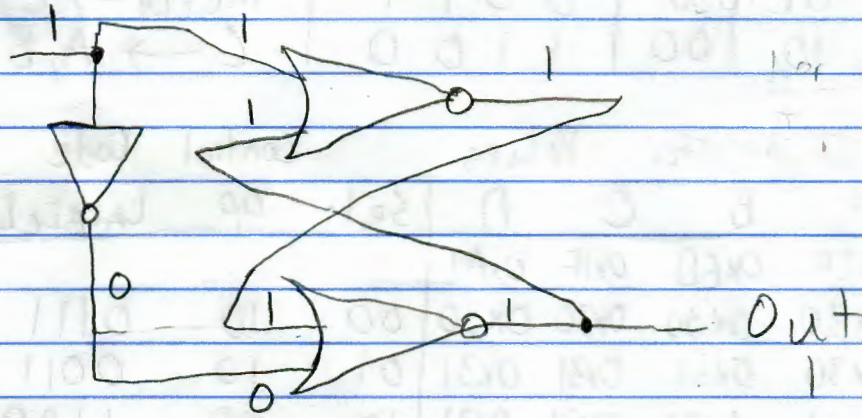
Asn 5

1.

A	Load	Counter$_t$	Counter$_{t+1}$	Out
0xBF	0	0x2E	0x2F	0x2F

2. $DFF_{t+1} = 1$ The state of the DFF component changes at every clock edge.

3.



Nor Gate 1	Nor Gate 2
Input = 1, 1	Input = 1, 0
Output = 1	Output = 1

4. $Register_{t+1} = 0xBB$

5.

Sel	Op	LA	LB	LC	LD	Action
11	11	0	1	1	1	neg(D) → B, C, D

A = 0x2F B = 0x5F C = 0x5F D = 0x5F

6.

Sel	Op	L_A	L_B	L_C	L_D	Action
11	11	0	1	1	1	neg(D) → B, C, D

Register Values

7.

time	A	B	C	D	Action
0	0x2F	0xED	0x1F	0xA1	
1	0x30	0x30	0x30	0x30	inc(A) → B, C, D
2	0x30	0x31	0x31	0x31	inc(B) → C, D
3	0x31	0x31	0x31	0x31	C → A, B

8.

Sel	Op	LA LB LC LD	Action
00	10	0 1 1 1	inc(A) → B, C, D
01	10	0 0 1 1	inc(B) → C, D
10	00	1 1 0 0	C → A, B

Register Values / Control Code

9.

Time	A	B	C	D	Sel	Op	LA LB LC LD	Action
0	0x2F	0xED	0x1F	0xA1				
1	0x30	0x30	0x30	0x30	00	10	0111	inc(A) → B, C, D
2	0x30	0x31	0x31	0x31	01	10	0011	inc(B) → C, D
3	0x31	0x31	0x31	0x31	10	00	1100	C → A, B

10.

Time	A	B	C	D	Dmux	Rmux	Sub	Action
0	0x2F	0xED	0x1F	0xA1				
1	0x4E	0xED	0x1F	0xA1	00	10	0	add(A, C) → A
2	0x4E	0xED	0x32	0xA1	10	01	1	sub(C, B) → C

11.

Time	Acc	A	B	C	D	Rmux	Dmux	Acc	Sub	LA LB LC LD	Action
0	0x00	0x2F	0xED	0x1F	0xA1						
1	0xA1	0x2F	0xED	0x1F	0xA1	11	1	1	0	0000	D → Acc
2	0xB4	0x2F	0xED	0xA1	0xA1	01	0	1	1	0010	sub(Acc, B) → C
3	0x55	0xB4	0xED	0xA1	0xA1	11	0	1	0	1000	add(Acc, D) → A