Asn 8

1) Memory, Out, PC, ACC

2) Memory, Out, PC, ACC, IR, Mar, RT State

Yes, the RTA state includes the ISA state

3) 4 RT state transitions

4) RTA state $2 = t_2$

5) When Hlt is passed through the IR, the instruction code is 1111. This code is then passed through a NAND gate and becomes 0000. Now, the code is passed to an AND gate with the clock, so the clock stops because the AND gates output will be 0 with the Hlt code. With no clock output, the SAM stops.

6) 16 op codes

7)

Instruction	Format
Lda M	000 mmmmm
Add M	001 mmmmm
Sub M	010 mmmmm
Sta M	011 mmmmm
Jmp M	100 mmmmm
Jaz M	101 mmmmm
Out	110 xxxxx
Hlt	111 xxxxx

32 by 8

8)

	Current			Next				
##	PC	RTA	instr	PC	RTA	Acc	Out	hex memory
0				0				0D 1E 2F E0 F0 ... 0
1	0	t_1	Lda	1	t_2	0	–	same
2	1	t_2	Lda	1	t_3	0	–	
3	1	t_3	Lda	1	t_4	04	–	
4	1	t_4	Lda	1	t_1	04	–	
5	1	t_1	Add	2	t_2	04	–	
6	2	t_2	Add	2	t_3	04	–	
7	2	t_3	Add	2	t_4	0B	–	
8	2	t_4	Add	2	t_1	0B	–	
9	2	t_1	Sub	3	t_2	0B	–	
10	3	t_2	Sub	3	t_3	0B	–	
11	3	t_3	Sub	3	t_4	09	–	
12	3	t_4	Sub	3	t_1	09	–	
13	3	t_1	Out	4	t_2	09	–	
14	4	t_2	Out	4	t_3	09	09	
15	4	t_3	Out	4	t_1	09	09	
16	4	t_1	Hlt	5	t_2	09	09	
17	5	t_2	Hlt	5	t_3	09	09	
18	5	t_3	Hlt	xx	xx	09	09	

9) $Inc = t_1$ $Amux = t_3 \wedge (Lda \vee Add \vee Sub \vee Sta)$
$Dmux = t_4 \wedge Lda$ $Acc = t_4 \wedge (Lda \vee Add \vee Sub)$
$Sub = t_4 \wedge Sub$ $Mst = t_4 \wedge Sta$ $PC = t_3 \wedge (Jmp \vee Ja$
$Out = t_3 \wedge Out$ $Hlt = t_3$

10) $PC = t_3 \wedge (Jmp \vee (Jaz \wedge NOR(ACC)))$