c:/Users/Anders/Documents/AIM-spice/DIK-project/Verilog/DIC-project/src/wave.asdb untitled.awc Signal name Value ...r init_in 0 0 .ureset_in 1 .ur clk_in 0 ...r exp_inc_in лг exp_dec_in 0 ₁ nre1_out 1 .rre2_out . r adc_out 0 .urexpose_out 0 . rerase_out Cursor 1 55 ms