```
1   //--------------------------------------------------------------------------
    ----
2   //
3   // Title       : camera_tb
4   // Design      : DIC-project
5   // Author      : Anders
6   // Company     : NTNU
7   //
8   //--------------------------------------------------------------------------
    ----
9   //
10  // File        : c:\Users\Anders\Documents\AIM-spice\DIK-project\Verilog\DIC-project\src
    era_tb.v
11  // Generated   : Wed Nov  8 12:06:36 2017
12  // From        : interface description file
13  // By          : Itf2Vhdl ver. 1.22
14  //
15  //--------------------------------------------------------------------------
    ----
16  //
17  // Description :
18  //
19  //--------------------------------------------------------------------------
    ----
20  `timescale 1 ms / 100 us       //Timescale of 1ms as it is the clock
    frequency
21
22
23  module camera_tb;
24
25      reg init_in, reset_in, clk_in, exp_inc_in, exp_dec_in;
26
27      wire nre1_out, nre2_out, adc_out, expose_out, erase_out;
28
29      parameter size = 2, exp_size = 5;
30
31
32      camera_control uut(         //Map the inputs and outputs of the
    testbench to the module
33          .init(init_in),
34          .reset(reset_in),
35          .clk(clk_in),
36          .exp_inc(exp_inc_in),
37          .exp_dec(exp_dec_in),
38          .nre1(nre1_out),
39          .nre2(nre2_out),
40          .expose(expose_out),
41          .erase(erase_out),
42          .adc(adc_out)
43          );
44
45      always
46          #0.5 clk_in = ~clk_in; // Generate a clock signal at 1kHz
47
48      initial
49          begin
50              clk_in = 1'b0;          //Reset clock and define initial values
51              reset_in = 1'b0;
52              init_in = 1'b0;
53              exp_inc_in = 1'b0;
```

```
54              exp_dec_in = 1'b1;
55              #1; reset_in = 1'b1;    //Reset is active-high
56              #1; reset_in = 1'b0;
57              #10; exp_dec_in = 1'b0;
58              #1; init_in = 1'b1;     //Initialise the camera operation
59              #1; init_in = 1'b0;
60              #1; exp_inc_in = 1'b1;
61              #5; reset_in = 1'b1;
62              #1; reset_in = 1'b0;
63              #5; init_in = 1'b1;
64              #1; init_in = 1'b0;
65              #40;
66              $finish;                //$finish to stop the simulation after
    the 40ms delay
67          end
68
69      initial
70          begin                       //Define the monitor outputs. Writes
    the different states to the console. Using uut.variable enables the
    monitoring of internal signals in the camera controller.
71              $monitor("time = %2d, clk_in =%b, init_in=%b, reset_in=%b,
    exp_inc_in=%b, exp_dec_in=%b, nre1_out=%b, nre2_out=%b, expose_out=%b,
    erase_out=%b, adc_out= %b, exp_time= %d, exp_count = %d, adc_read_cycle =
    %d", $time,clk_in,init_in,reset_in,exp_inc_in,exp_dec_in,nre1_out,nre2_out,
    expose_out,erase_out,adc_out,uut.exp_time, uut.exp_count, uut.
    adc_read_cycle);
72          end
73  endmodule
74
```