c:/Users/Anders/Documents/AIM-spice/DIK-project/Verilog/DIC-project/src/wave.asdb untitled.awc Signal name Value ...r init\_in 0 0 .ureset\_in .ur clk\_in 1 .மexp\_inc\_in лг exp\_dec\_in 0 .rre1\_out 1 .rre2\_out . r adc\_out 0 .urexpose\_out 0 . rerase\_out Cursor 1 67 ms