Arria10 Development Kit Installation Guide for OpenCL

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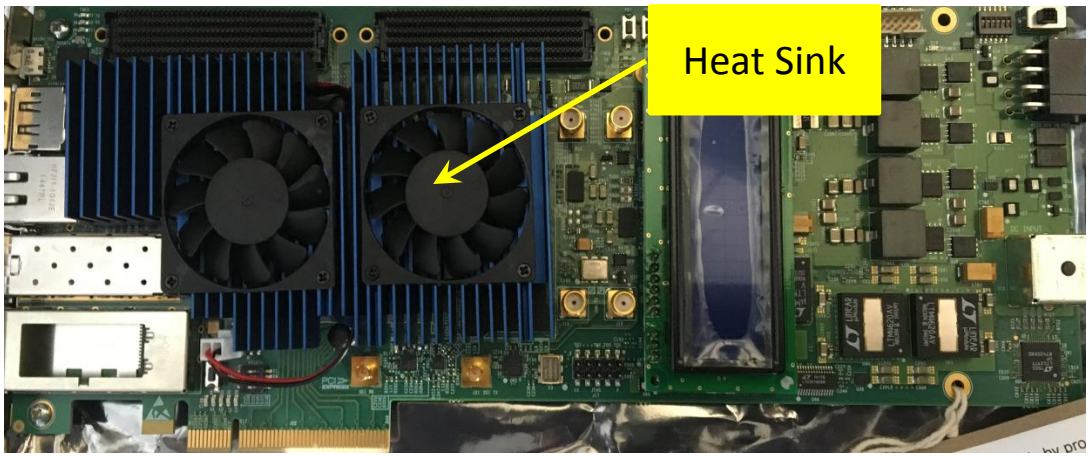
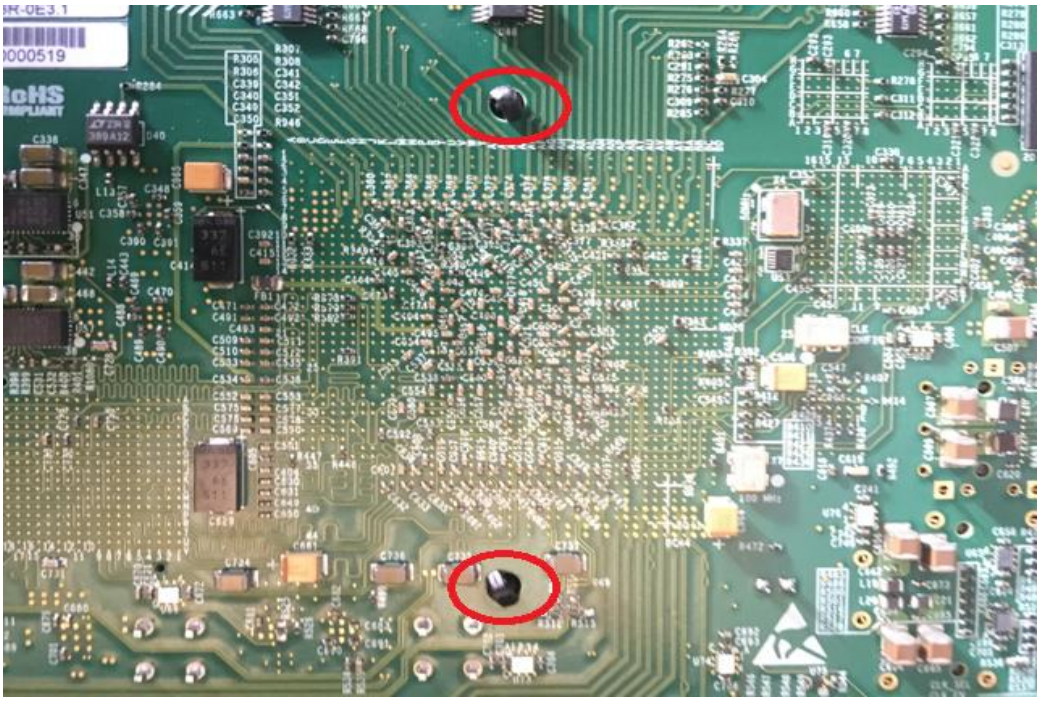
Hardware Setup

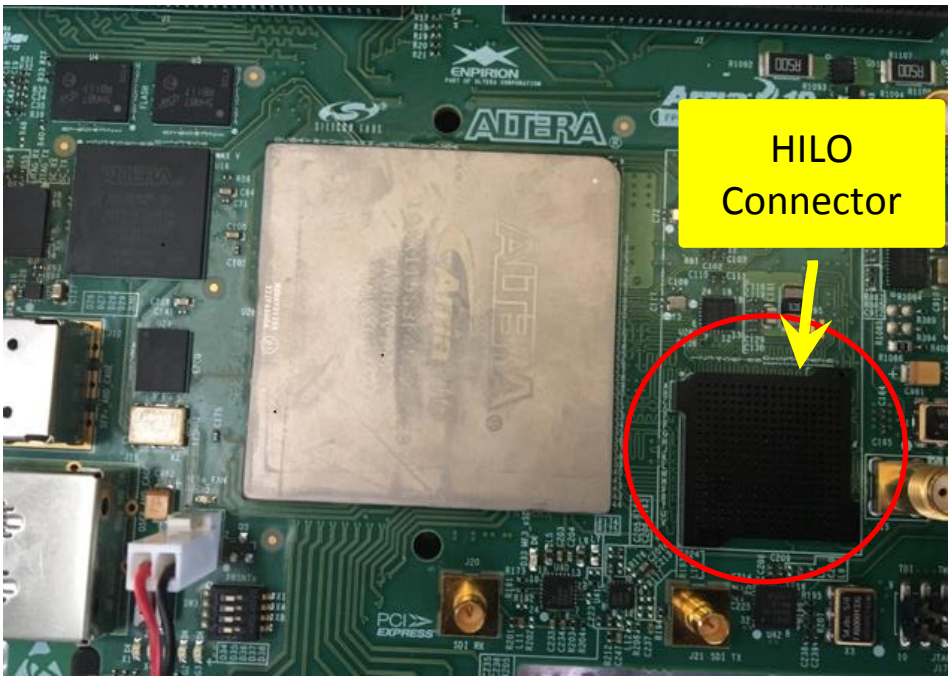
1. This is the picture of the front side of A10 Dev Kit with heat sink.



2. When you receive an Arria10 Dev Kit, first thing you will need to do is to remove the heat sink and plug in the DDR4 memory module in the HILO connector. To remove the heat sink from the board, squeeze and push out the two pins from the back of the board as shown in the picture below.



3. You will see the FPGA and HILO connector on the board as shown below.

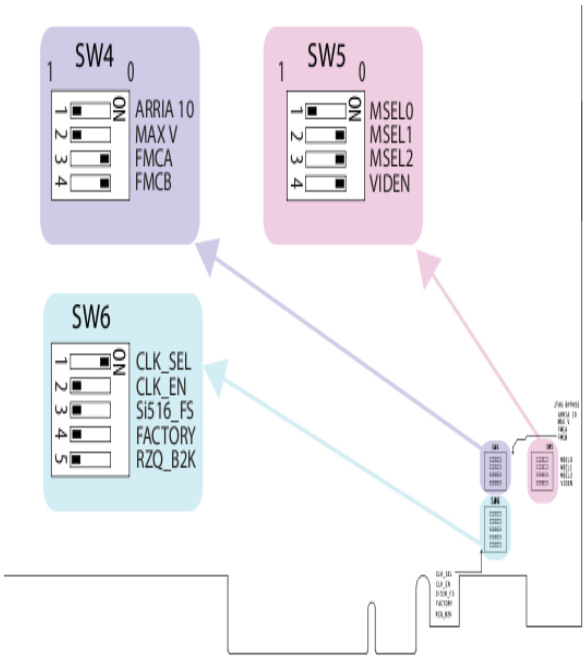


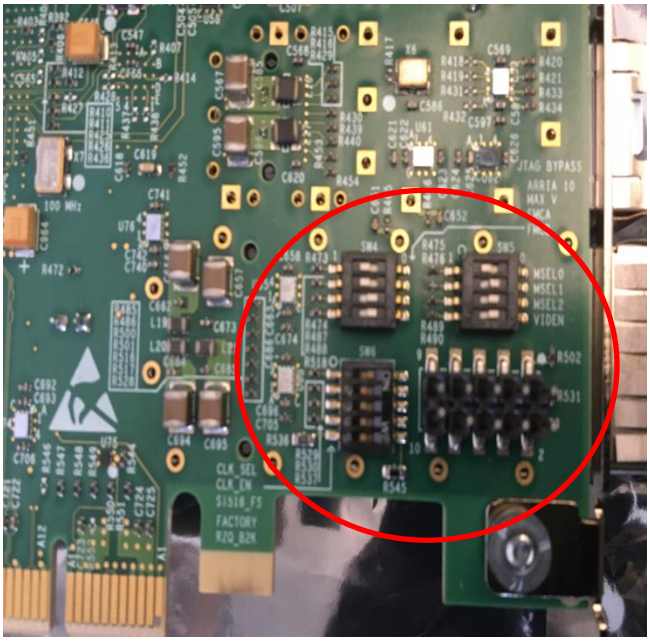
4. This is how the DDR4 memory module you get with the board looks like.

5. Plug the DDR4 module in the HILO connector.

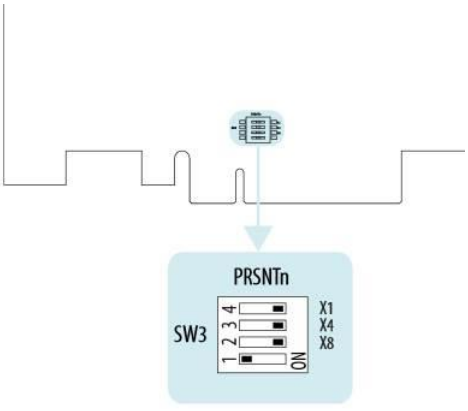
6. After installation of the memory you should put the heatsink back on top of the FPGA. There should be two fans visible.

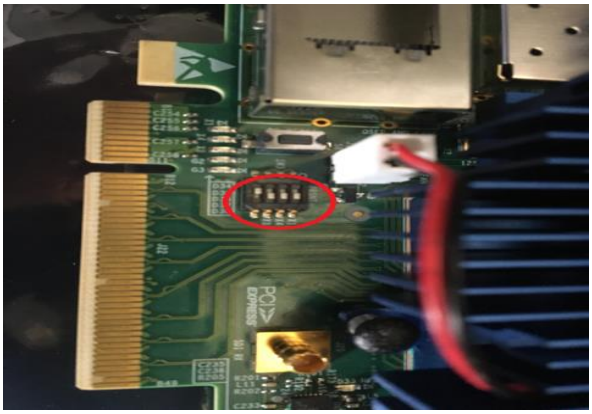
7. Ensure the board DIP switches SW4, SW5 and SW6 are configured as shown below. These switches are located on the back side of the board at the right hand corner.



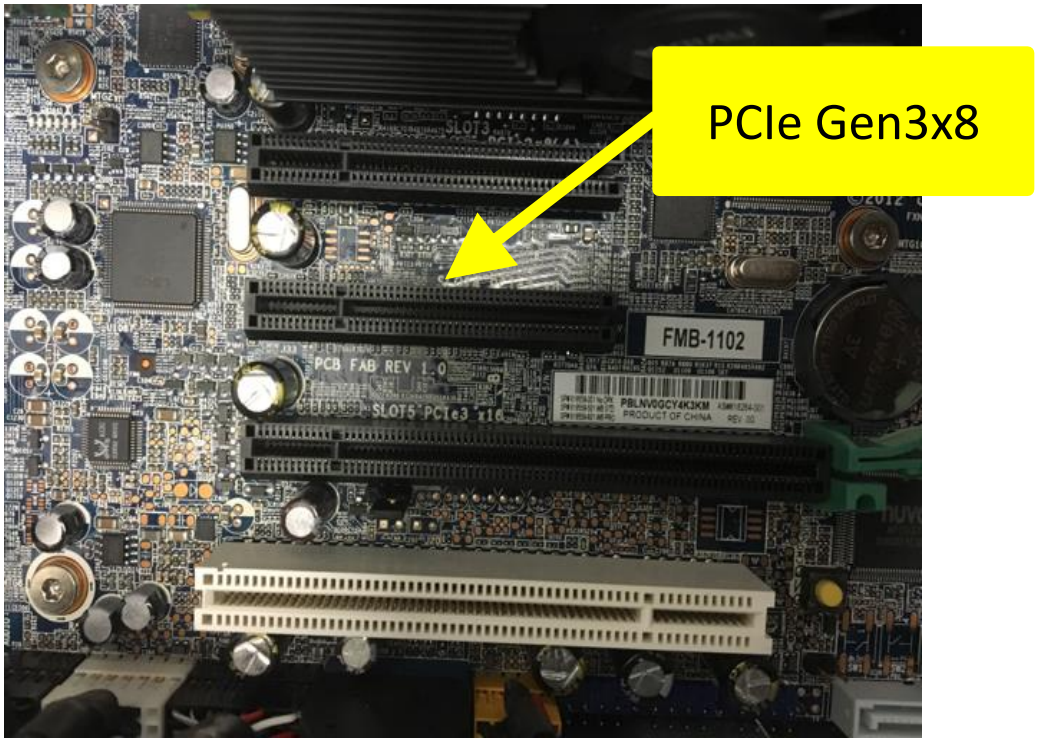


8. Ensure the DIP SW3 is configured as shown below. SW3 is locating on the front side of the board next to the PCIe connector.

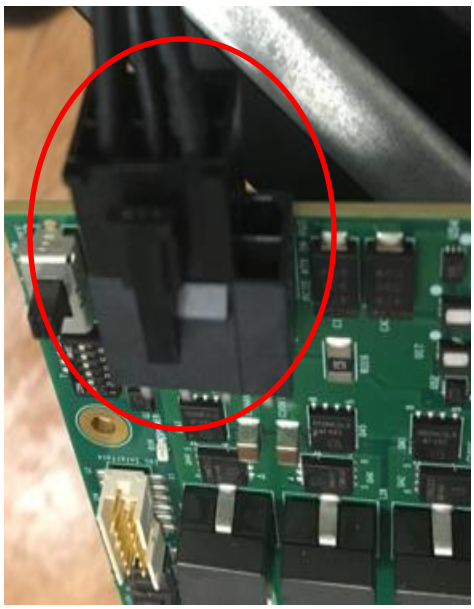




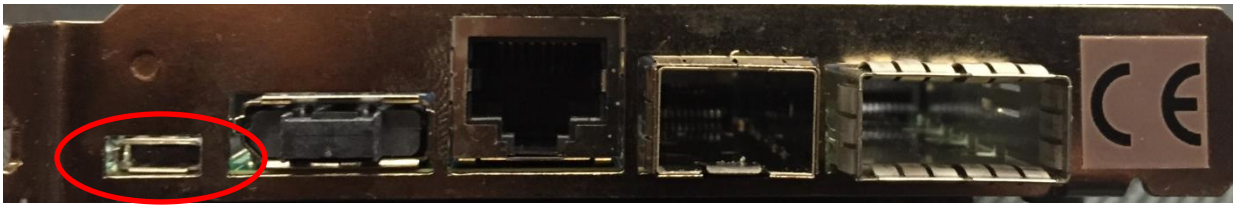
9. Find a **Gen3x8** slot on the host to plug in the board.



10. There is a 6-pin power connector on the host which needs to be plugged on to the board.



11. Plug in the micro USB cable on to the Dev Kit as shown in the picture below.



You have completed the hardware installation of the A10 Dev Kit at this point. The next section will cover Software Installation.

Initialization

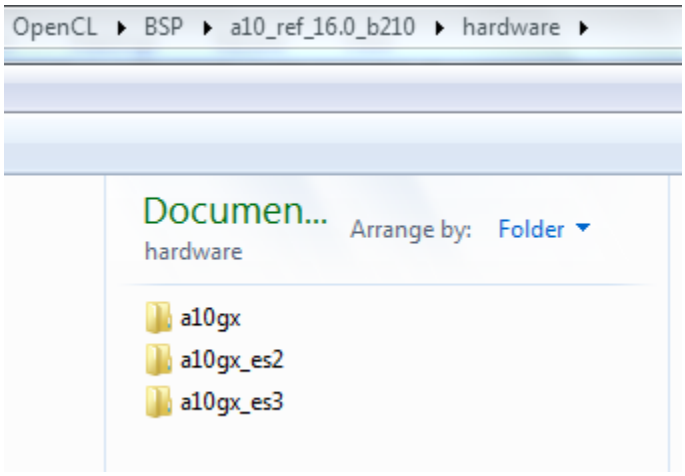
Once the setup is complete, we can move onto the initialization of the A10 Dev Kit.

The A10 Dev Kit does not have an OpenCL image loaded into flash, thus when PC boots up the OS does not find the OpenCL PCIe card and hence Altera OpenCL Compiler (AOCL) cannot find any device.

1. Download A10_Ref_Initialization_for_FAEs.zip. A set of binary files consisting of .sof and .aocx files for each of the A10 reference board variants (a10gx, a10gx_es2, a10gx_es3) are included in this zip. These should be used to initialize and even test the card as shown below.

2. Unzip to folder a10_ref_16.0_b211

3. Under the folder /hardware, locate the folder with your device name (e.g.: for a board with ES3 use a10gx_es3).



4. Use the Quartus Programmer to update the MAXV configuration with the max5_150.pof file for a10gx and a10gx_es3 boards or max5_133.pof for a10gx_es2 board.

    a. Ensure `quartus_pgm -l` shows cable number 1 is the one connected to the A10 Dev Kit. The output should look like the following:

```
Info: Command: quartus_pgm -l
1) USB-BlasterII [2-1.3]
Info: Quartus Prime Programmer was successful. 0 errors, 0
warnings
```

    b. First run jtagconfig to confirm output similar to below:

```
bash-4.1$ jtagconfig

1) USB-BlasterII [2-1.1]
  02E060DD   10AT115N(2E2|3E2|4E2)/..
  020A40DD   5M2210Z/EPM2210
```

c. Run the following command for max_150.pof (analogous for max5_133.pof):

```
quartus_pgm -c 1 -m JTAG -o "p;max5_150.pof@2"
```

5. Program top.sof to the FPGA and warm reboot

   a. Run the following command to program the FPGA:

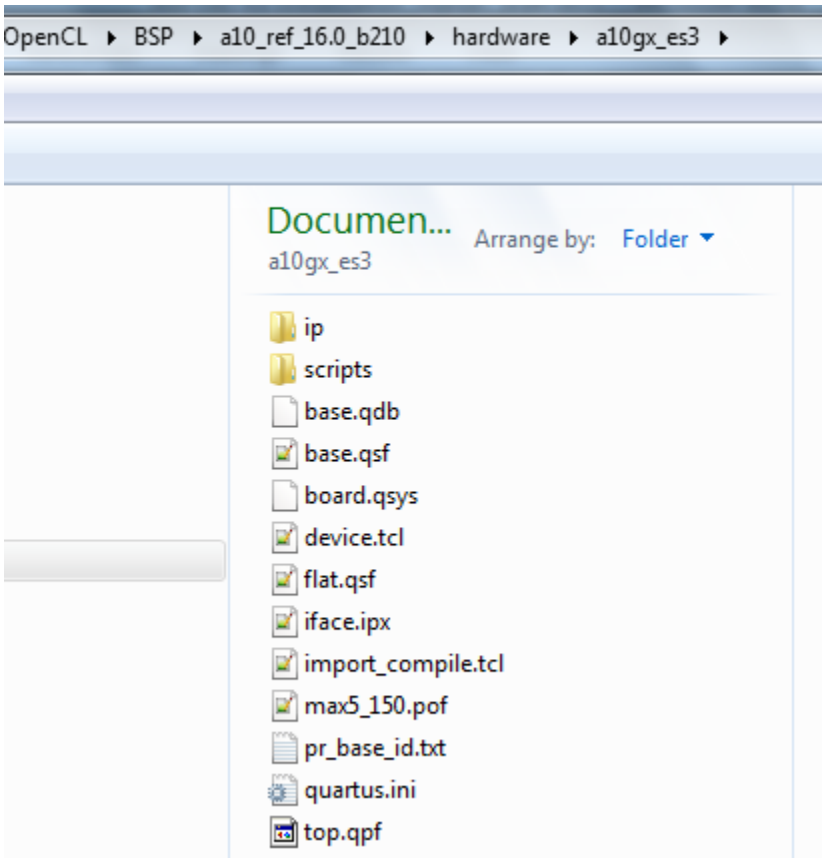
   ```
   quartus_pgm -c 1 -m JTAG -o "p;top.sof"
   ```

   b. Reboot the host without killing power. Use the following command to reboot `/sbin/reboot`. Rebooting after the FPGA image is programmed allows the PC to recognize the card, which will allow the AOCL driver to be loaded.

6. Program the Flash and power cycle/cold reboot

   a. Set AOCL_BOARD_PACKAGE_ROOT to point to the a10_ref BSP folder.

   b. Change directory to the /a10_ref_16.0_211/hardware folder corresponding to your device (e.g. for a card with ES3 use a10gx_es3)



   c. Run the following command to program the flash. This command does not use PCIe, it only requires JTAG.

   ```
   aocl flash acl0 boardtest.aocx
   ```

d. Power cycle the host (power it down, then power it on)

You have completed the A10 Dev Kit initialization at this point. If you run in to any issues, please see the trouble shooting section. In the following section, we will describe how to test the Dev Kit that it is ready for OpenCL

Software Installation & Testing

After completing the initialization, follow the steps below to install OpenCL run-time driver and run diagnostic.

1. Set AOCL_BOARD_PACKAGE_ROOT to point to the a10_ref BSP

2. Install the driver using this command.

```
aocl install
```

   Please note that admin/root rights are required to successfully complete this step. Please ask your system administrator if needed.

   The output should look like following:

```
aocl install: Running install from
/tools/aclboardpkg/altera_a10pciedk/16.0/linux64/libexec
Using kernel source files from  /lib/modules/2.6.32-
358.el6.x86_64/build
Building driver for BSP with name a10_ref
make: Entering directory `/usr/src/kernels/2.6.32-358.el6.x86_64'
  CC [M]  /tmp/opencl_driver_x6GjWS/aclpci_queue.o
  CC [M]  /tmp/opencl_driver_x6GjWS/aclpci.o
  CC [M]  /tmp/opencl_driver_x6GjWS/aclpci_fileio.o
  CC [M]  /tmp/opencl_driver_x6GjWS/aclpci_dma.o
  CC [M]  /tmp/opencl_driver_x6GjWS/aclpci_pr.o
  CC [M]  /tmp/opencl_driver_x6GjWS/aclpci_cmd.o
  LD [M]  /tmp/opencl_driver_x6GjWS/aclpci_a10_ref_drv.o
  Building modules, stage 2.
  MODPOST 1 modules
  CC      /tmp/opencl_driver_x6GjWS/aclpci_a10_ref_drv.mod.o
  LD [M]  /tmp/opencl_driver_x6GjWS/aclpci_a10_ref_drv.ko.unsigned
  NO SIGN [M] /tmp/opencl_driver_x6GjWS/aclpci_a10_ref_drv.ko
make: Leaving directory `/usr/src/kernels/2.6.32-358.el6.x86_64'
```

3. Run the following command to check if the initialization completed successfully.

```
aocl diagnose
```

   The output should look similar to the following:

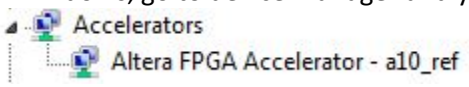
```
aocl diagnose: Running diagnose from
/tools/aclboardpkg/altera_a10pciedk/16.0/linux64/libexec

------------------------- acl0 -------------------------
Vendor: Altera Corporation

Phys Dev Name Status  Information
acla10_ref0   Passed   Arria 10 Reference Platform
                       PCIe dev_id = 2494, bus:slot.func = 04:00.00,
Gen3 x8
                       FPGA temperature = 38.8 degrees C.

DIAGNOSTIC_PASSED
--------------------------------------------------------
```

You should also be able to see Altera device on PCIe port.

a. For Linux, run `/sbin/lspci | grep Altera` and it should output following:

```
-bash-4.1$ lspci | grep Altera
03:00.0 Class 1200: Altera Corporation Device 2494 (rev 01)
```

b. For windows, go to device manager and you should be able to see following:



Troubleshooting

1. Quartus Programmer may error out during aocl flash or aocl program

Your board may fail with the error:

```
Info: Command: quartus_pgm -c 1 flash.cdf
Info (213045): Using programming cable "USB-BlasterII [2-1.1]"
Info (209060): Started Programmer operation at Wed May 20 13:56:27 2015
Error (209025): Can't recognize silicon ID for device 2
Error (209025): Can't recognize silicon ID for device 2
Error (209012): Operation failed
Info (209061): Ended Programmer operation at Wed May 20 13:56:28 2015
```

Solution

Above error means that the MAXV device is not programmed with the correct image. Use the Quartus Programmer to update the MAXV configuration with the max5_150.pof file (for a10gx and a10gx_es3 boards) or max5_133.pof file (for a10gx_es2 board). If the error persists, program the FPGA with top.sof and program the Flash using `aocl flash` command again.

2. Quartus Programmer may fail with one of the following errors while programming either FPGA or Flash

a. `Error (209014): CONF_DONE pin failed to go high in device 1`
b. `Error (209012): Operation failed`

Solution

- Use following command to slower the JTAG clock to 6MHz:

```
jtagconfig --setparam 1 JtagClock 6M
```

- You can get the actual JTAG clock frequency by:

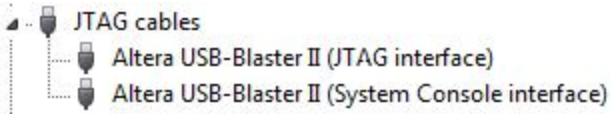
```
jtagconfig --getparam JtagClock
```

3. For Microsoft© Windows© users, USB Blaster driver may not have installed on your host

Solution

Please follow the instructions given on the link below to install the driver:
https://www.altera.com/support/support-resources/download/drivers/usb-blaster/dri-usb-blaster-vista.html

After the installation, you should see following cables in your Windows Device Manager.



4. PCIe read/write speed is slower than expected

Solution

Verify that your A10 Dev Kit is plugged into the PCIe Gen3x8 slot on your host. Please refer to Hardware Set up section.