11. Gaia – Zirkuitu digitalak

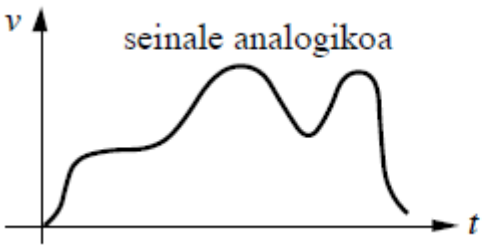
2018-2019 Ikasturtea
Irakaslea: Jose Manuel Gonzalez
Teknologia Elektronikoko Saila
5I28 – Bilboko Ingeniaritza Eskola (II Eraikina)
josemanuel.gonzalezp@ehu.eus

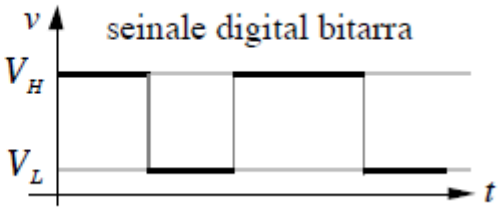
Gaiaren gai-zerrenda

1. Definizioak
2. Integrazio mailak
3. Familia logikoak
4. Bipolarra ate logikoetan
5. NMOS ate logikoetan
6. PMOS ate logikoetan

1. Definizioak

Seinale digitalak

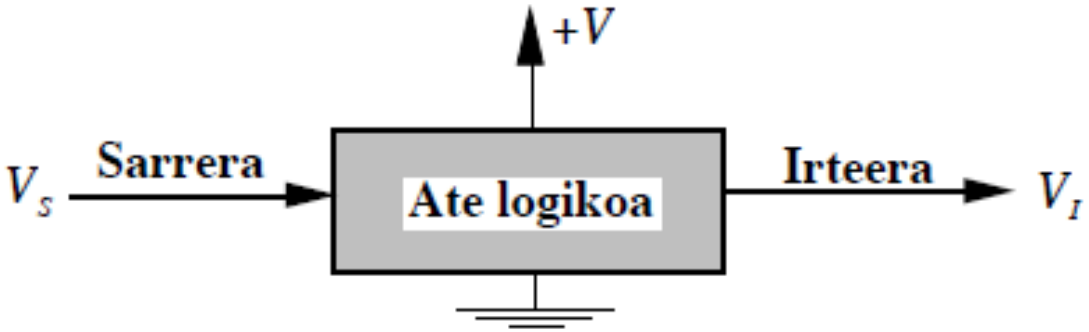




- Balio diskretuak
- Seinale bitarra
- Bi tentsio maila:
  - V_H: Tentsio maila altua – “1” logikoa – Egia
  - V_L: Tentsio maila baxua – “0” logikoa – Faltsua
- Logika positiboa eta negatiboa

Zirkuitu digitalak

- Ate logikoak
  - Irteera tentsioa sarrera funtzio
  - Elikatuta



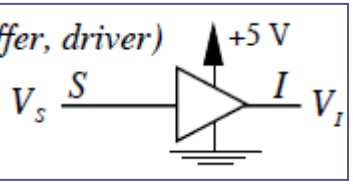
1. DEFINIZIOAK

Ateak

Identitatea

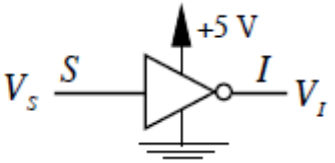
V_S	V_I
L	L
H	H

(Buffer, driver)



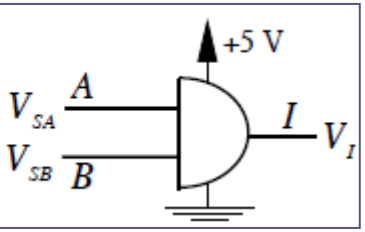
Alderanzkailua
NOT

V_S	V_I
L	H
H	L



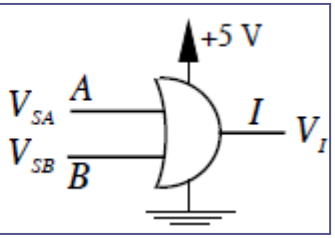
AND

V_{SA}	V_{SB}	V_I
L	L	L
L	H	L
H	L	L
H	H	H



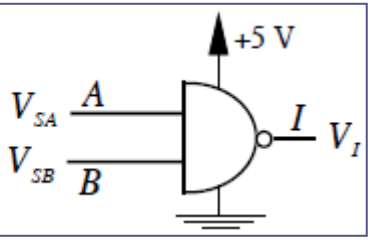
OR

V_{SA}	V_{SB}	V_I
L	L	L
L	H	H
H	L	H
H	H	H



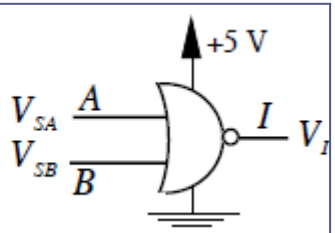
NAND

V_{SA}	V_{SB}	V_I
L	L	H
L	H	H
H	L	H
H	H	L



NOR

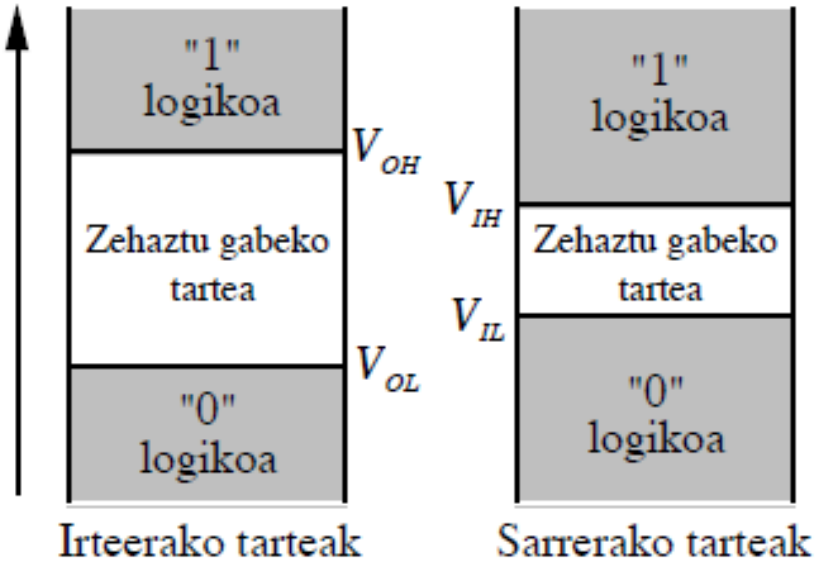
V_{SA}	V_{SB}	V_I
L	L	H
L	H	L
H	L	L
H	H	L



1. Definizioak

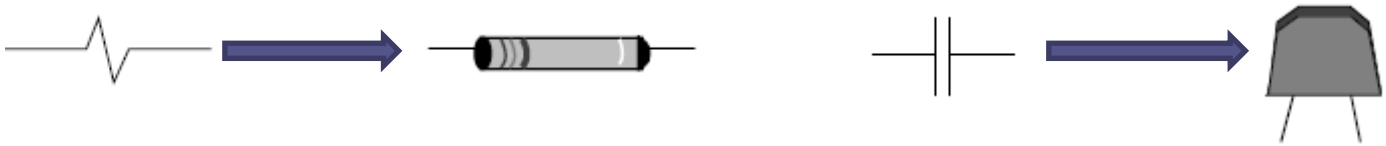
Balio tarteak

- V_{IL}: Sarreran izan daitekeen tentsio baxuaren (L) balio maximoa, ateak 0 logikotzat har dezan
- V_{IH}: Sarreran izan daitekeen tentsio altuaren (H) balio minimoa, ateak 1 logikotzat har dezan
- V_{OL}: Ate baten irteeran ager daitekeen tentsio baxuaren (L) balio maximoa
- V_{OH}: Ate baten irteeran ager daitekeen tentsio altuaren (H) balio minimoa

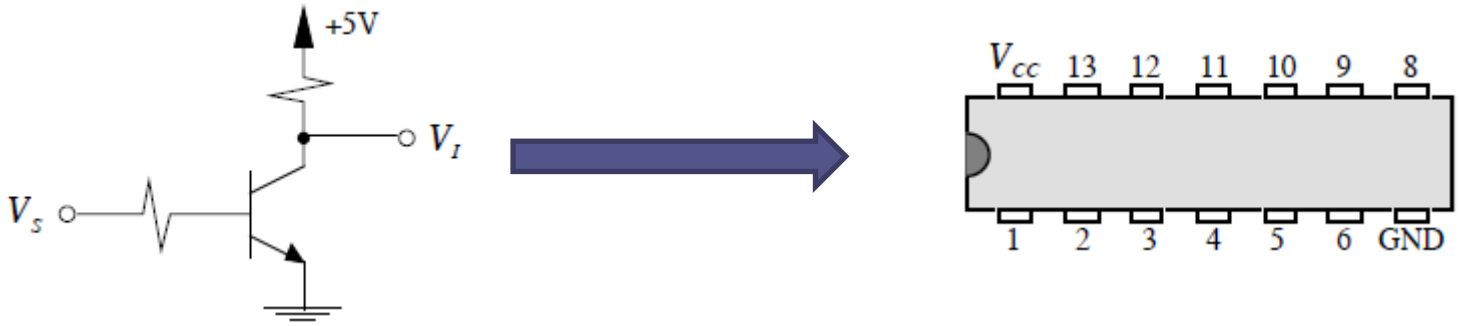


2. Integrazio mailak

- **Osagai diskretuak**



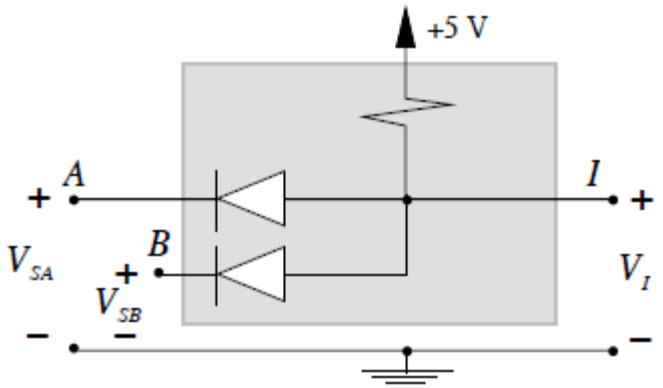
- **Zirkuitu integratuak**



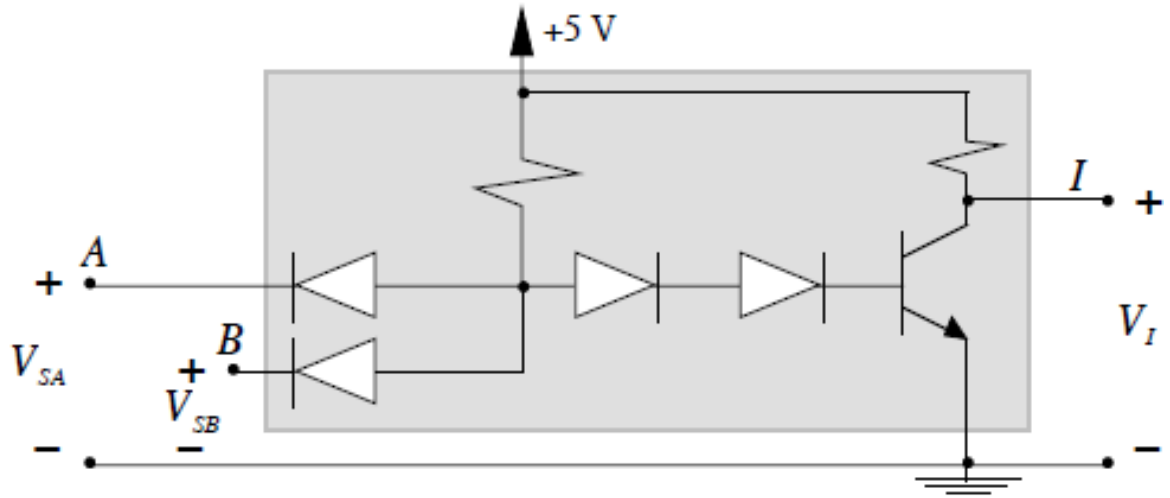
- SSI (integrazio-eskala txikia – Small Scale of Integration)
- MSI (integrazio-eskala ertaina – Medium Scale of Integration)
- LSI (integrazio-eskala handia – Large Scale of Integration)
- VLSI (integrazio-eskala oso handia – Very Large Scale of Integration):

3. Familia logikoak

- **Diodoz osatutako ate logikoak (Diode Logic, DL)**

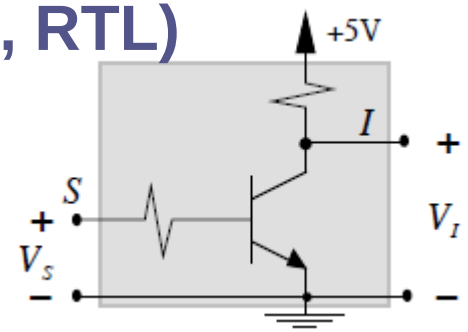


- **Diodo/transistore logika (DTL)**

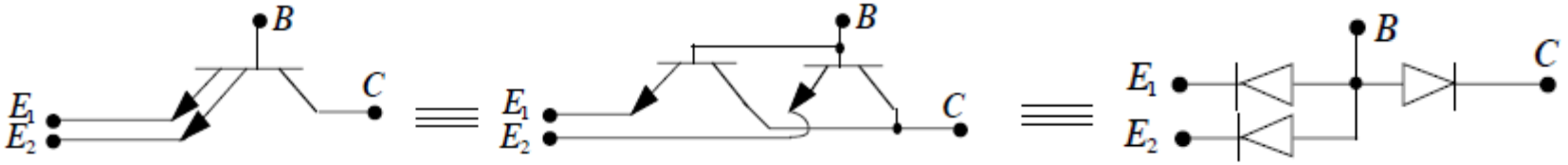


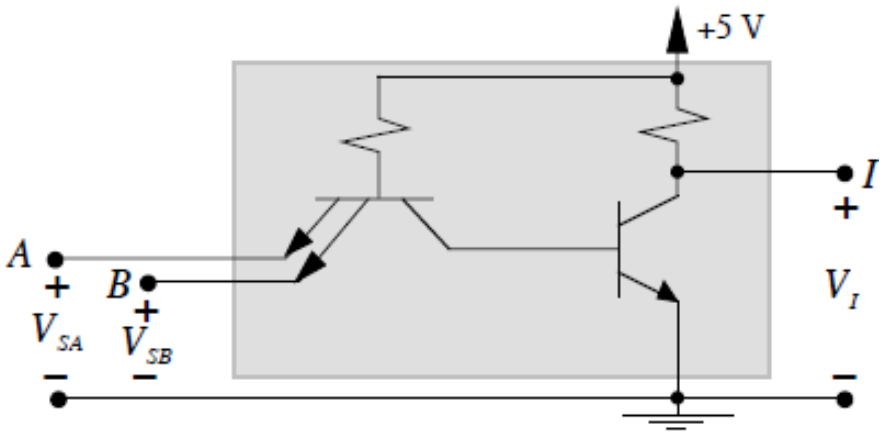
3. FAMILIA LOGIKOAK

- **Erresistentzia/transistore logika (Resistor Transistor Logic, RTL)**



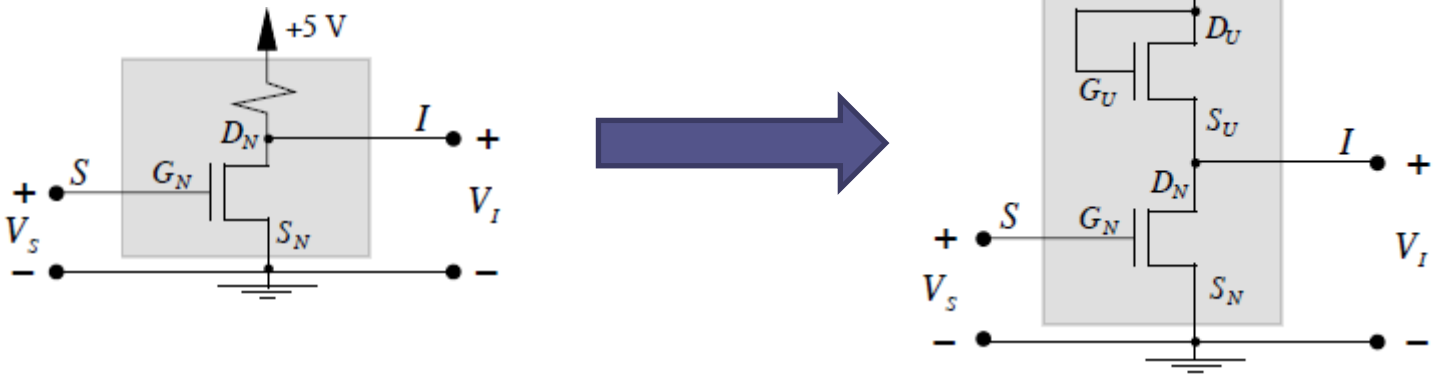
- **Transistore/transistore logika (TTL)**



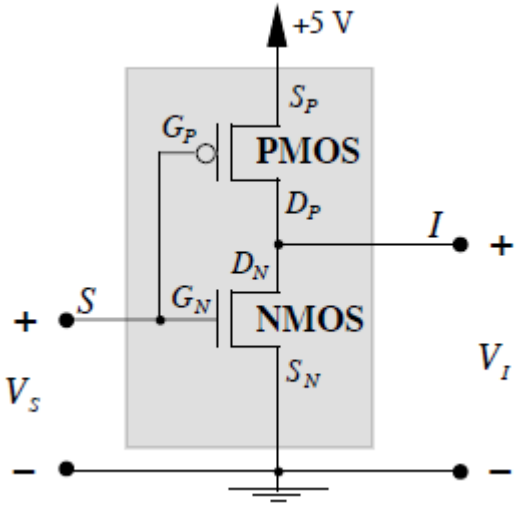


3. FAMILIA LOGIKOAK

- **NMOS logika**

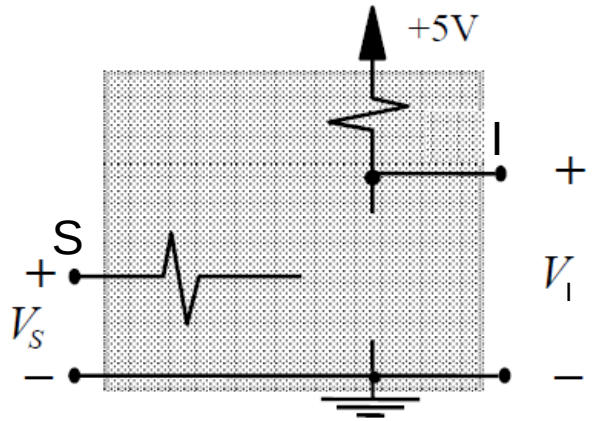


- **CMOS logika**



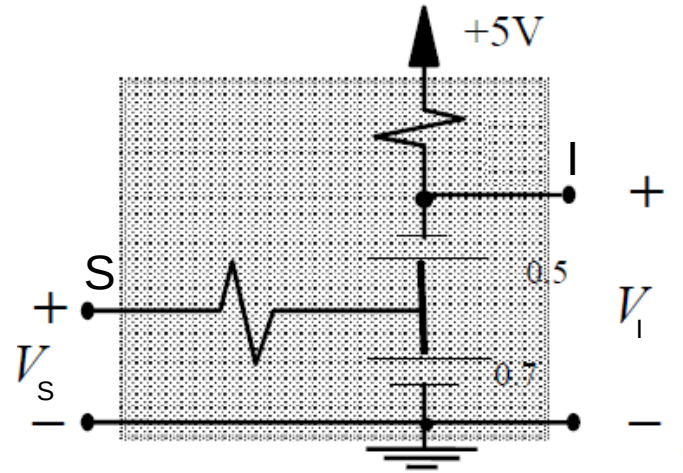
4. BIPOLARRA ATE LOGIKOETAN

- Bi tentsio: H, L
  → Bi funtzionamendu egoera:
  - Etendura eta asetasuna
- **Etendura**



$$V_{BE} \leq 0.7V$$

- **Asetasuna**



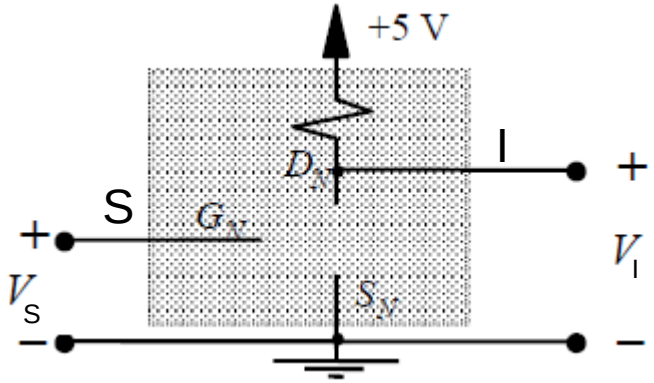
5. NMOS ATE LOGIKOETAN

- Bi tentsio: H, L

  → Bi funtzionamendu egoera: $V_T > 0$

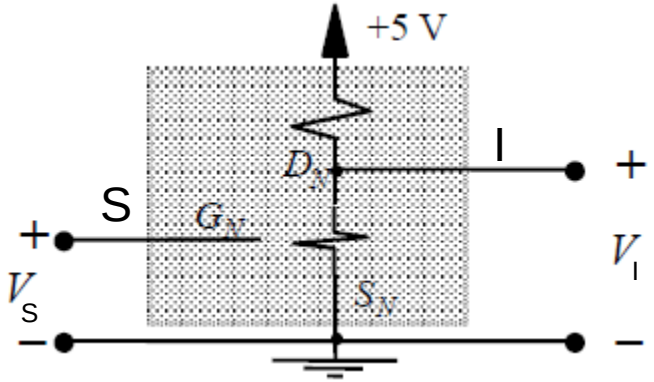
  - Etendura eta gune ohmikoa

- **Etendura**



$V_{GS} \leq V_T$

- **Gune ohmikoa**



$V_{GS} \geq V_T$

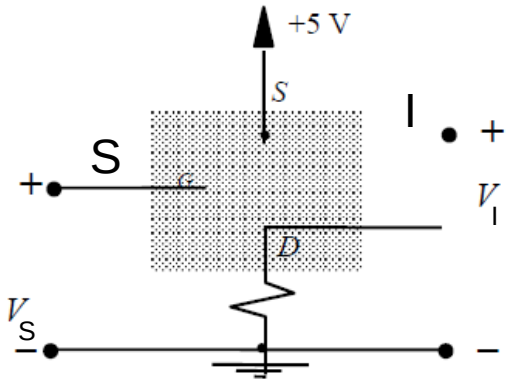
6. PMOS ATE LOGIKOETAN

- Bi tentsio: H, L

  → Bi funtzionamendu egoera: $V_T < 0$

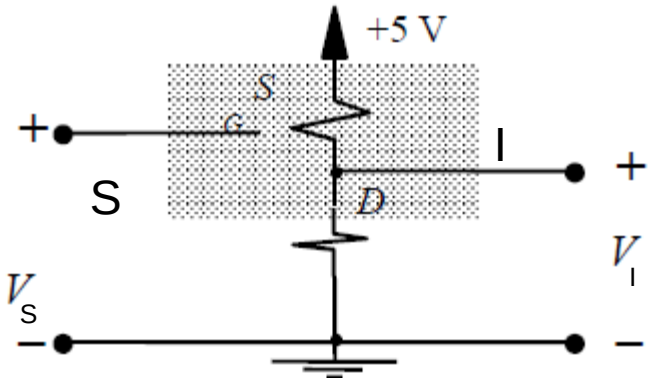
  - Etendura eta gune ohmikoa

- **Etendura**



$V_{GS} \geq V_T$

- **Gune ohmikoa**



$V_{GS} \leq V_T$