

Teknologia Elektronikoa Saila

KONPUTAGAILUEN ARKITEKTURA 80c552 mikro-kontroladorea

Kudeaketa eta Informazio Sistemen Informatikaren Ingenieritzako Graduaren 3. maila

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(alain.sanchez@ehu.eus)

2019-2020, 1. lauhilabetea

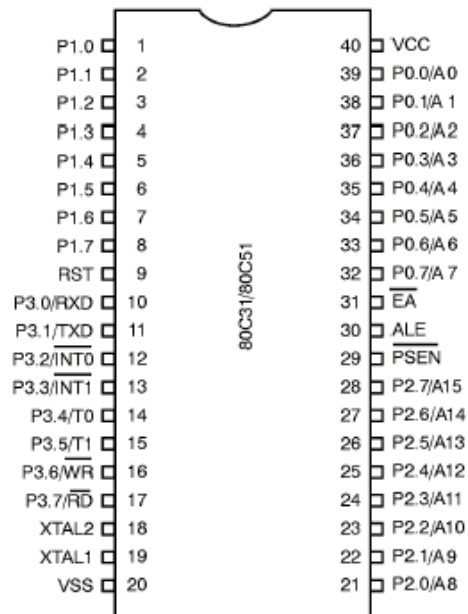
80c552 familia ezagutzea

80c51-arekiko, 80c552-ak dauzkan ezberdintasunak
ulertzea

80c552 mikro-kontroladorea

Zelakoa da 80c552 mikro-kontroladorea?

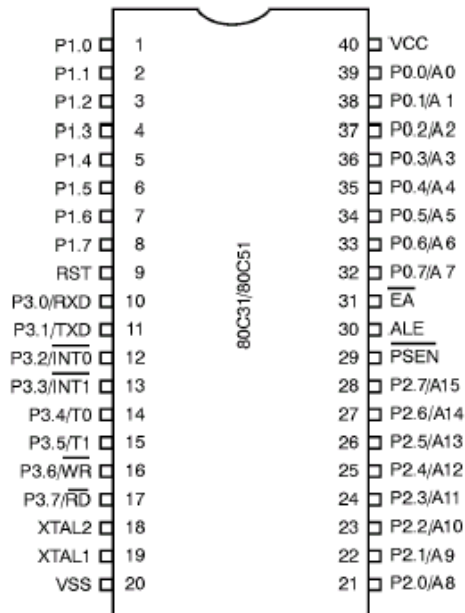
80c51



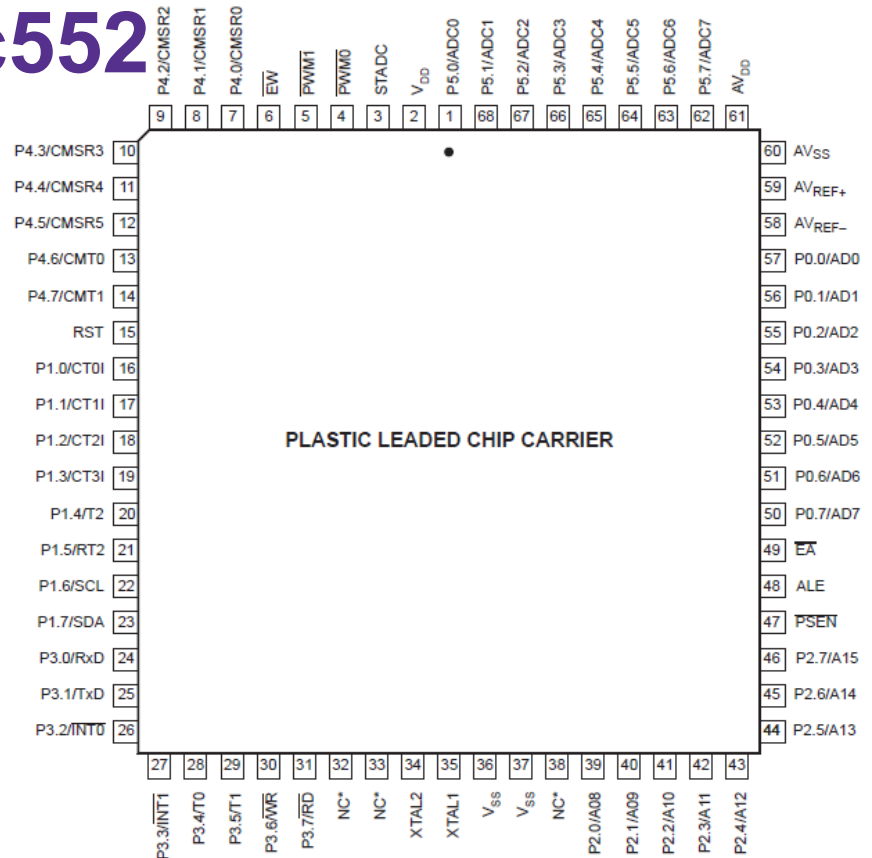
80c552 mikro-kontroladorea

Zelakoa da 80c552 mikro-kontroladorea?

80c51



80c552



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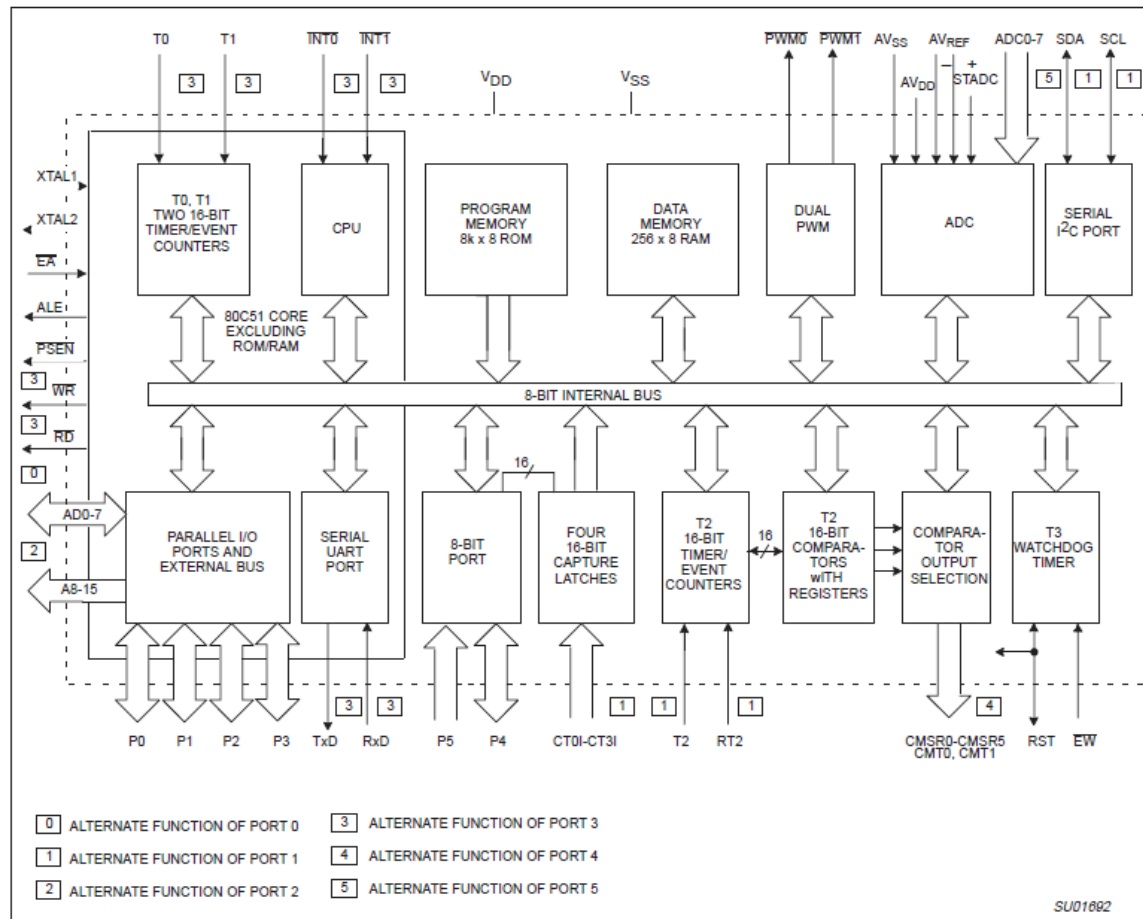
P0-tik P5 era, byte bateko sei aldagai erabili daitezke

Askoz funtzio gehiago, beraz, askoz pin gehiago

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BLOCK DIAGRAM



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8XC552 OVERVIEW

The 8XC552 is a stand-alone high-performance microcontroller designed for use in real-time applications such as instrumentation, industrial control, and automotive control applications such as engine management and transmission control. The device provides, in addition to the 80C51 standard functions, a number of dedicated hardware functions for these applications.

The 8XC552 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 8XC552 uses the powerful instruction set of the 80C51. Additional special function registers are incorporated to control the on-chip peripherals. Three versions of the derivative exist although the generic term "8XC552" is used to refer to family members:

83C552: 8k bytes mask-programmable ROM, 256 bytes RAM

87C552: 8k bytes EPROM, 256 bytes RAM

80C552: ROMless version of the 83C552

The 8XC552 contains a nonvolatile $8k \times 8$ read-only program memory, a volatile 256×8 read/write data memory, five 8-bit I/O

Differences From the 80C51

Program Memory

The 8XC552 contains 8k bytes of on-chip program memory which can be extended to 64k bytes with external memories (see Figure 1). When the \overline{EA} pin is held high, the 8XC552 fetches instructions from internal ROM unless the address exceeds 1FFFFH. Locations 2000H to FFFFFH are fetched from external program memory. When the \overline{EA} pin is held low, all instruction fetches are from external memory. ROM locations 0003H to 0073H are used by interrupt service routines.

Data Memory

The internal data memory is divided into 3 sections: the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte special function register areas. The lower 128 bytes of RAM are directly and indirectly addressable. While RAM locations 128 to 255 and the special function register area share the same address space, they are accessed through different addressing modes. RAM locations 128 to 255 are only indirectly addressable, and the special function registers are only directly addressable. All other aspects of the internal RAM are identical to the 8051.

The stack may be located anywhere in the internal RAM by loading the 8-bit stack pointer. Stack depth is 256 bytes maximum.

Special Function Registers

The special function registers (directly addressable only) contain all of the 8XC552 registers except the program counter and the four register banks. Most of the 56 special function registers are used to control the on-chip peripheral hardware. Other registers include arithmetic registers (ACC, B, PSW), stack pointer (SP), and data pointer registers (DHP, DPL). Sixteen of the SFRs contain 128 directly addressable bit locations. Table 1 lists the 8XC552's special function registers.

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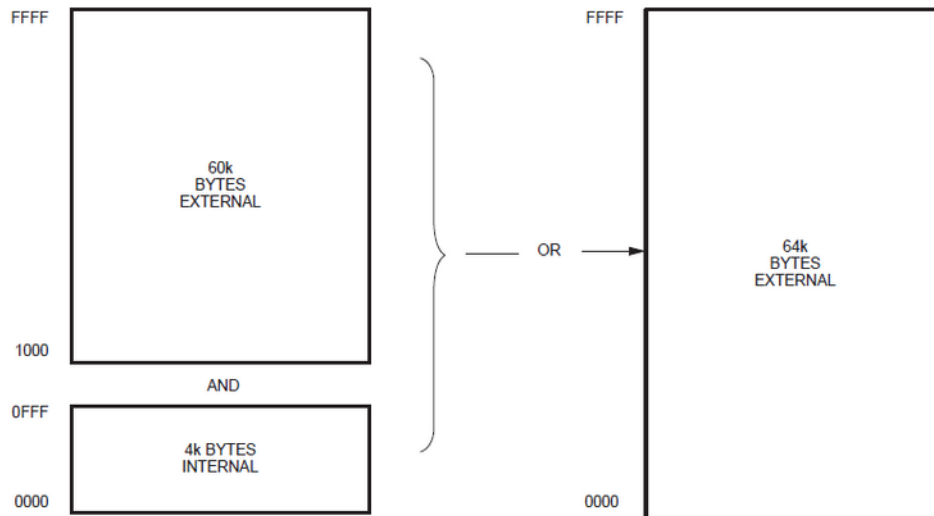
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Zelakoa da 80c552 mikro-kontroladorearen programa memoria?

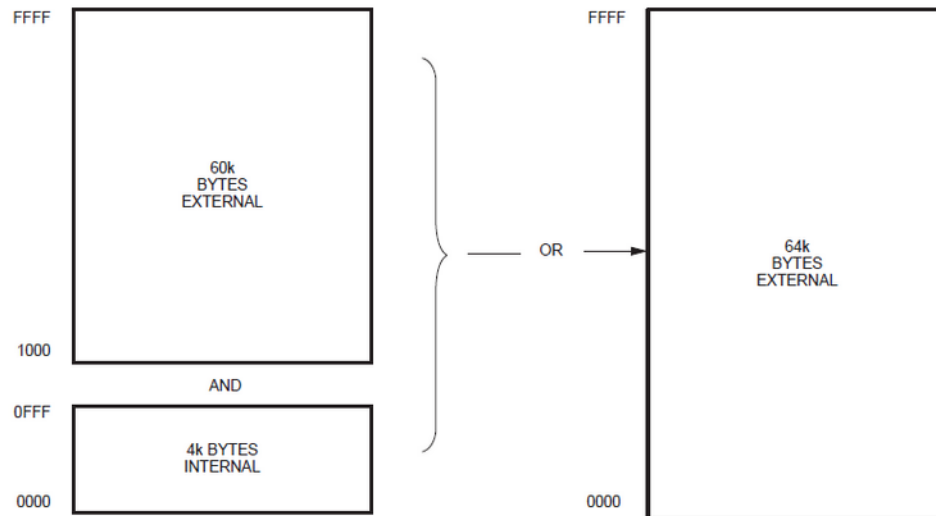
80c51



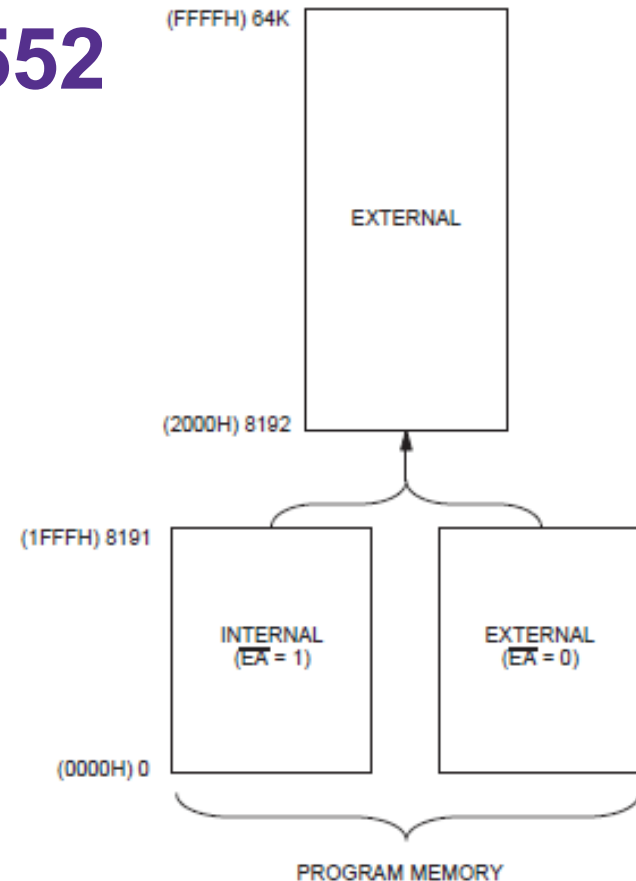
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Zelakoa da 80c552 mikro-kontroladorearen programa memoria? 4kbyte-tik, 8kbyte-era.

80c51



80c552



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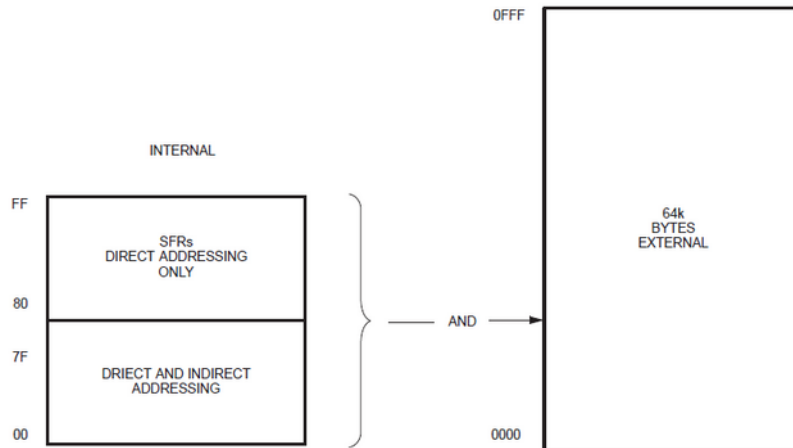
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Zelakoa da 80c552 mikro-kontroladorearen datu memoria?

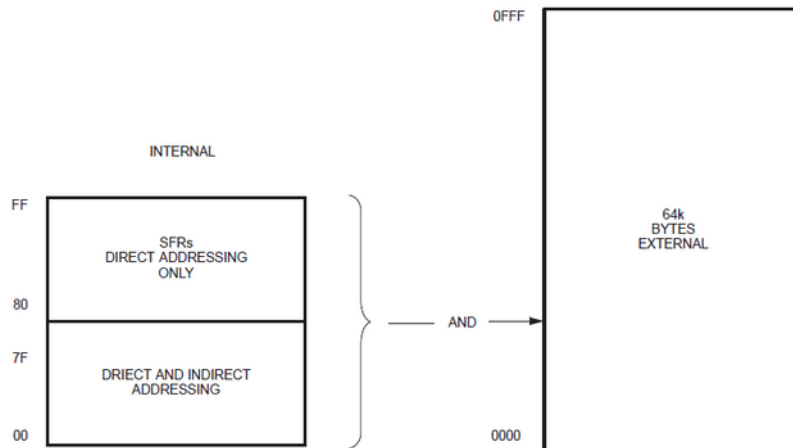
80c51



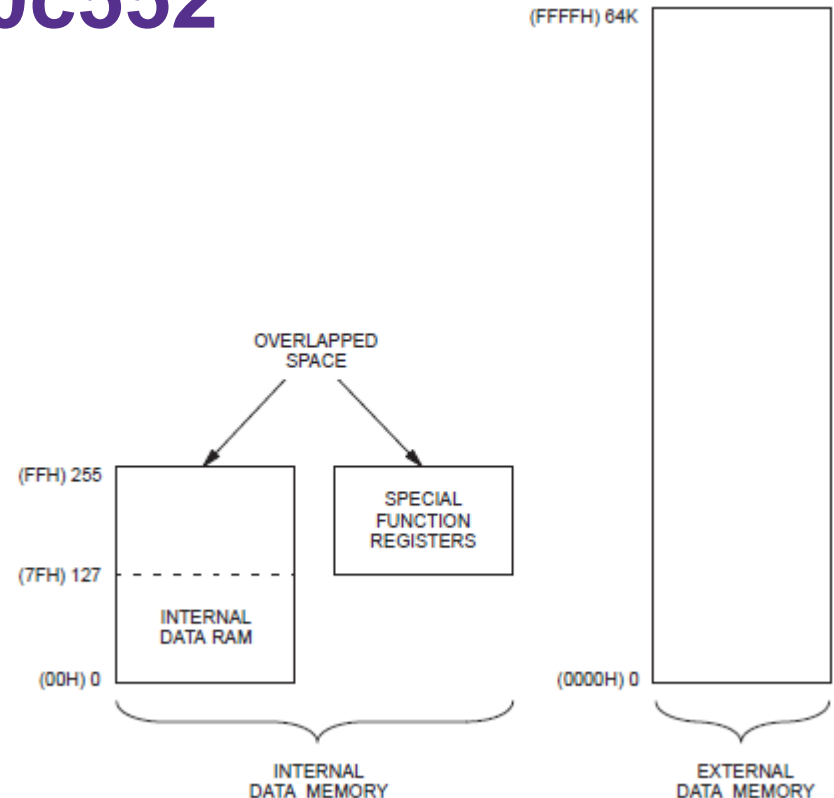
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Zelakoa da 80c552 mikro-kontroladorearen datu memoria? SFR-ko helbideak, memoria bezala erabili ahal.

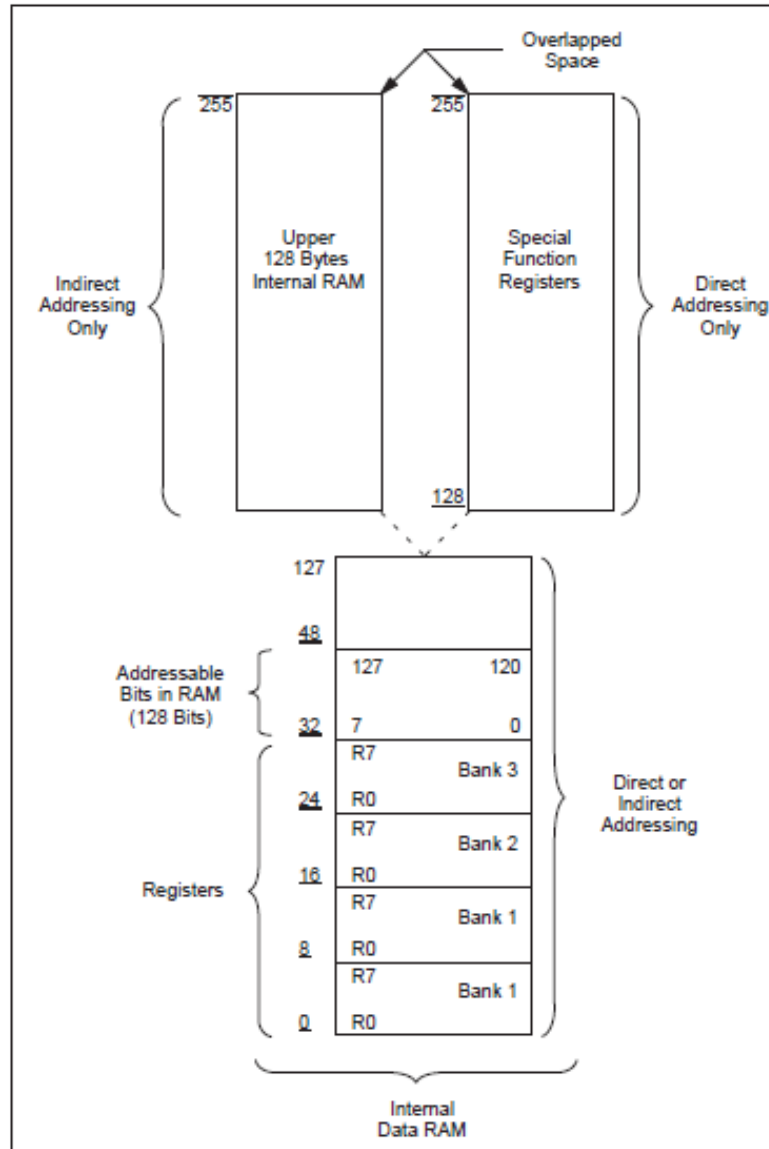
80c51



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Zelakoa da 80c552 mikro-kontroladorearen SFR-a?

80c51

8 BYTES

F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8									DF
D0	PSW								D7
C8									CF
C0									C7
B8	IP								BF
B0	P3								B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	P1								97
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

↑
 BIT ADDRESSABLE

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Zelakoa da 80c552 mikro-kontroladorearen SFR-a?

80c51

8 BYTES

F8							
F0	B						
E8							
E0	ACC						
D8							
D0	PSW						
C8							
C0							
B8	IP						
B0	P3						
A8	IE						
A0	P2						
98	SCON	SBUF					
90	P1						
88	TCON	TMOD	TL0	TL1	TH0	TH1	
80	P0	SP	DPL	DPH			PCON

↑
BIT ADDRESSABLE

80c552

Register Mnemonic	Bit Address	Direct Byte Address (Hex)
T3		FFH
PWMP		FEH
PWM1		FDH
PWM0		FCH
IP1	FF FE FD FC FB FA F9 F8	F8H
B	F7 F6 F5 F4 F3 F2 F1 F0	FOH
RTE		FEH
STE		EEH
#TMH2		EDH
#TML2		ECH
CTCON		EBH
TM2CON		EAH
IE1	EF EE ED EC EB EA E9 E8	E8H
ACC	E7 E6 E5 E4 E3 E2 E1 E0	E0H
S1ADR		DBH
S1DAT		DAH
#S1STA		D9H
S1CON	DF DE DD DC DB DA D9 D8	D8H
PSW	D7 D6 D5 D4 D3 D2 D1 D0	D0H
#CTH3		CFH
#CTH2		CEH
#CTH1		CDH
#CTH0		CCH
CMH2		CBH
CMH1		CAH
CMH0		C9H
TM2IR	CF CE CD CC CB CA C9 C8	C8H
#ADCH		C6H
ADCON		C5H
#P5		C4H
P4	C7 C6 C5 C4 C3 C2 C1 C0	C0H

SFRs containing directly addressable bits

Register Mnemonic	Bit Address	Direct Byte Address (Hex)
IP0	BF BE BD BC BB BA B9 B8	B8H
P3	B7 B6 B5 B4 B3 B2 B1 B0	B0H
#CTL3		AFH
#CTL2		AEH
#CTL1		ADH
#CTL0		ACH
CML2		ABH
CML1		AAH
CML0		A9H
IE0	AF AE AD AC AB AA A9 A8	A8H
P2	A7 A6 A5 A4 A3 A2 A1 A0	A0H
S0BUF		99H
S0CON	9F 9E 9D 9C 9B 9A 99 98	98H
P1	97 96 95 94 93 92 91 90	90H
TH1		8DH
TH0		8CH
TL1		8BH
TL0		8AH
TMOD		89H
TCON	8F 8E 8D 8C 8B 8A 89 88	88H
PCON		87H
DPH		83H
DPL		82H
SP		81H
P0	87 86 85 84 83 82 81 80	80H

SFRs containing directly addressable bits

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Zelakoa da 80c552 mikro-kontroladorearen PSW-a?

80c51

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P
----	----	----	-----	-----	----	---	---

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Zelakoa da 80c552 mikro-kontroladorearen PSW-a?

80c51

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P
----	----	----	-----	-----	----	---	---

80c552

PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P
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Zelakoa dira 80c552 mikro-kontroladorearen interruptzioak?

80c51

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	—	—	ES	ET1	EX1	ET0	EX0
----	---	---	----	-----	-----	-----	-----

IP: INTERRUPT PRIORITY REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is 1 the corresponding interrupt has a higher priority.

—	—	—	PS	PT1	PX1	PT0	PX0
---	---	---	----	-----	-----	-----	-----

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Zelakoa dira 80c552 mikro-kontroladorearen interruptzioak?

80c51

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----	---	---	----	-----	-----	-----	-----

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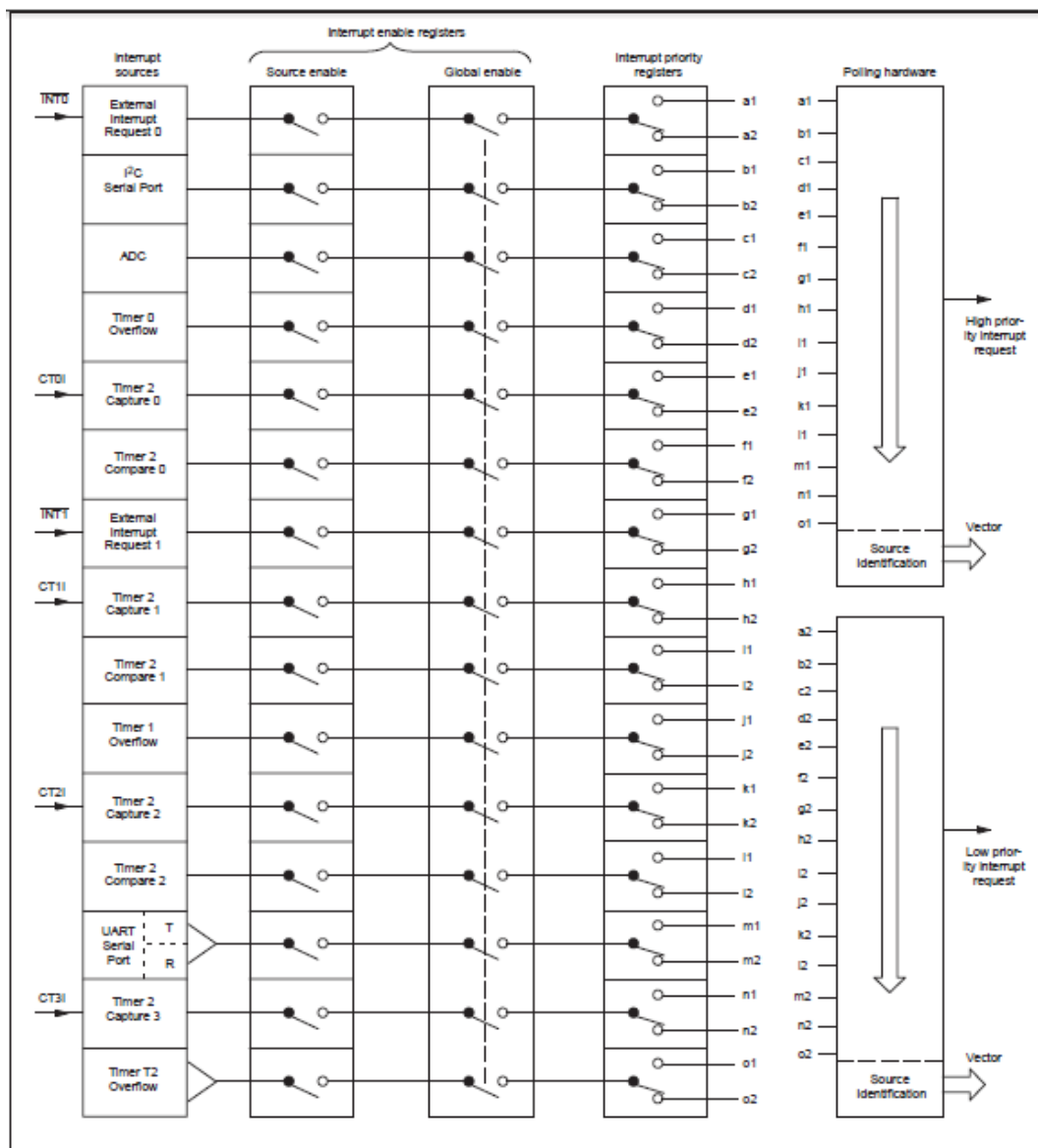
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—	—	—	PS	PT1	PX1	PT0	PX0
---	---	---	----	-----	-----	-----	-----

80c552

IEN0*#	Interrupt enable 0	A8H	EA	EAD	ES1	ES0	ET1	EX1	ET0	EX0	00H
			EF	EE	ED	EC	EB	EA	E9	E8	
IEN1*#	Interrupt enable 1	E8H	ET2	ECM2	ECM1	ECM0	ECT3	ECT2	ECT1	ECT0	00H
			BF	BE	BD	BC	BB	BA	B9	B8	
IP0*#	Interrupt priority 0	B8H	—	PAD	PS1	PS0	PT1	PX1	PT0	PX0	x0000000B
			FF	FE	FD	FC	FB	FA	F9	F8	
IP1*#	Interrupt priority 1	F8H	PT2	PCM2	PCM1	PCM0	PCT3	PCT2	PCT1	PCT0	00H

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KONPUTAGAILUEN ARKITEKTURA

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Irakaslea: Alain Sanchez
(alain.sanchez@ehu.eus)

2019-2020, 1. lauhilabetea