eman ta zabal zazu

Universidad del País Vasco
Euskal Herriko Unibertsitatea

BILBOKO INGENIARITZA ESKOLA
ESCUELA DE INGENIERÍA DE BILBAO

Teknologia Elektronikoa Saila

KONPUTAGAILUEN ARKITEKTURA
80c51 mikro-kontroladorea

Kudeaketa eta Informazio Sistemen Informatikaren Ingenieritzako Graduaren 3. maila

Irakaslea: Alain Sanchez
(alain.sanchez@ehu.eus)

2019-2020, 1. lauhilabetea

HELBURUAK

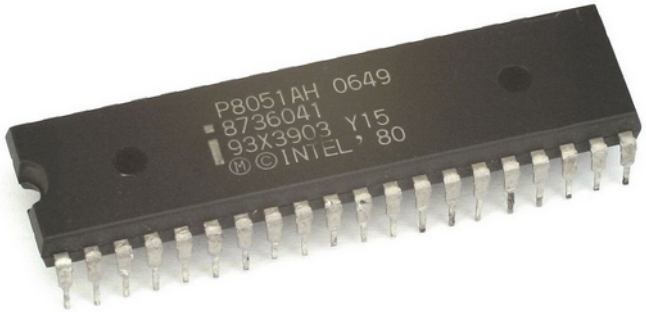
80c51 familia ezagutzea

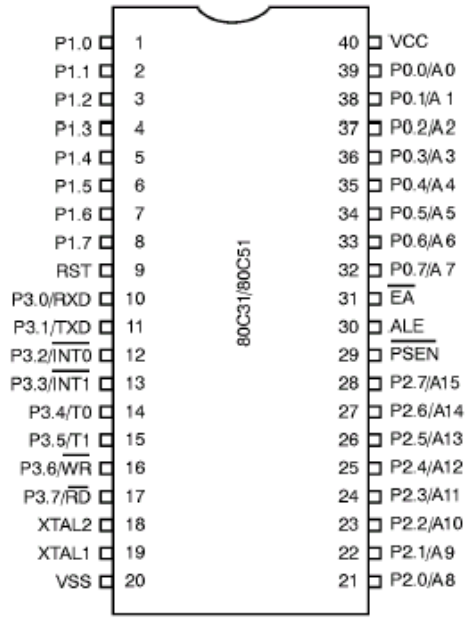
Memorien banaketa ulertzea

80c51 mikro-kontroladorea

Zelakoa da 80c51 mikro-kontroladorea?

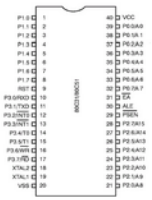
Bi deskribapen mota: datasheet elektrikoa eta “dokumentu funtzionala”





80c51 mikro-kontroladorea

Datasheet elektrikoa: konexio elektrikoak definitu

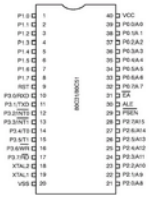


80c51 mikro-kontroladorea

Datasheet elektrikoa: konexio elektrikoak definitu

Ze tentsiora elikatzen da?

Zer da ‘1’? Eta ‘0’?



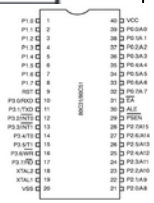
80c51 mikro-kontroladorea

Datasheet elektrikoa: konexio elektrikoak definitu

DC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C or –40°C to +85°C, V_{CC} = 2.7 V to 5.5 V, V_{SS} = 0 V (16 MHz devices)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
V_{IL}	Input low voltage[11]	4.0 V < V_{CC} < 5.5 V	–0.5		0.2 V_{CC}–0.1	V
		2.7 V<V_{CC}< 4.0 V	–0.5		0.7	V
V_{IH}	Input high voltage (ports 0, 1, 2, 3, $\overline{EA}$)		0.2 V_{CC}+0.9		V_{CC}+0.5	V
V_{IH1}	Input high voltage, XTAL1, RST[11]		0.7 V_{CC}		V_{CC}+0.5	V
V_{OL}	Output low voltage, ports 1, 2, [8]	V_{CC} = 2.7 V I_{OL} = 1.6 mA[2]			0.4	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$[8, 7]	V_{CC} = 2.7 V I_{OL} = 3.2 mA[2]			0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3 [3]	V_{CC} = 2.7 V I_{OH} = –20 µA	V_{CC} – 0.7			V
		V_{CC} = 4.5 V I_{OH} = –30 µA	V_{CC} – 0.7			V
V_{OH1}	Output high voltage (port 0 in external bus mode), ALE[9], $\overline{PSEN}$[3]	V_{CC} = 2.7 V I_{OH} = –3.2 mA	V_{CC} – 0.7			V



80c51 mikro-kontroladorea

Dokumentu funtzionala: hardware-a zelan definituta dagoen eta zelan konfiguratu

Philips Semiconductors

80C51 Family

80C51 family programmer's guide and instruction set

80c51 - Memoria

Zer da memoria bat?

Zer egiten du memoria batek?

Ze memoria mota daude?

80c51 - Memoria

Zer da memoria bat?

Zer egiten du memoria batek?

Ze memoria mota daude?

RAM	ROM
1. Temporary Storage.	1. Permanent storage.
2. Store data in MBs.	2. Store data in GBs.
3. Volatile.	3. Non-volatile.
4.Used in normal operations.	4. Used for startup process of computer.
5. Writing data is faster.	5. Writing data is slower.

80c51 - Memoria

Programa memoria

Datu memoria

Zein da zer?

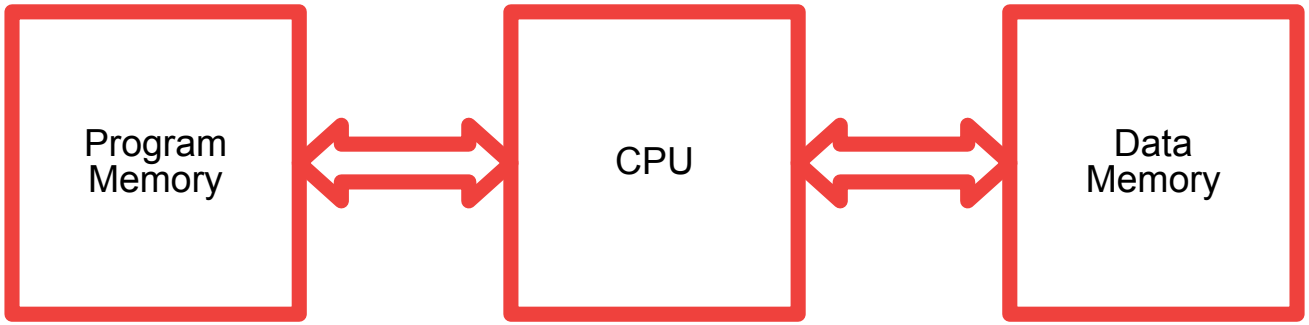
80c51 - Memoria

ROM

Programa memoria: Read Only Memory (ROM)

RAM

Datu memoria: Random Access Memory (RAM)



80c51 - Memoria

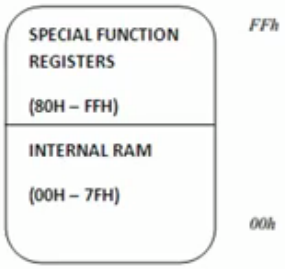
ROM

Programa memoria: Read Only Memory (ROM)

RAM

Datu memoria: Random Access Memory (RAM)

- ***Program memory*** is normally referred to be ROM which is non volatile memory and read only in nature. It is used store
  - Boot up programs.
  - ISR (Interrupt service routines)
  - Macro functions
- ***Data memory*** is useful in the case of storage of data temporarily, say during context switching. 8051 is organized so neatly with 256 bytes of memory and they are split as follows.
  - First 128 bytes: 00h to 1Fh Register Banks
  - 20h to 2Fh Bit Addressable RAM
  - 30 to 7Fh General Purpose RAM
  - Next 128 bytes: 80h to FFh Special Function Registers



80c51 - Memoria

PROGRAMMER'S GUIDE AND INSTRUCTION SET

Memory Organization

Program Memory

The 80C51 has separate address spaces for program and data memory. The Program memory can be up to 64k bytes long. The lower 4k can reside on-chip. Figure 1 shows a map of the 80C51 program memory.

The 80C51 can address up to 64k bytes of data memory to the chip. The MOVX instruction is used to access the external data memory.

The 80C51 has 128 bytes of on-chip RAM, plus a number of Special Function Registers (SFRs). The lower 128 bytes of RAM can be accessed either by direct addressing (MOV data addr) or by indirect addressing (MOV @Ri). Figure 2 shows the Data Memory organization.

Direct and Indirect Address Area

The 128 bytes of RAM which can be accessed by both direct and indirect addressing can be divided into three segments as listed below and shown in Figure 3.

1. Register Banks 0-3: Locations 0 through 1FH (32 bytes). The device after reset defaults to register bank 0. To use the other register banks, the user must select them in software. Each register bank contains eight 1-byte registers 0 through 7. Reset initializes the stack pointer to location 07H, and it is incremented once to start from location 08H, which is the first register (R0) of the second register bank. Thus, in order to use more than one register bank, the SP should be initialized to a different location of the RAM where it is not used for data storage (i.e., the higher part of the RAM).
2. Bit Addressable Area: 16 bytes have been assigned for this segment, 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH). The bits can be referred to in two ways, both of which are acceptable by most assemblers. One way is to refer to their address (i.e., 0-7FH). The other way is with reference to bytes 20H to 2FH. Thus, bits 0-7 can also be referred to as bits 20.0-20.7, and bits 8-FH are the same as 21.0-21.7, and so on. Each of the 16 bytes in this segment can also be addressed as a byte.
3. Scratch Pad Area: 30H through 7FH are available to the user as data RAM. However, if the stack pointer has been initialized to this area, enough bytes should be left aside to prevent SP data destruction.

Figure 2 shows the different segments of the on-chip RAM.

80c51 - Memoria

PROGRAMMER'S GUIDE AND INSTRUCTION SET

Memory Organization

Program Memory

The 80C51 has separate address spaces for program and data memory. The Program memory can be up to 64k bytes long. The lower 4k can reside on-chip. Figure 1 shows a map of the 80C51 program memory.

The 80C51 can address up to 64k bytes of data memory to the chip. The MOVX instruction is used to access the external data memory.

The 80C51 has 128 bytes of on-chip RAM, plus a number of Special Function Registers (SFRs). The lower 128 bytes of RAM can be accessed either by direct addressing (MOV data addr) or by indirect addressing (MOV @Ri). Figure 2 shows the Data Memory organization.

Direct and Indirect Address Area

The 128 bytes of RAM which can be accessed by both direct and indirect addressing can be divided into three segments as listed below and shown in Figure 3.

1. Register Banks 0-3: Locations 0 through 1FH (32 bytes). The device after reset defaults to register bank 0. To use the other register banks, the user must select them in software. Each register bank contains eight 1-byte registers 0 through 7. Reset initializes the stack pointer to location 07H, and it is incremented once to start from location 08H, which is the first register (R0) of the second register bank. Thus, in order to use more than one register bank, the SP should be initialized to a different location of the RAM where it is not used for data storage (i.e., the higher part of the RAM).
2. Bit Addressable Area: 16 bytes have been assigned for this segment, 20H-2FH. Each one of the 128 bits of this segment can be directly addressed (0-7FH). The bits can be referred to in two ways, both of which are acceptable by most assemblers. One way is to refer to their address (i.e., 0-7FH). The other way is with reference to bytes 20H to 2FH. Thus, bits 0-7 can also be referred to as bits 20.0-20.7, and bits 8-FH are the same as 21.0-21.7, and so on. Each of the 16 bytes in this segment can also be addressed as a byte.
3. Scratch Pad Area: 30H through 7FH are available to the user as data RAM. However, if the stack pointer has been initialized to this area, enough bytes should be left aside to prevent SP data destruction.

Figure 2 shows the different segments of the on-chip RAM.

80c51 - Programa memoria

Programa memoria: Read Only Memory (ROM)

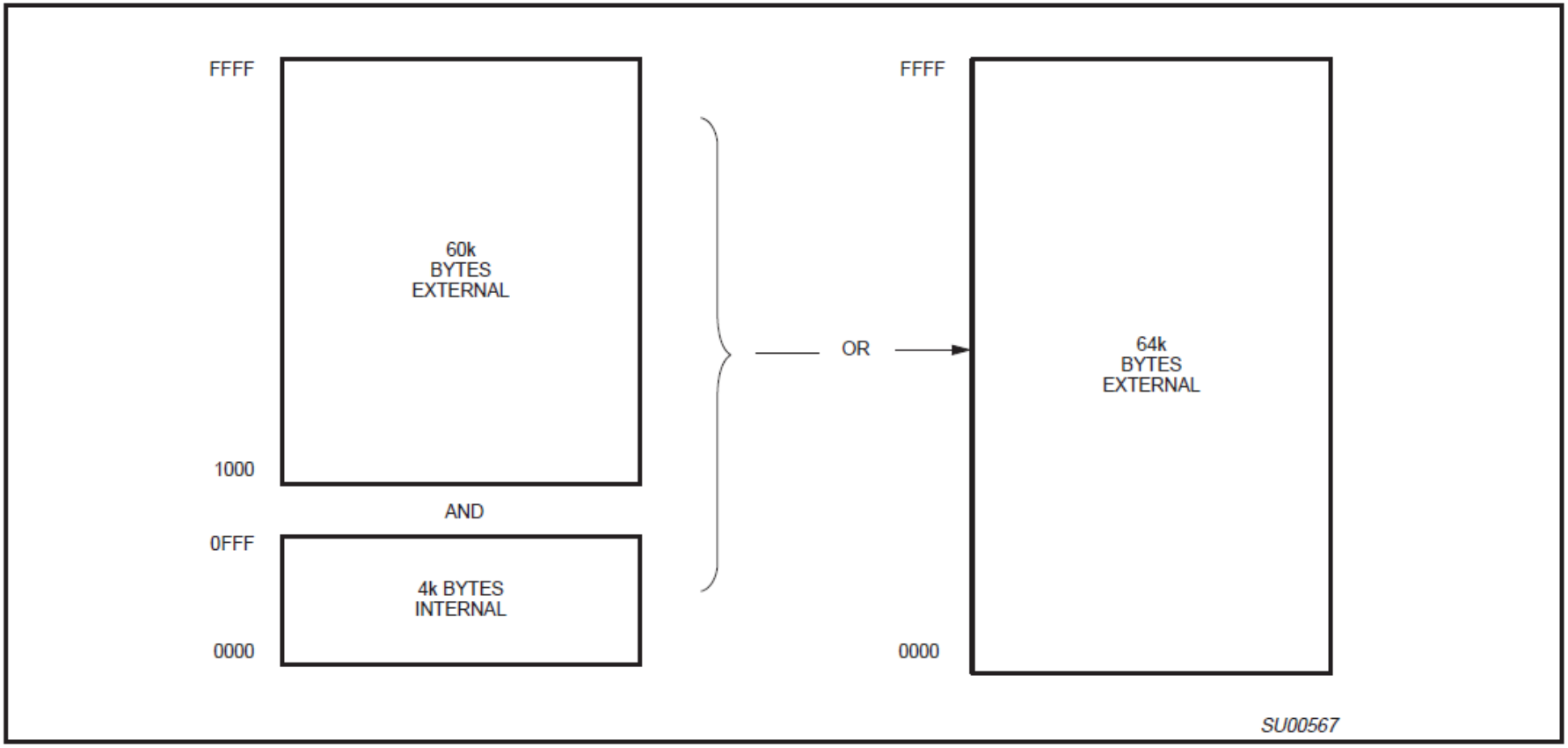


Figure 1. 80C51 Program Memory

80c51 - Datu memoria

Datu memoria: Random Access Memory (RAM)

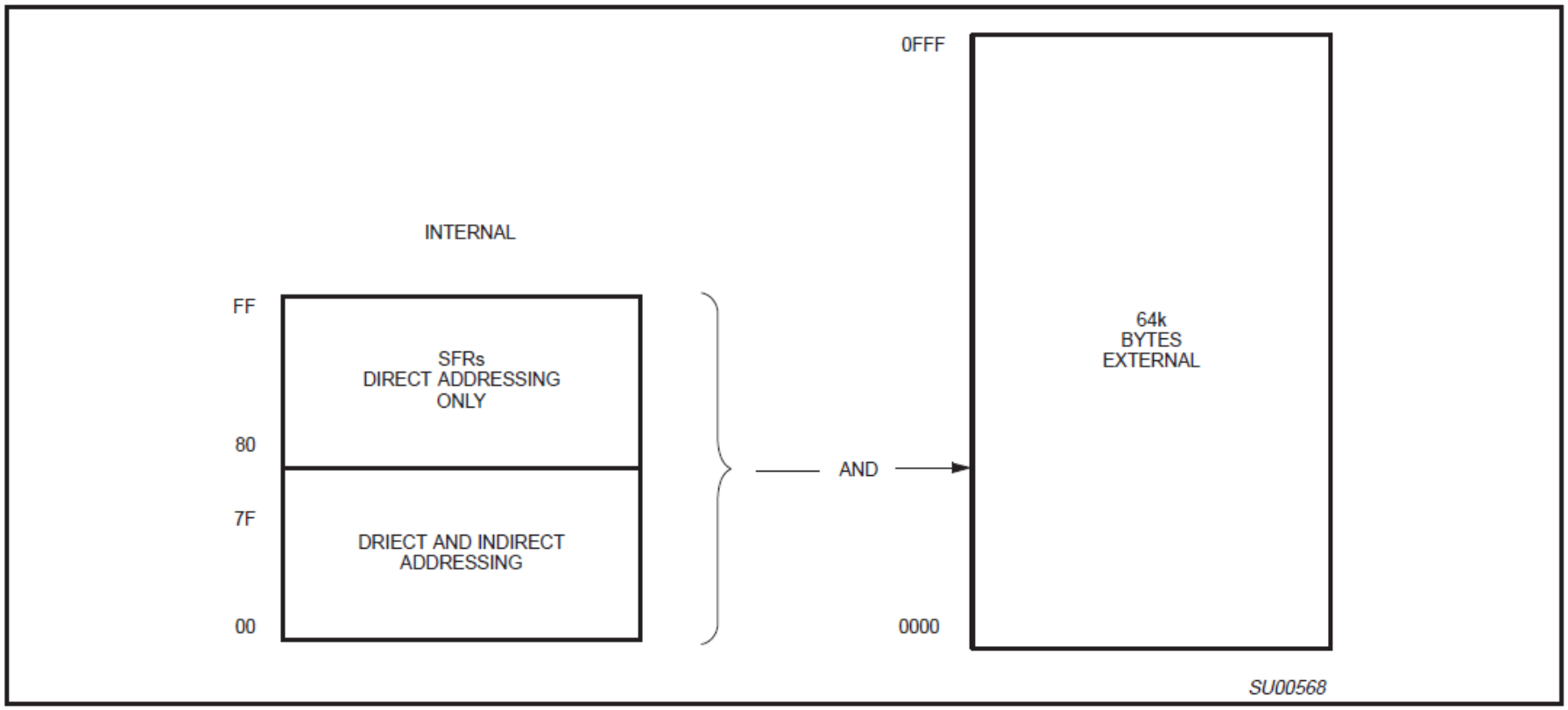


Figure 2. 80C51 Data Memory

80c51 - Datu memoria

Datu memoria: Random Access Memory (RAM)

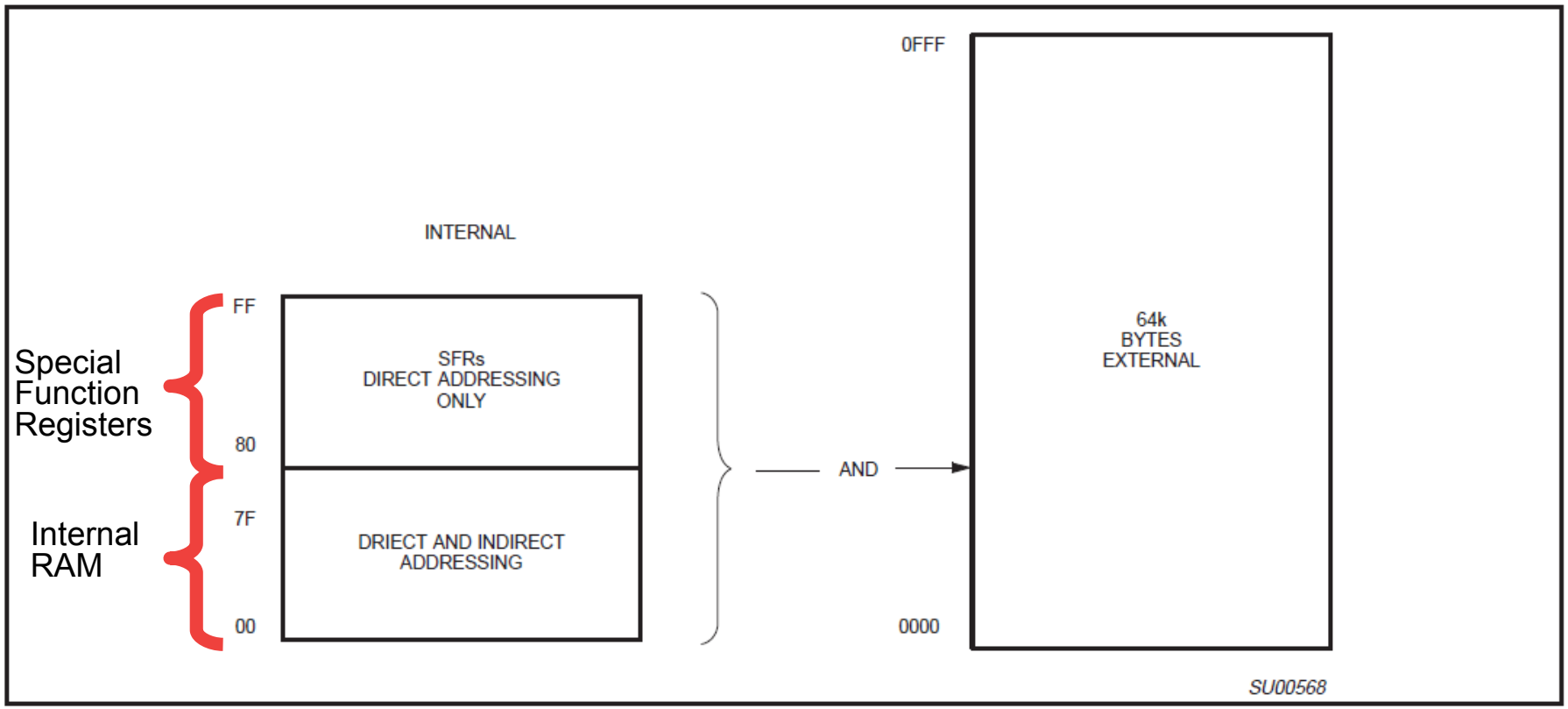


Figure 2. 80C51 Data Memory

80c51 - Datu memoria

Barne RAM: hiru zatitan banatu

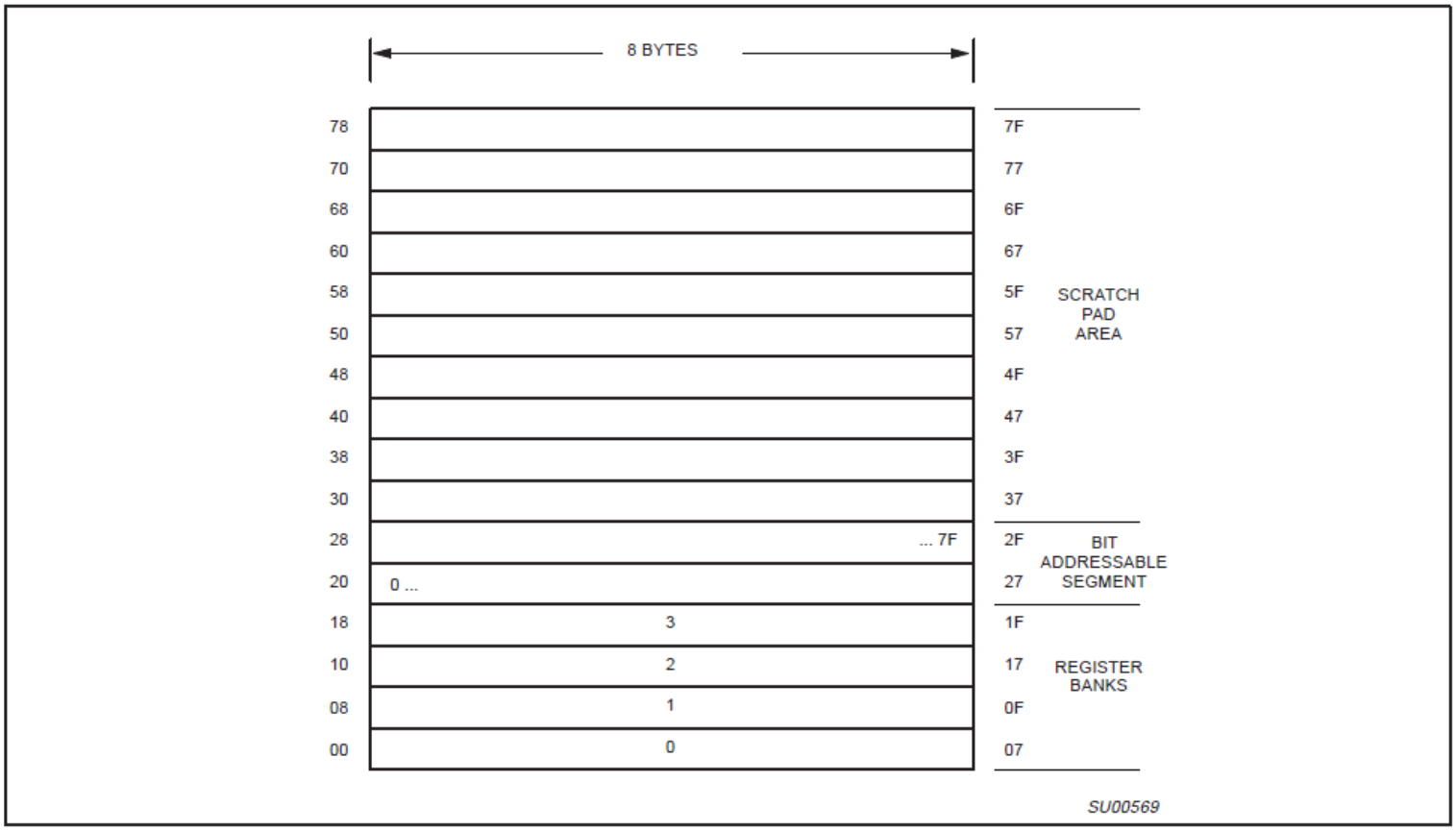
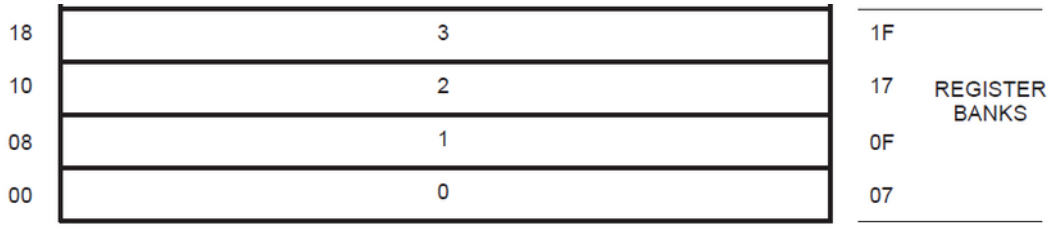


Figure 3. 128 Bytes of RAM Direct and Indirect Addressable

80c51 - Datu memoria

Register Bank: R0..R7, byte (8 bit) bateko 8 aldagai



PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P

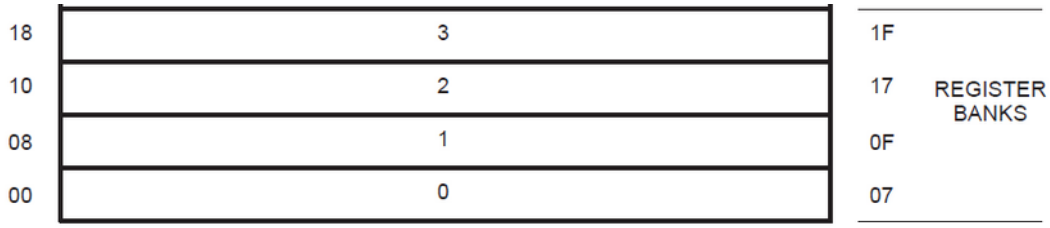
CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary Carry Flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1 (SEE NOTE 1).
RS0	PSW.3	Register Bank selector bit 0 (SEE NOTE 1).
OV	PSW.2	Overflow Flag.
–	PSW.1	Usable as a general purpose flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bus in the accumulator.

NOTE:
1. The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

80c51 - Datu memoria

Register Bank: R0..R7, byte (8 bit) bateko 8 aldagai



PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P

CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary Carry Flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1 (SEE NOTE 1).
RS0	PSW.3	Register Bank selector bit 0 (SEE NOTE 1).
OV	PSW.2	Overflow Flag.
–	PSW.1	Usable as a general purpose flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bus in the accumulator.

NOTE:
1. The value presented by RS0 and RS1 selects the corresponding register bank.

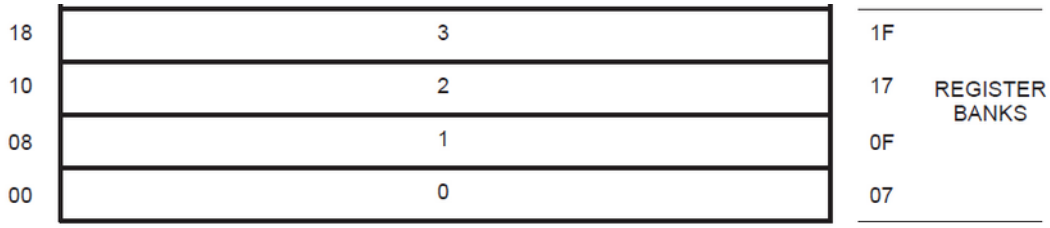
RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

***Nemonikoa erabili daiteke.**
***Era zuzen edo ez zuzenean erabili daiteke.**

MOV R0,#80H
MOV @R0,#0FH

80c51 - Datu memoria

Register Bank: R0..R7, byte (8 bit) bateko 8 aldagai



PSW: PROGRAM STATUS WORD, BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P

CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary Carry Flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1 (SEE NOTE 1).
RS0	PSW.3	Register Bank selector bit 0 (SEE NOTE 1).
OV	PSW.2	Overflow Flag.
–	PSW.1	Usable as a general purpose flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bus in the accumulator.

NOTE:
1. The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

80c51 - Datu memoria

Bit Addressable Segment:

Bitez bit programa daitekeen memoria zatia.

Helbide bakoitzean byte bakoitzeko bit batera heltzeko gaitasuna.

Bi eratan heldu daiteke helbidera:

- Bytearen balioa emanez.
- Bita programatuz.

80c51 - Datu memoria

Bit Addressable Segment:

Bitez bit programa daitekeen memoria zatia.

Helbide bakoitzean byte bakoitzeko bit batera heltzeko gaitasuna.

Bi eratan heldu daiteke helbidera:

Bytearen balioa emanez.

Bita programatuz.

Aginduak:

SETB

CLR

SETB 20H.0

CLR 20H.0

80c51 - Datu memoria

Bit Addressable Segment:

Bitez bit programa daitekeen memoria zatia.

Helbide bakoitzean byte bakoitzeko bit batera heltzeko gaitasuna.

Bi eratan heldu daiteke helbidera:

Bytearen balioa emanez.

Bita programatuz.

Non 20H.0, 0H den.

Aginduak:

SETB
CLR

SETB	*20H.7*	*SETB*	*07H*
CLR	*20H.7*	*CLR*	*07H*

80c51 - Datu memoria

General Purpose RAM: Edozer gordetzeko erabili daitekeen memoria zatia.

80c51 - Datu memoria

Datu memoria: Random Access Memory (RAM)

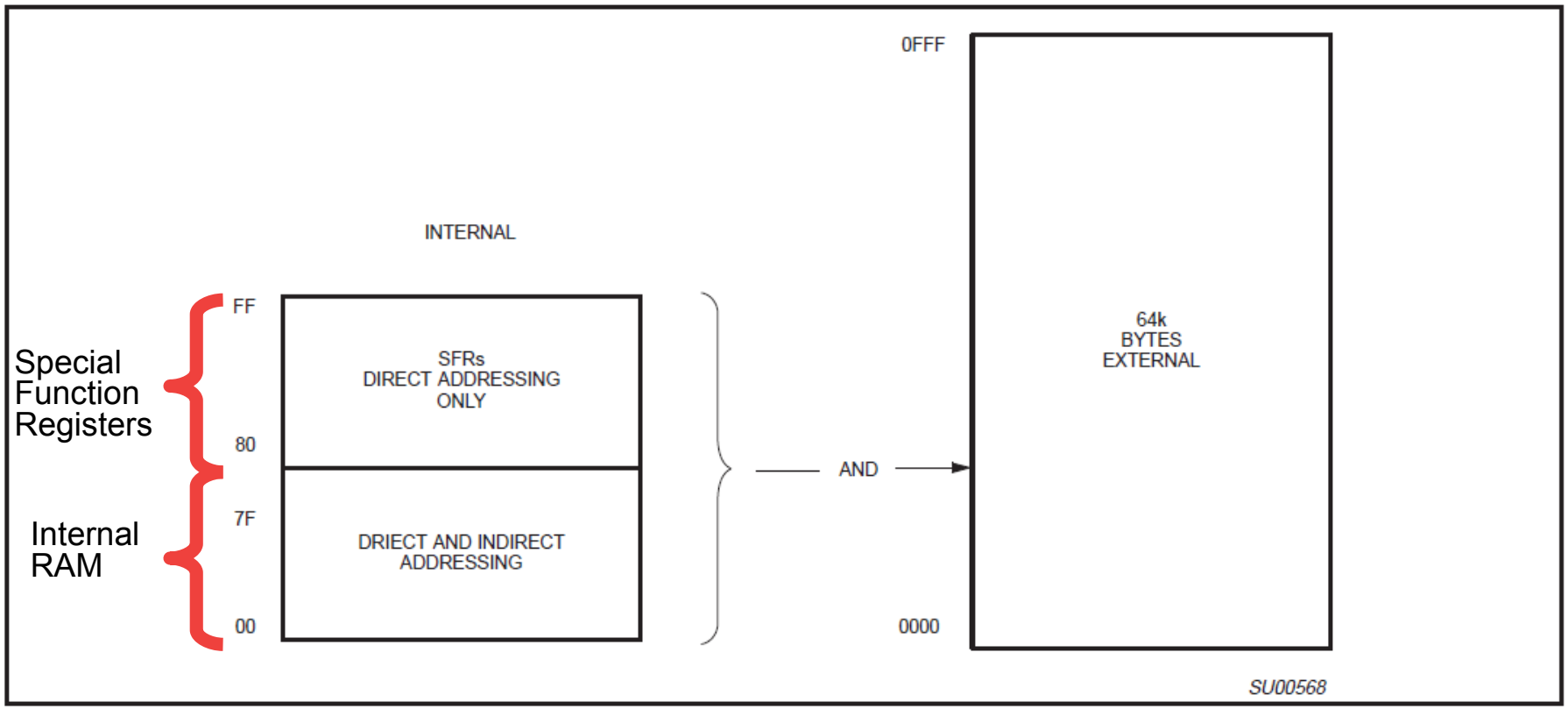


Figure 2. 80C51 Data Memory

80c51 - Special Function Register

SFR: Funtzio ezberdinak konfiguratzeko memoria zatia

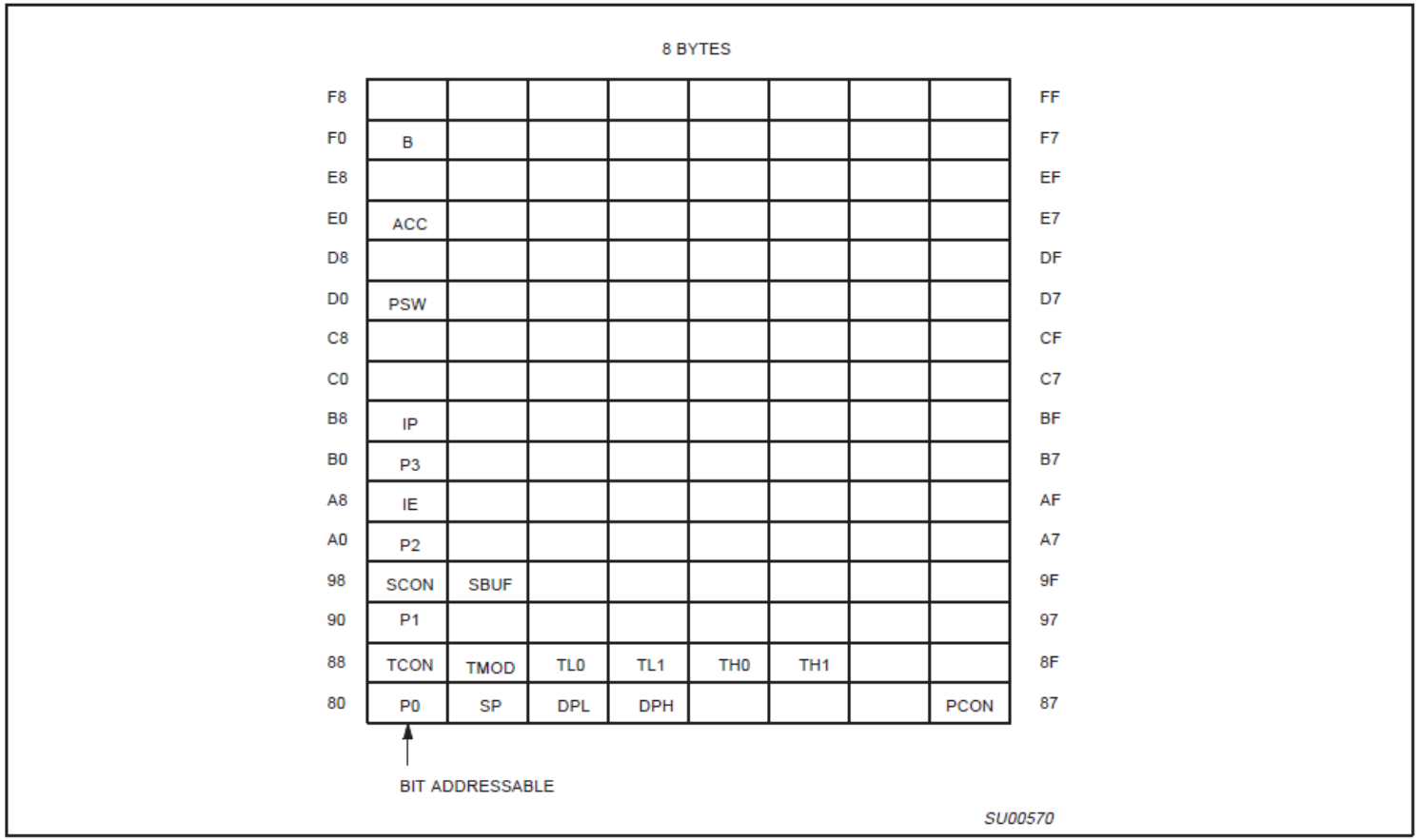


Figure 4. SFR Memory Map

80c51 - Datu memoria

Register Bank

-->Lau banku ezberdin.
-->Banku bakoitzak R0-tik R7-ra. R bakoitzak 8 bit.
-->RAM memorian 00H-tik 1FH-ra.
-->Helbideratze zuzena eta ez zuzena.
-->RS0 eta RS1 bitekin aukeratu bankua.
-->Agindu tipikoa: MOV

Bit Addressable Segment

-->Bit bakarra programatu daiteke.
-->RAM memorian 20H-tik 2FH-ra.
-->Izendatzeko bi aukera:
---->Byte zenbakia . Bit zenbakia.
----> Bit zenbakia nun 20H, 0H den; eta 2FH, 7FH.
----> Agindu tipikoak: SETB, CLR.

80c51 - Datu memoria

RAM generikoa

-->RAM memorian 30H-tik 7FH-ra.
-->Helbideratze zuzena.
-->Agindu tipikoa: MOV

Special Function Register

-->Mikro-kontroladorearen funtzio ezberdinak kontrolatzeko memoria.

80c51 - Datu memoria

1.- Bank2-ko R5 posizioan, 50H balioa gorde nahi da.

2.- Bank0-ko R3 posizioan, 60H balioa gorde nahi da, eta 60H helbidean (R3 erabiliz), 55H balioa.

3.- 21.7 bita ‘1’era jarri nahi da (bit zenbakia erabiliz) eta 6F bita ‘0’ra jarri nahi da,

80c51 - Special Function Register

SFR: Funtzio ezberdinak konfiguratzeko memoria zatia

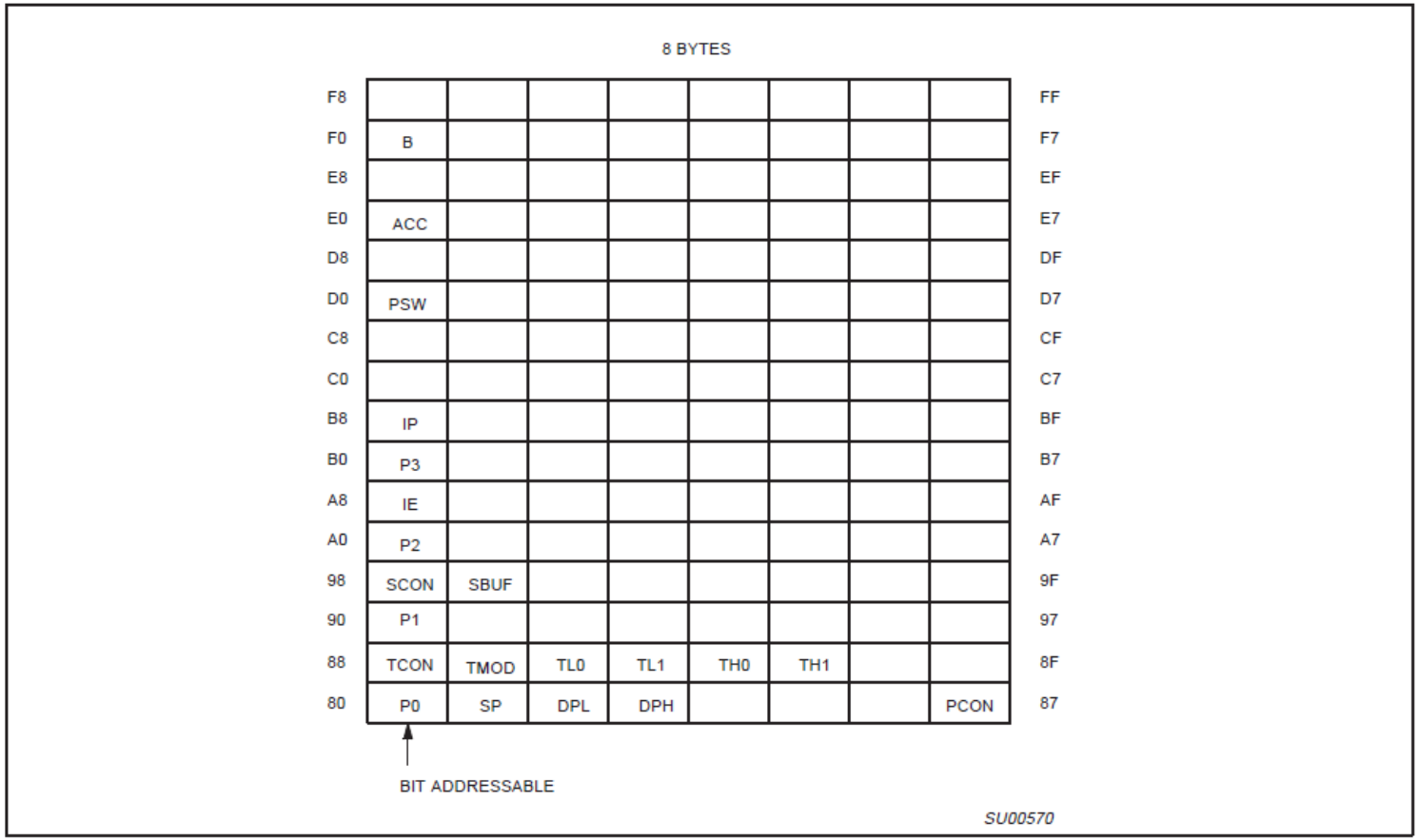
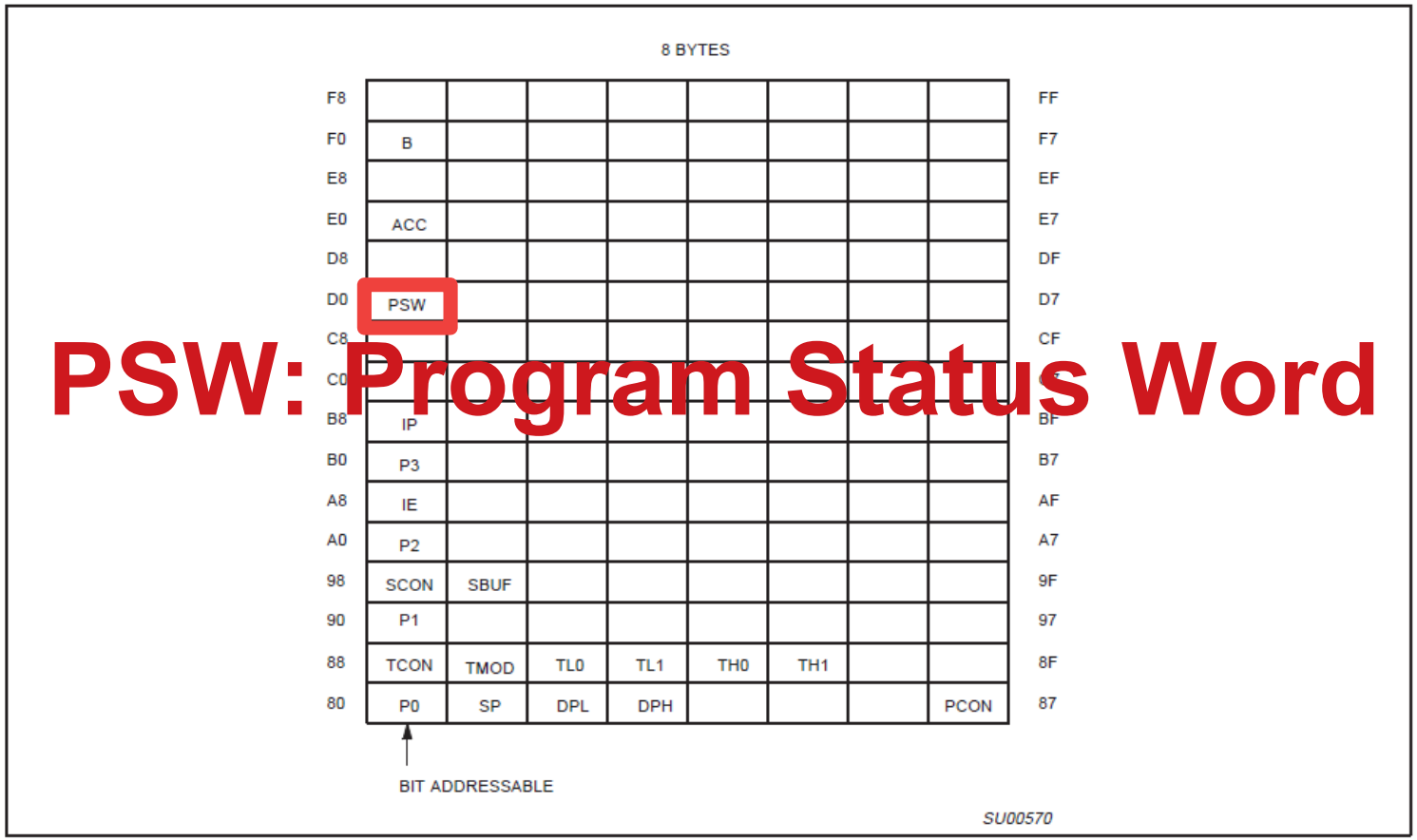


Figure 4. SFR Memory Map

80c51 - Special Function Register

SFR: Funtzio ezberdinak konfiguratzeko memoria zatia



PSW: Program Status Word

Figure 4. SFR Memory Map

80c51 - Special Function Register

PSW: Program Status Word

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P

CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary Carry Flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1 (SEE NOTE 1).
RS0	PSW.3	Register Bank selector bit 0 (SEE NOTE 1).
OV	PSW.2	Overflow Flag.
–	PSW.1	Usable as a general purpose flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bus in the accumulator.

NOTE:
1. The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

80c51 - [SFR] PSW: Program Status Word

PSW: Program Status Word

CY: batuketa baten 9. bit (D8?) bat behar denean aktibatzen da.

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P

80c51 - [SFR] PSW: Program Status Word

PSW: Program Status Word

CY: batuketa baten 9. bit (D8?) bat behar denean aktibatzen da.

AC: batuketa baten D3-tik D4-ra carry-a dagoenan. BCD-rekin (Binary Coded Decimal) lotuta.

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

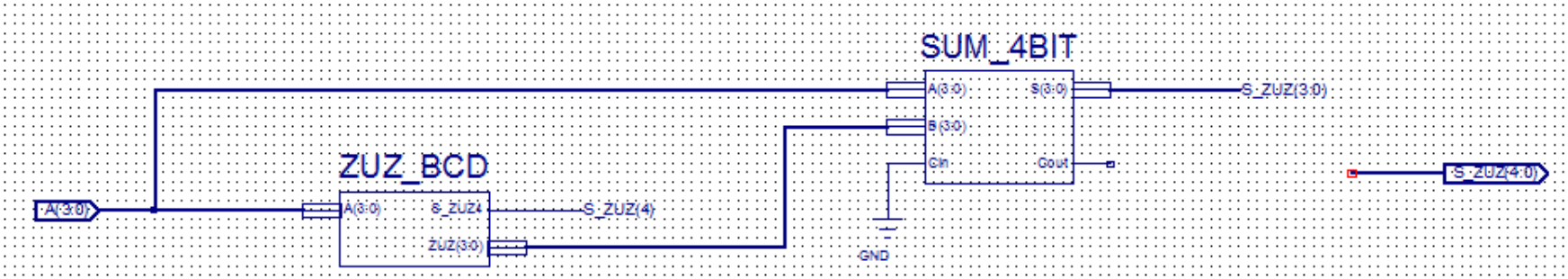
CY	AC	F0	RS1	RS0	OV	–	P

80c51 - [SFR] PSW: Program Status Word

PSW: Program Status Word

CY: batuketa baten 9. bit (D8?) bat behar denean aktibatzen da.

AC: batuketa baten D3-tik D4-ra carry-a dagoenan. BCD-rekin (Binary Coded Decimal) lotuta.



PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

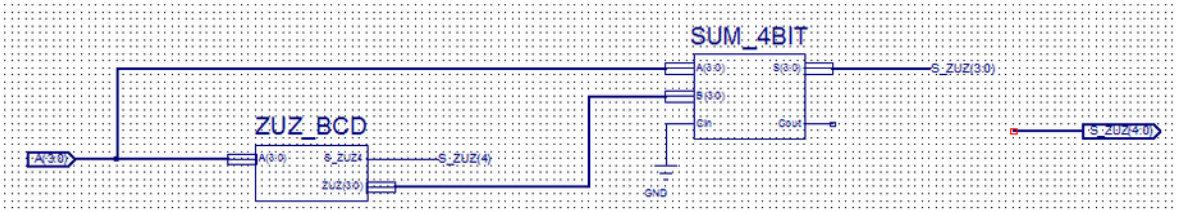
CY	AC	F0	RS1	RS0	OV	–	P

80c51 - [SFR] PSW: Program Status Word

PSW: Program Status Word

CY: batuketa baten 9. bit (D8?) bat behar denean aktibatzen da.

AC: batuketa baten D3-tik D4-ra carry-a dagoenan. BCD-rekin (Binary Coded Decimal) lotuta.




```
  0010 0101   25
+ 0100 1000   48
-------------
  0110 1101   6D, intermediate result
+      0110   06, adjustment
-------------
  0111 0011   73, adjusted result
```

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P

80c51 - [SFR] PSW: Program Status Word

PSW: Program Status Word

CY: batuketa baten 9. bit (D8?) bat behar denean aktibatzen da.

AC: batuketa baten D3-tik D4-ra carry-a dagoenan. BCD-rekin (Binary Coded Decimal) lotuta.

OV: ikurra daukaten zenbakien eragiketetan Overflow (gainezkatzea) ematen denean.

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P

80c51 - [SFR] PSW: Program Status Word

PSW: Program Status Word

CY: batuketa baten 9. bit (D8?) bat behar denean aktibatzen da.

AC: batuketa baten D3-tik D4-ra carry-a dagoenan. BCD-rekin (Binary Coded Decimal) lotuta.

OV: ikurra daukaten zenbakien eragiketetan Overflow (gainezkatzea) ematen denean.

P: ‘1’ kopurua bikoitia izateko hartzen du balioa partitate bitak.

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	–	P

80c51 - [SFR] PSW: Program Status Word

PSW-ko ze bit aktibatzen dira eragiketa hauekin?

1.- E0H + 43H

2.- AAH + 98H

3.- 0FH + 11H

4.- 90H + F0H

80c51 - Special Function Register

SFR: Funtzio ezberdinak konfiguratzeko memoria zatia

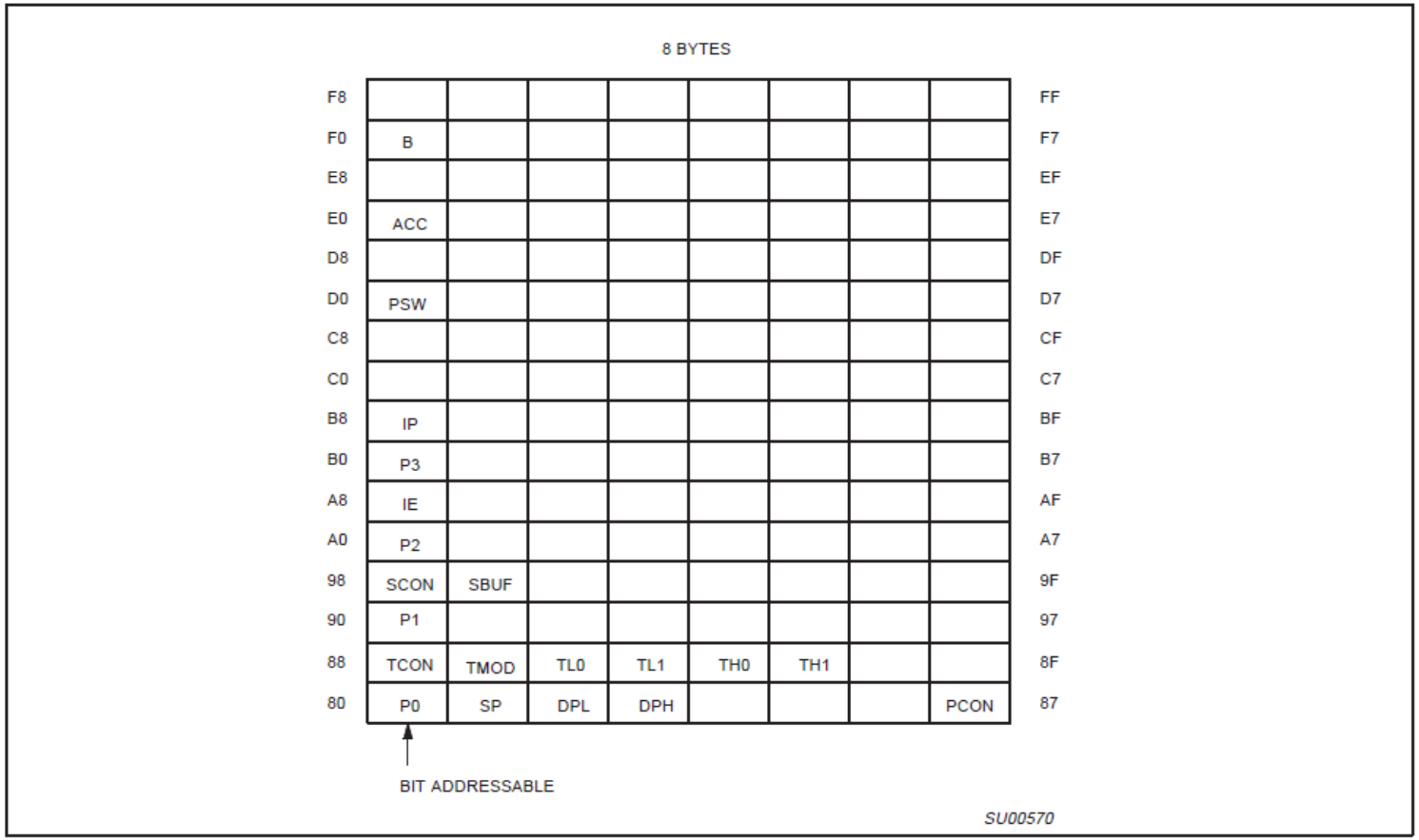


Figure 4. SFR Memory Map

80c51 - Special Function Register

SFR: Funtzio ezberdinak konfiguratzeko memoria zatia

IE: Interrupt Enable

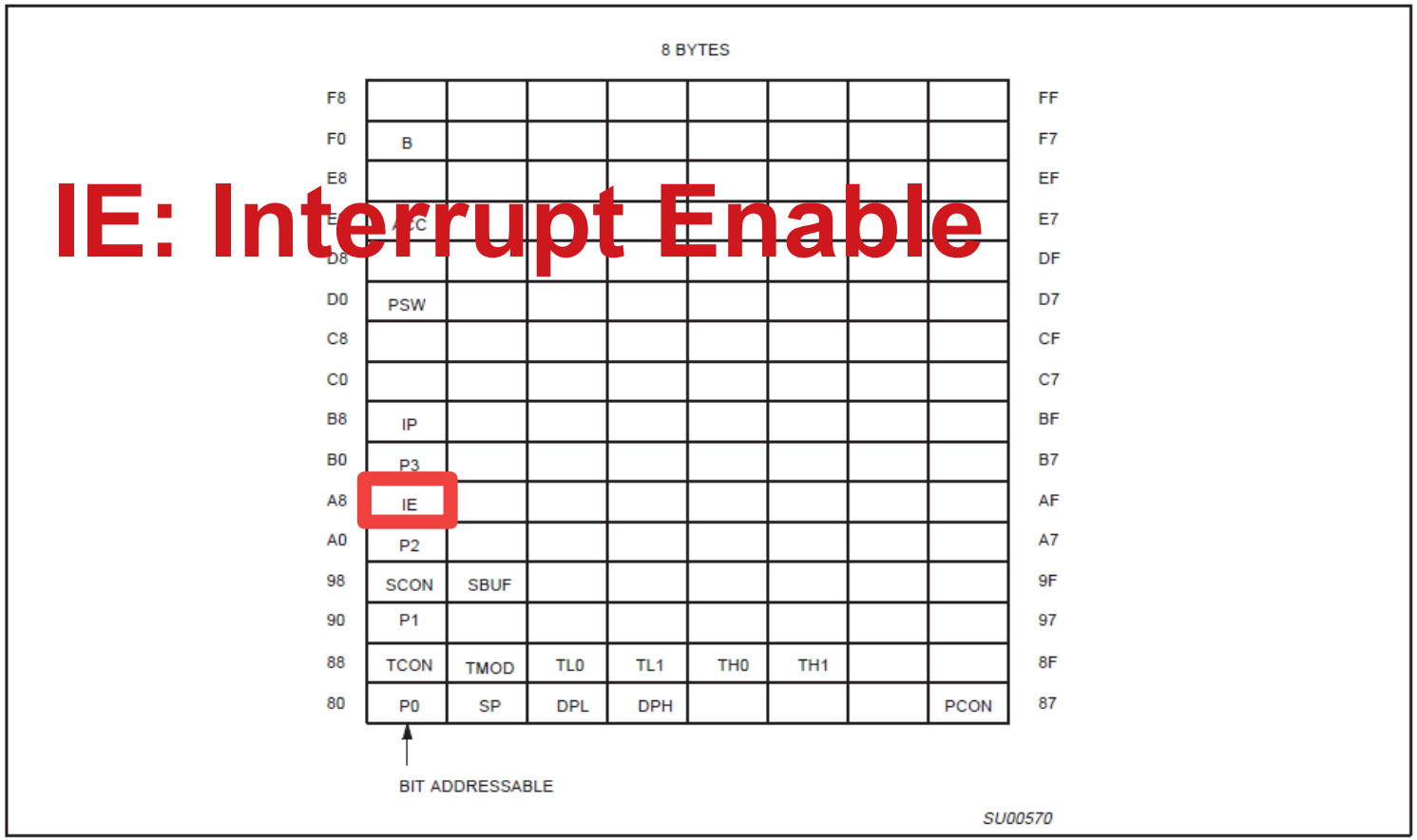


Figure 4. SFR Memory Map

80c51 - [SFR] IE: Interrupt Enable

Zer da interrupzio bat?

80c51 - [SFR] IE: Interrupt Enable

Programa nagusia ejekutatzen utzi, eta beste errutina ejekutatzea

Programa nagusia ejekutatzen utzi aurretik, dagoen errutina ejekutatzen bukatu behar

“Estimulo” batek esan behar dio mikro-kontroladoreari, programa nagusia ejekutatzen uzteko

80c51 - [SFR] IE: Interrupt Enable

IE. Interrupt Enable Register

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Not implemented, reserved for future use.*
—	IE.5	Not implemented, reserved for future use.*
ES	IE.4	Enable or disable the serial port interrupt.
ET1	IE.3	Enable or disable the Timer 1 overflow interrupt.
EX1	IE.2	Enable or disable External Interrupt 1.
ET0	IE.1	Enable or disable the Timer 0 overflow interrupt.
EX0	IE.0	Enable or disable External Interrupt 0.

* User software should not write 1s to reserved bits. These bits may be used in future 80C51 products to invoke new features.

80c51 - [SFR] IE: Interrupt Enable

IE: Interrupt Enable

EA: Interrupt-ak egoteko aukera egotea

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

IE: Interrupt Enable

EA: Interrupt-ak egoteko aukera egotea

ETx: Timer-ak balio jakin bat hartzerakoan interrupzioan sartu

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

IE: Interrupt Enable

EA: Interrupt-ak egoteko aukera egotea

ETx: Timer-ak balio jakin bat hartzerakoan interrupzioan sartu

EXx: kanpotik datorren bit bat aktibatzerakoan interrupzioan sartu

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

IE: Interrupt Enable

EA: Interrupt-ak egoteko aukera egotea

ETx: Timer-ak balio jakin bat hartzerakoan interrupzioan sartu

EXx: kanpotik datorren bit bat aktibatzerakoan interrupzioan sartu. ‘1’ denean edo transizioarekin definitu

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

IE: Interrupt Enable

EA: Interrupt-ak egoteko aukera egotea

ETx: Timer-ak balio jakin bat hartzerakoan interrupzioan sartu

EXx: kanpotik datorren bit bat aktibatzerakoan interrupzioan sartu. ‘1’ denean edo transizioarekin definitu

ES: serie portutik trama bat datorrenean interrupzioan sartu

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - Special Function Register

IE. Interrupt Enable Register

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Not implemented, reserved for future use.*
—	IE.5	Not implemented, reserved for future use.*
ES	IE.4	Enable or disable the serial port interrupt.
ET1	IE.3	Enable or disable the Timer 1 overflow interrupt.
EX1	IE.2	Enable or disable External Interrupt 1.
ET0	IE.1	Enable or disable the Timer 0 overflow interrupt.
EX0	IE.0	Enable or disable External Interrupt 0.

* User software should not write 1s to reserved bits. These bits may be used in future 80C51 products to invoke new features.

```
SETB    EA
CLR     EA
MOV     IE,#80H
```

80c51 - [SFR] IE: Interrupt Enable

IE: Interrupt Enable

INTERRUPTS:

To use any of the interrupts in the 80C51 Family, the following three steps must be taken.

1. **Set the EA (enable all) bit in the IE register to 1.**
2. **Set the corresponding individual interrupt enable bit in the IE register to 1.**
3. **Begin the interrupt service routine at the corresponding Vector Address of that interrupt. See Table below.**

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

IE: Interrupt Enable

INTERRUPTS:

To use any of the interrupts in the 80C51 Family, the following three steps must be taken.

1. **Set the EA (enable all) bit in the IE register to 1.**
2. **Set the corresponding individual interrupt enable bit in the IE register to 1.**
3. **Begin the interrupt service routine at the corresponding Vector Address of that interrupt. See Table below.**

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

IE: Interrupt Enable

INTERRUPTS:

To use any of the interrupts in the 80C51 Family, the following three steps must be taken.

1. **Set the EA (enable all) bit in the IE register to 1.**
2. **Set the corresponding individual interrupt enable bit in the IE register to 1.**
3. **Begin the interrupt service routine at the corresponding Vector Address of that interrupt. See Table below.**

INTERRUPT SOURCE	VECTOR ADDRESS
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI & TI	0023H

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

Aldi berean ematen badira, zelan dakigu zeinek daukan prioritate gehiago?

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

Aldi berean ematen badira, zelan dakigu zeinek daukan prioritate gehiago?

IP: INTERRUPT PRIORITY REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is 1 the corresponding interrupt has a higher priority.

–	–	–	PS	PT1	PX1	PT0	PX0

–	IP.7	Not implemented, reserved for future use.*
–	IP.6	Not implemented, reserved for future use.*
–	IP.5	Not implemented, reserved for future use.*
PS	IP.4	Defines the Serial Port interrupt priority level.
PT1	IP.3	Defines the Timer 1 interrupt priority level.
PX1	IP.2	Defines External Interrupt 1 priority level.
PT0	IP.1	Defines the Timer 0 interrupt priority level.
PX0	IP.0	Defines the External Interrupt 0 priority level.

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

Aldi berean ematen badira, zelan dakigu zeinek daukan prioritate gehiago?

IP: INTERRUPT PRIORITY REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is 1 the corresponding interrupt has a higher priority.

–	–	–	PS	PT1	PX1	PT0	PX0

–	IP.7	Not implemented, reserved for future use.*
–	IP.6	Not implemented, reserved for future use.*
–	IP.5	Not implemented, reserved for future use.*
PS	IP.4	Defines the Serial Port interrupt priority level.
PT1	IP.3	Defines the Timer 1 interrupt priority level.
PX1	IP.2	Defines External Interrupt 1 priority level.
PT0	IP.1	Defines the Timer 0 interrupt priority level.
PX0	IP.0	Defines the External Interrupt 0 priority level.

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

Aldi berean ematen badira, zelan dakigu zeinek daukan prioritate gehiago?

PRIORITY WITHIN LEVEL:

Priority within level is only to resolve simultaneous requests of the same priority level.

From high to low, interrupt sources are listed below:

IE0
TF0
IE1
TF1
RI or TI

IP: INTERRUPT PRIORITY REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is 1 the corresponding interrupt has a higher priority.

–	–	–	PS	PT1	PX1	PT0	PX0

IE: INTERRUPT ENABLE REGISTER. BIT ADDRESSABLE.

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	–	–	ES	ET1	EX1	ET0	EX0

80c51 - [SFR] IE: Interrupt Enable

IE-ko eta IP-ko kasu hauetan, ze interrupzio ejekutatuko litzateke? (X0, X1, T0, T1, S)

IE	IP	Interrupt.	Ejekutatu?
40H	00H	T0,X0	
80H	00H	T1,T0	
91H	11H	S,X0	
9EH	01H	S,X0	
9FH	10H	S,T0	
7FH	05H	X1,X0	
97H	0AH	T1,T0	
9FH	08H	T1,T0	

EA	–	–	ES	ET1	EX1	ET0	EX0

–	–	–	PS	PT1	PX1	PT0	PX0

80c51 - Special Function Register

ACC: Akumuladorea, eragiketa aritmetikoak egiteko

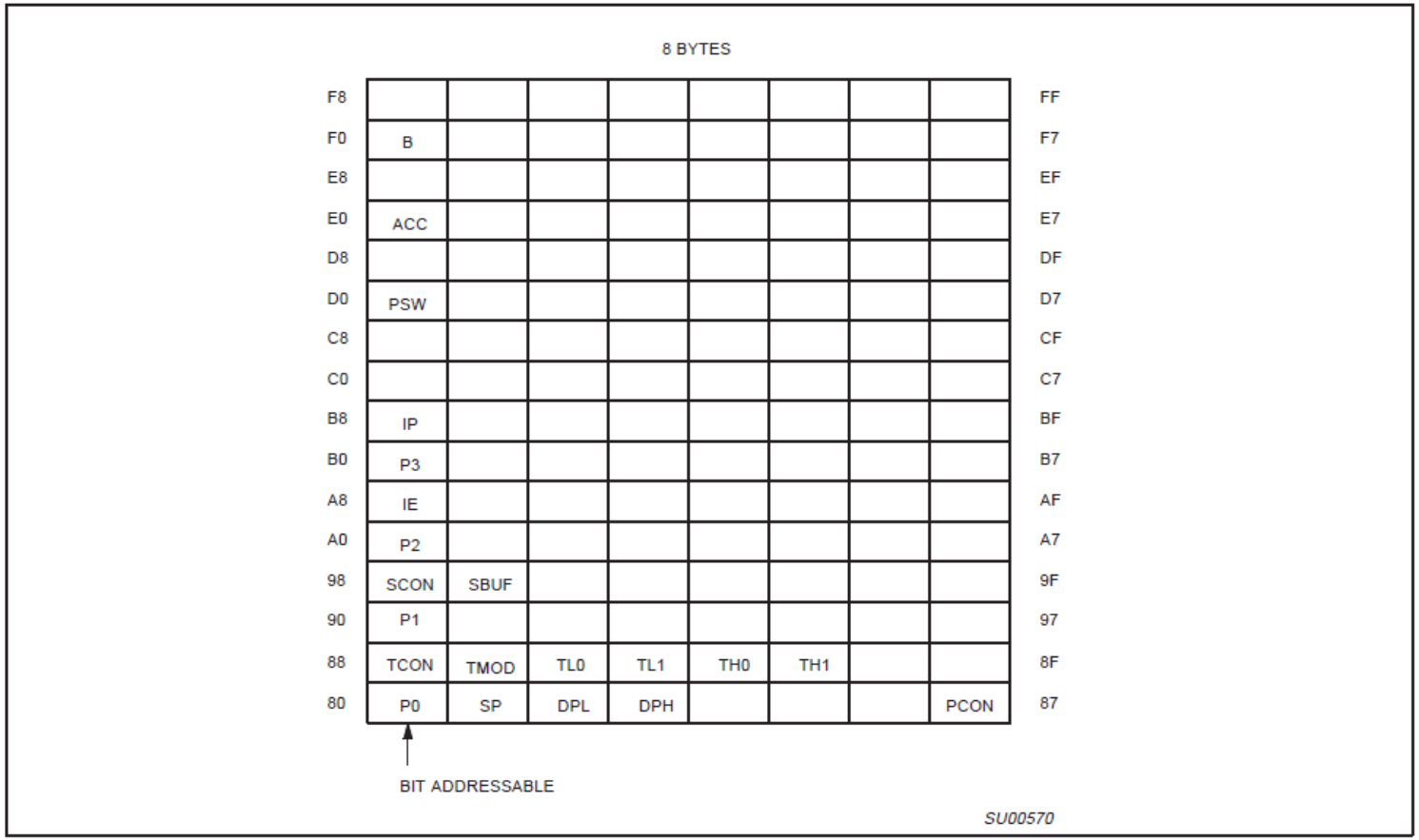
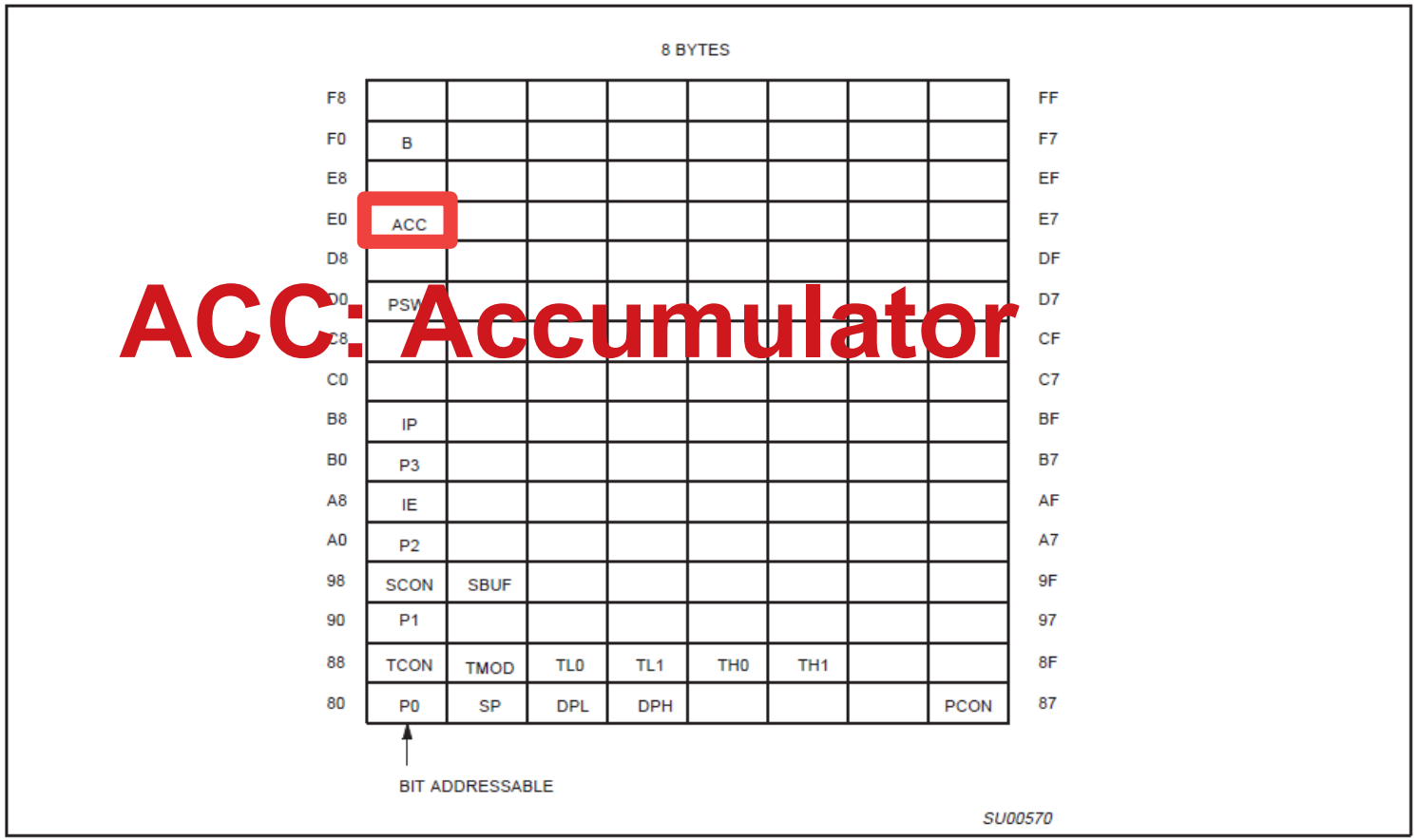


Figure 4. SFR Memory Map

80c51 - Special Function Register

ACC: Akumuladorea, eragiketa aritmetikoak egiteko



ACC: Accumulator

Figure 4. SFR Memory Map

80c51 - [SFR] ACC: Accumulator

ACC: Akumuladorea, eragiketa aritmetikoak egiteko

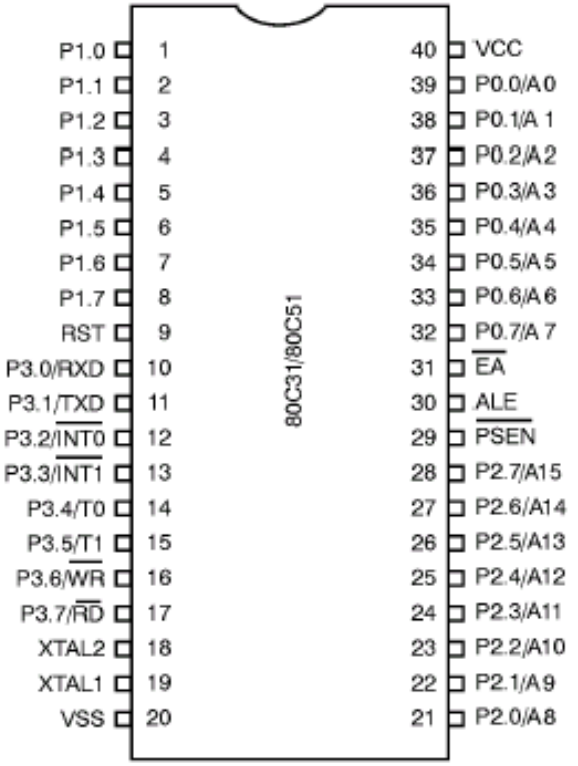
8 biteko aldagaia: A

Eragiketan parte hartu; bertan emaitza gordetzea posible

MOV (A, #00H), ADD, ADDC, SUBB, etc. agindu tipikoak

80c51 - Ports

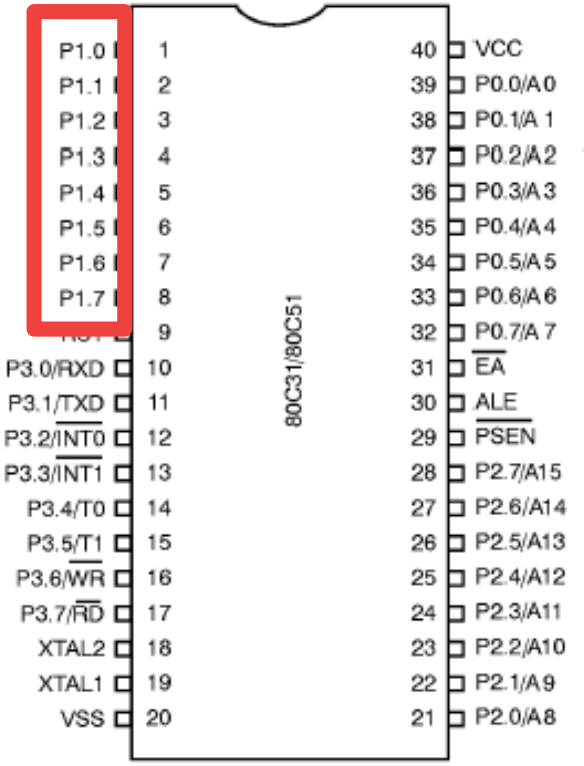
Ports: Kanpotik byte bateko aldagaiak hartzeko pinak



80c51 - Ports

Px aldagai bezala erabili instrukzioekin (MOV, ADD, etc.)

P0..P3. Batzuek bi funtzionalitate, horregatik P1 portua erabili



80c51 - Addressing

Helbideraketa zuzena: MOV A,40H. 40H helbideko datua A-ra.

Helbideraketa ez zuzena: MOV A,#40H. #40H datua A-ra.

Registroak: MOV A,R0. R0-ko datua A-ra.

Registro ez-zuzenak: MOV A,@R0. R0-k adierazten duen helbideko datua A-ra.

80c51 - [SFR] ACC: Accumulator

Acc erabiliz, egin ondorengo ejekuzioak

1.- Bank3-ko R3 posizioan, P1 balioa gorde nahi da. Acc + R3 (Bank3) egin eta akumuladorean gorde

2.- Bank1-ko R0 posizioan, 71H balioa gorde nahi da. Acc + R0.k apuntatzen duen helbideko datua (Bank1) egin eta akumuladorean gorde

3.- 50H helbidean R0 (Bank0) datua sartu. Akumuladorean R0-k apuntatzen duen helbideko datua sartu. Akumuladorean #80H balioko datua gehitu (ADD).

HELBURUAK

80c51 familia ezagutzea

Memorien banaketa ulertzea

eman ta zabal zazu

Universidad del País Vasco
Euskal Herriko Unibertsitatea

BILBOKO INGENIARITZA ESKOLA
ESCUELA DE INGENIERÍA DE BILBAO

Teknologia Elektronikoa Saila

KONPUTAGAILUEN ARKITEKTURA
80c51 mikro-kontroladorea

Kudeaketa eta Informazio Sistemen Informatikaren Ingenieritzako Graduaren 3. maila

Irakaslea: Alain Sanchez
(alain.sanchez@ehu.eus)

2019-2020, 1. lauhilabetea