eman ta zabal zazu

Universidad del País Vasco
Euskal Herriko Unibertsitatea

BILBOKO INGENIARITZA ESKOLA
ESCUELA DE INGENIERÍA DE BILBAO

Teknologia Elektronikoa Saila

KONPUTAGAILUEN ARKITEKTURA
80c552 - PWM

Kudeaketa eta Informazio Sistemen Informatikaren Ingenieritzako Graduaren 3. maila

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2019-2020, 1. lauhilabetea

HELBURUAK

Irteerako aldagai analogikoekin zelan lan egin ulertzea

80c552-aren PWM-a zelan konfiguratzen den ikastea

PWM

Ze aldagai mota egon daitezke? Zer da PWM bat?

PWM

Ze aldagai mota egon daitezke? Zer da PWM bat?

Zelan mugitzen dira DC motorrak?

PWM

Ze aldagai mota egon daitezke? Zer da PWM bat?

Zelan mugitzen dira DC motorrak?

Anplitudean ze balioraino atera dezakegu tentsioa?

PWM

PWM: Pluse Width Modulation. Irteerako periodo batetan nahi den batazbesteko tentsioa jarri.

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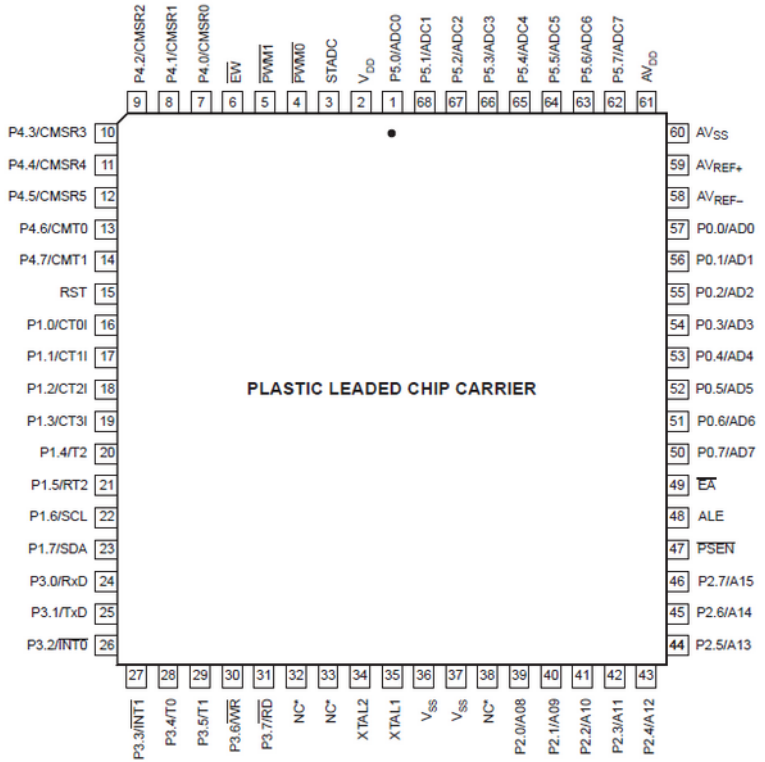
PWM0 eta PWM1 portuak erabili.



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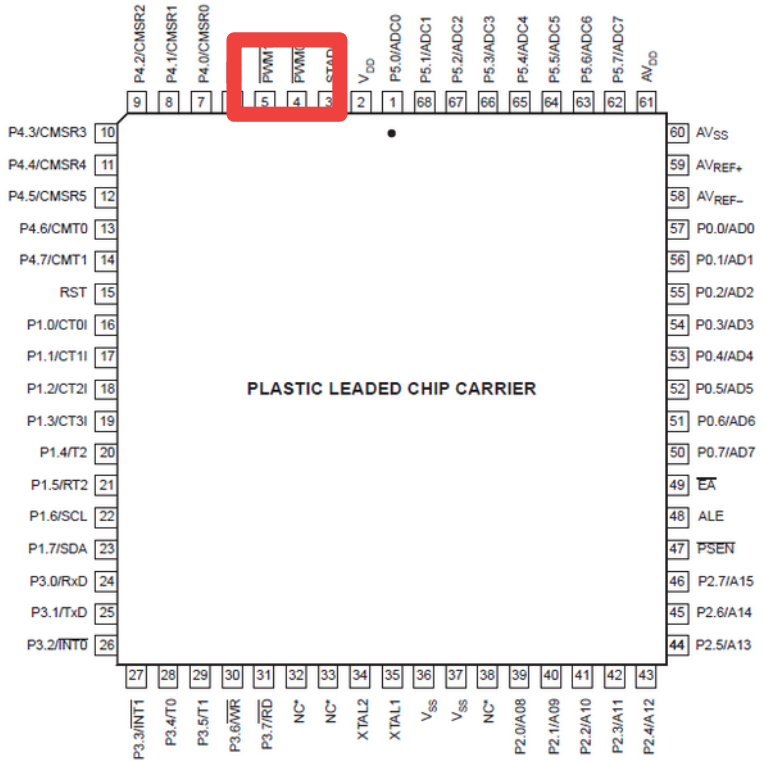

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PWM0 eta PWM1 portuak erabili.

Nahi den bataz besteko tentsioa lortu.

PWM

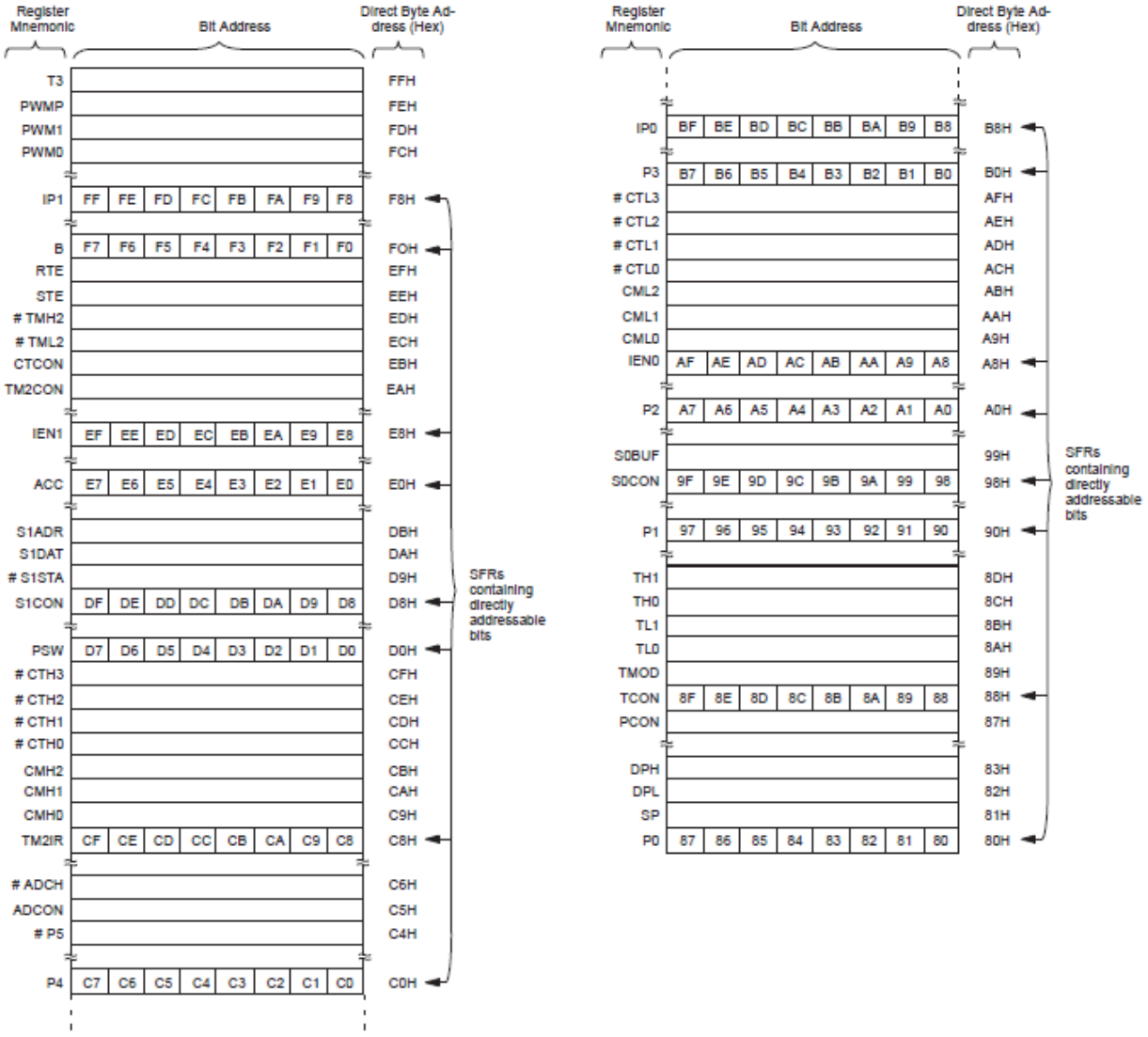
PWM: Pluse Width Modulation. Irteerako periodo batetan nahi den batazbesteko tentsioa jarri.

PWM0 eta PWM1 portuak erabili.

Nahi den bataz besteko tentsioa lortu.

Batzutan behe-pasa iragazki (filtro) bat jartzen da motorrera konektatzeko.

PWM


Register Mnemonic
Bit Address
Direct Byte Address (Hex)
T3 FFH
PWMP FEH
PWM1 FDH
PWM0 FCH
IP1 FF FE FD FC FB FA F9 F8 F8H
B F7 F6 F5 F4 F3 F2 F1 F0 F0H
RTE EFH
STE EEH
TMH2 EDH
TML2 ECH
CTCON EBH
TM2CON EAH
IEN1 EF EE ED EC EB EA E9 E8 E8H
ACC E7 E6 E5 E4 E3 E2 E1 E0 E0H
S1ADR DBH
S1DAT DAH
S1STA D9H
S1CON DF DE DD DC DB DA D9 D8 D8H
PSW D7 D6 D5 D4 D3 D2 D1 D0 D0H
CTH3 CFH
CTH2 CEH
CTH1 CDH
CTH0 CCH
CMH2 CBH
CMH1 CAH
CMH0 C9H
TM2IR CF CE CD CC CB CA C9 C8 C8H
ADCH C6H
ADCON C5H
P5 C4H
P4 C7 C6 C5 C4 C3 C2 C1 C0 C0H
SFRs containing directly addressable bits
Register Mnemonic
Bit Address
Direct Byte Address (Hex)
IP0 BF BE BD BC BB BA B9 B8 B8H
P3 B7 B6 B5 B4 B3 B2 B1 B0 B0H
CTL3 AFH
CTL2 AEH
CTL1 ADH
CTL0 ACH
CML2 ABH
CML1 AAH
CML0 A9H
IEN0 AF AE AD AC AB AA A9 A8 A8H
P2 A7 A6 A5 A4 A3 A2 A1 A0 A0H
SDBUF 99H
SDCON 9F 9E 9D 9C 9B 9A 99 98 98H
P1 97 96 95 94 93 92 91 90 90H
TH1 8DH
TH0 8CH
TL1 8BH
TL0 8AH
TMOD 89H
TCON 8F 8E 8D 8C 8B 8A 89 88 88H
PCON 87H
DPH 83H
DPL 82H
SP 81H
P0 87 86 85 84 83 82 81 80 80H
SFRs containing directly addressable bits

PWM


Register Mnemonic
Bit Address
Direct Byte Address (Hex)
PWMP FEH
PWM1 FDH
PWM0 FCH
IP1 FF FE FD FC FB FA F9 F8 F8H
B F7 F6 F5 F4 F3 F2 F1 F0 F0H
RTE EFH
STE EEH
TMH2 EDH
TML2 ECH
CTCON EBH
TM2CON EAH
IEN1 EF EE ED EC EB EA E9 E8 E8H
ACC E7 E6 E5 E4 E3 E2 E1 E0 E0H
S1ADR DBH
S1DAT DAH
S1STA D9H
S1CON DF DE DD DC DB DA D9 D8 D8H
PSW D7 D6 D5 D4 D3 D2 D1 D0 D0H
CTH3 CFH
CTH2 CEH
CTH1 CDH
CTH0 CCH
CMH2 CBH
CMH1 CAH
CMH0 C9H
TM2IR CF CE CD CC CB CA C9 C8 C8H
ADCH C6H
ADCON C5H
P5 C4H
P4 C7 C6 C5 C4 C3 C2 C1 C0 C0H
SFRs containing directly addressable bits
IP0 BF BE BD BC BB BA B9 B8 B8H
P3 B7 B6 B5 B4 B3 B2 B1 B0 B0H
CTL3 AFH
CTL2 AEH
CTL1 ADH
CTL0 ACH
CML2 ABH
CML1 AAH
CML0 A9H
IEN0 AF AE AD AC AB AA A9 A8 A8H
P2 A7 A6 A5 A4 A3 A2 A1 A0 A0H
SDBUF 99H
SDCON 9F 9E 9D 9C 9B 9A 99 98 98H
P1 97 96 95 94 93 92 91 90 90H
TH1 8DH
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TL1 8BH
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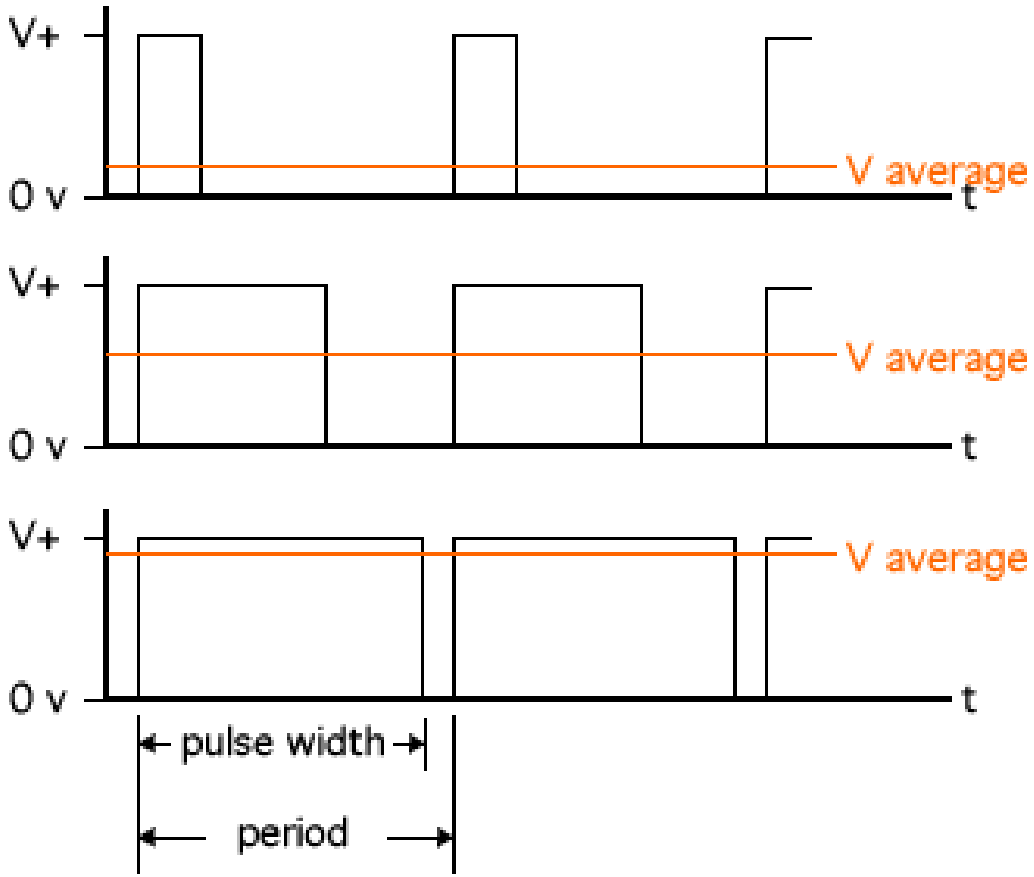
PCON 87H
DPH 83H
DPL 82H
SP 81H
P0 87 86 85 84 83 82 81 80 80H
SFRs containing directly addressable bits

PWM

Zer da PWM kontzeptua?



PWM

Pulse Width Modulated Outputs

The 8XC552 contains two pulse width modulated output channels (see Figure 33). These channels generate pulses of programmable length and interval. The repetition frequency is defined by an 8-bit prescaler PWMP, which supplies the clock for the counter. The prescaler and counter are common to both PWM channels. The 8-bit counter counts modulo 255, i.e., from 0 to 254 inclusive. The value of the 8-bit counter is compared to the contents of two registers: PWM0 and PWM1. Provided the contents of either of these registers is greater than the counter value, the corresponding $\overline{\text{PWM0}}$ or $\overline{\text{PWM1}}$ output is set LOW. If the contents of these registers are equal to, or less than the counter value, the output will be HIGH. The pulse-width-ratio is therefore defined by the contents of the registers PWM0 and PWM1. The pulse-width-ratio is in the range of 0 to 1 and may be programmed in increments of 1/255.

Buffered PWM outputs may be used to drive DC motors. The rotation speed of the motor would be proportional to the contents of PWMn. The PWM outputs may also be configured as a dual DAC. In this application, the PWM outputs must be integrated using conventional operational amplifier circuitry. If the resulting output voltages have to be accurate, external buffers with their own analog supply should be used to buffer the PWM outputs before they are integrated. The repetition frequency f_{PWM}, at the PWMn outputs is give by:

$$f_{PWM} = \frac{f_{OSC}}{2 \times (1 + PWMP) \times 255}$$

This gives a repetition frequency range of 123Hz to 31.4kHz (f_{OSC} = 16MHz). At fosc = 24MHz, the frequency range is 184Hz to 47.1Hz. By loading the PWM registers with either 00H or FFH, the PWM channels will output a constant HIGH or LOW level, respectively. Since the 8-bit counter counts modulo 255, it can never actually reach the value of the PWM registers when they are loaded with FFH.

When a compare register (PWM0 or PWM1) is loaded with a new value, the associated output is updated immediately. It does not have to wait until the end of the current counter period. Both $\overline{\text{PWMn}}$ output pins are driven by push-pull drivers. These pins are not used for any other purpose.

Prescaler frequency control register PWMP

PWMP (FEH)	7	6	5	4	3	2	1	0
	MSB							LSB

PWMP.0-7 Prescaler division factor = PWMP + 1.

Reading PWMP gives the current reload value. The actual count of the prescaler cannot be read.

PWM0 (FCH) PWM1 (FDH)	7	6	5	4	3	2	1	0
	MSB							LSB

PWM0/1.0-7} Low/high ratio of $\overline{\text{PWMn}}$ $= \frac{(PWMn)}{255 - (PWMn)}$

PWM

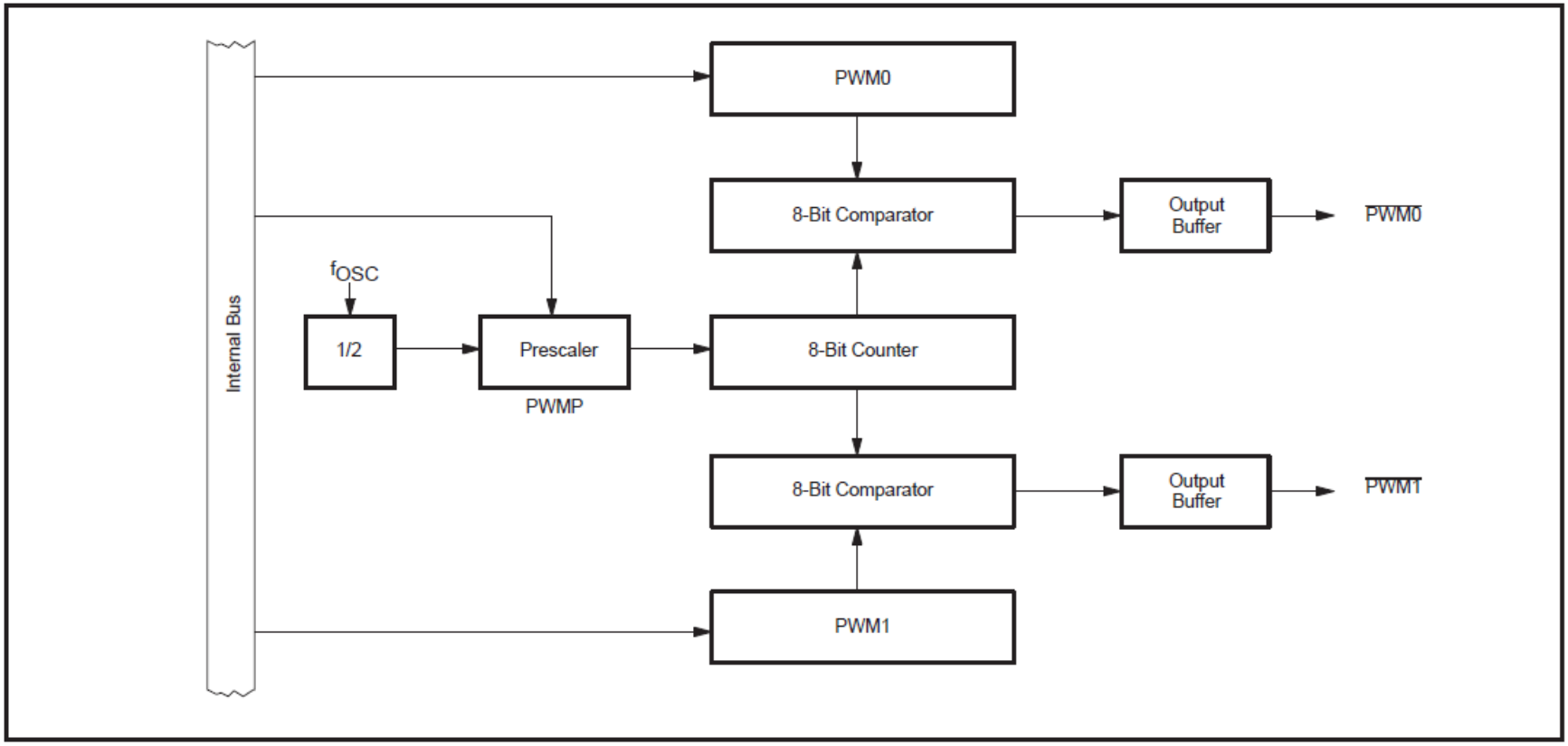


Figure 33. Functional Diagram of Pulse Width Modulated Outputs

PWM

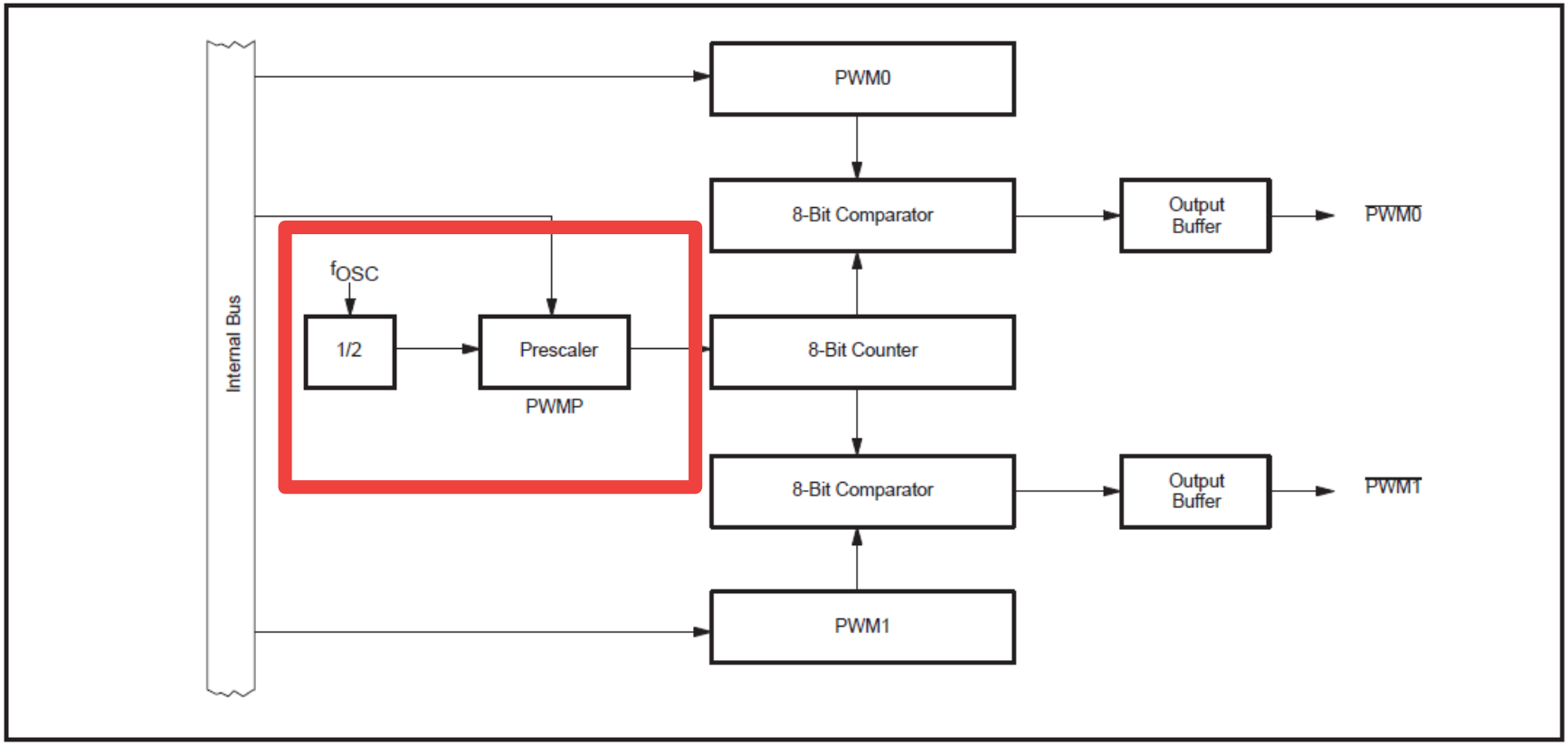


Figure 33. Functional Diagram of Pulse Width Modulated Outputs

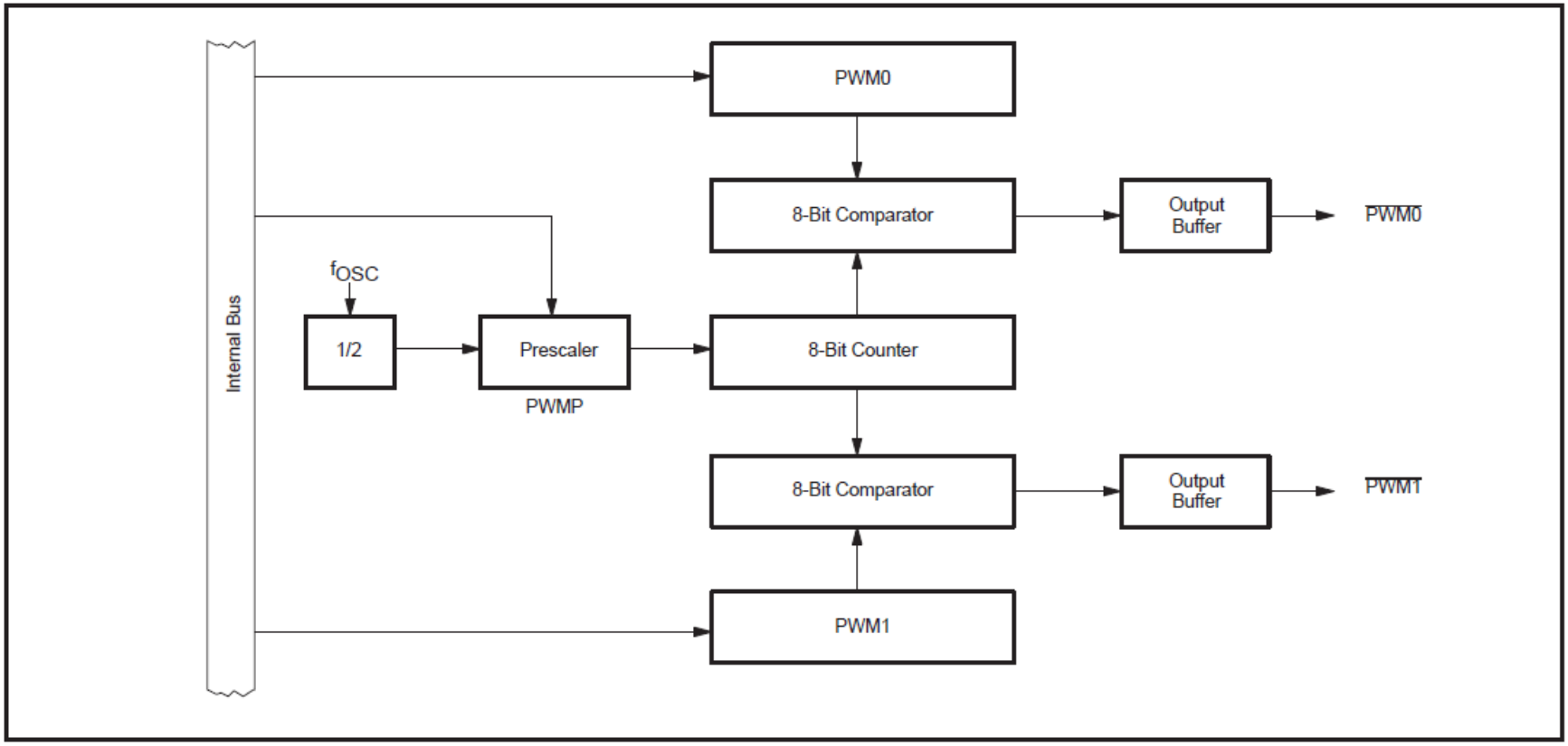
PWM

fPWM,counter = fclk/2/(1+PWMP)

fPWM,total = fclk/2/(1+PWMP)/255

$$f_{PWM} = \frac{f_{OSC}}{2 \times (1 + PWMP) \times 255}$$

PWM



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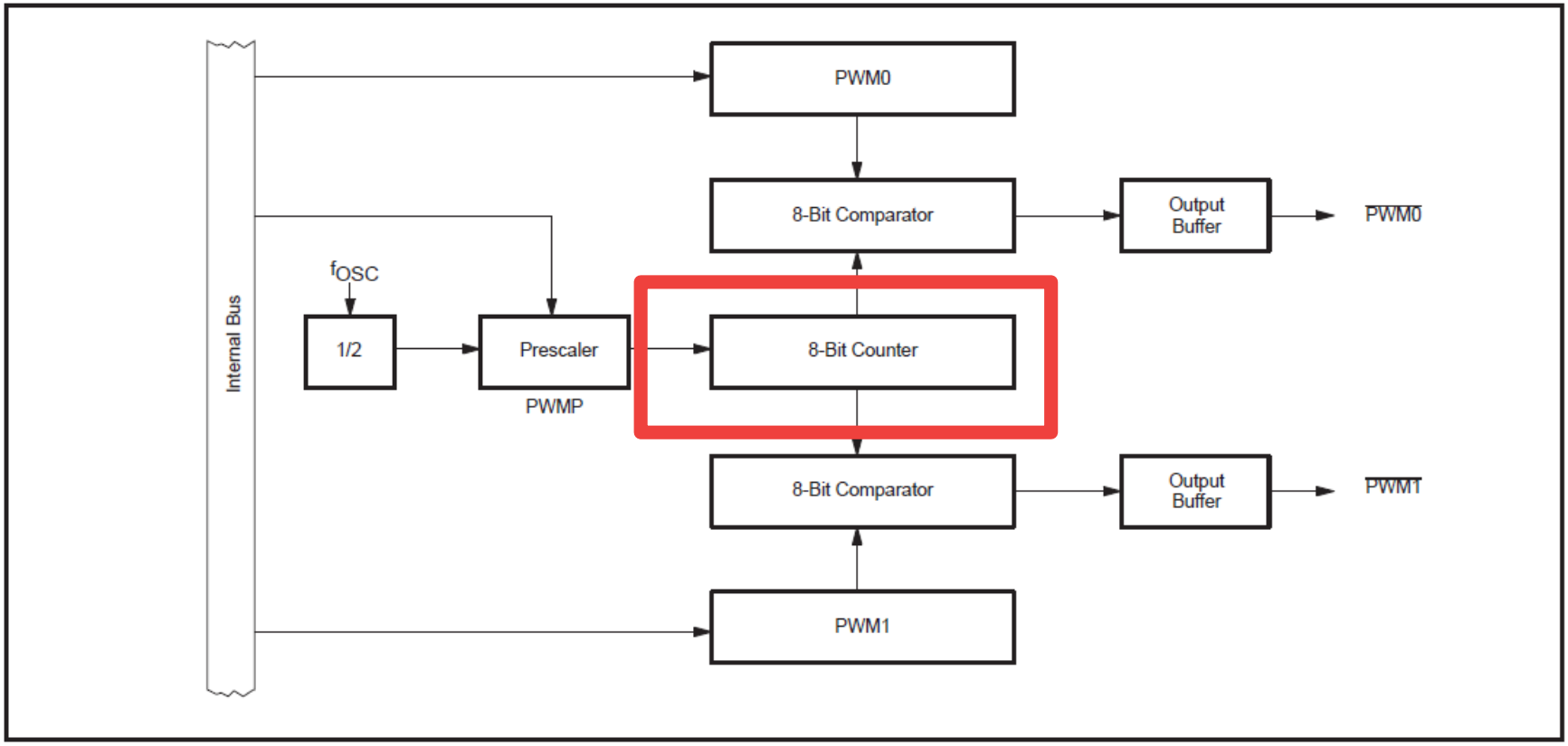
PWM



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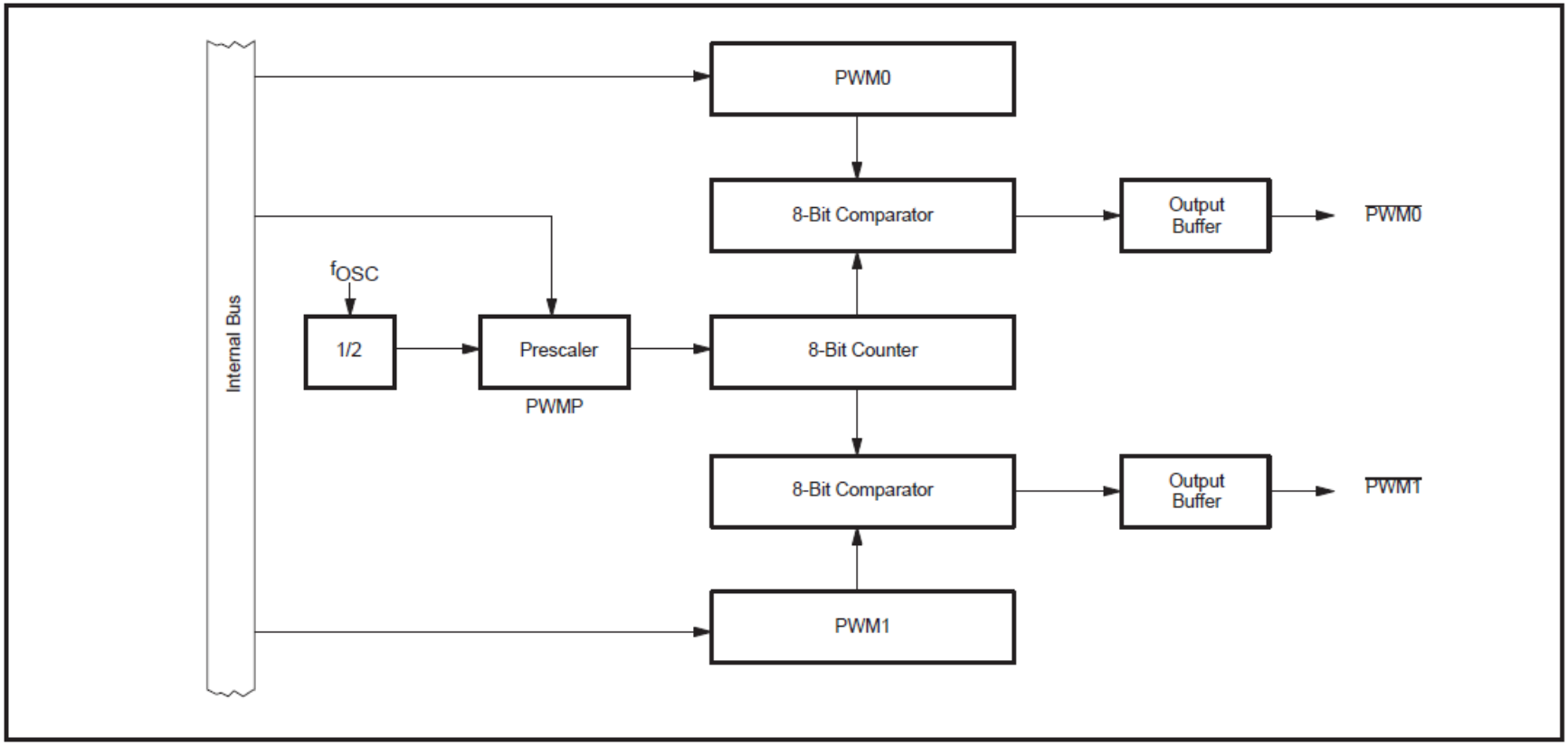
PWM

fPWM,counter = fclk/2/(1+PWMP)

fPWM,total = fclk/2/(1+PWMP)/255

Counter bat 0-tik 254-ra.

PWM



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PWM

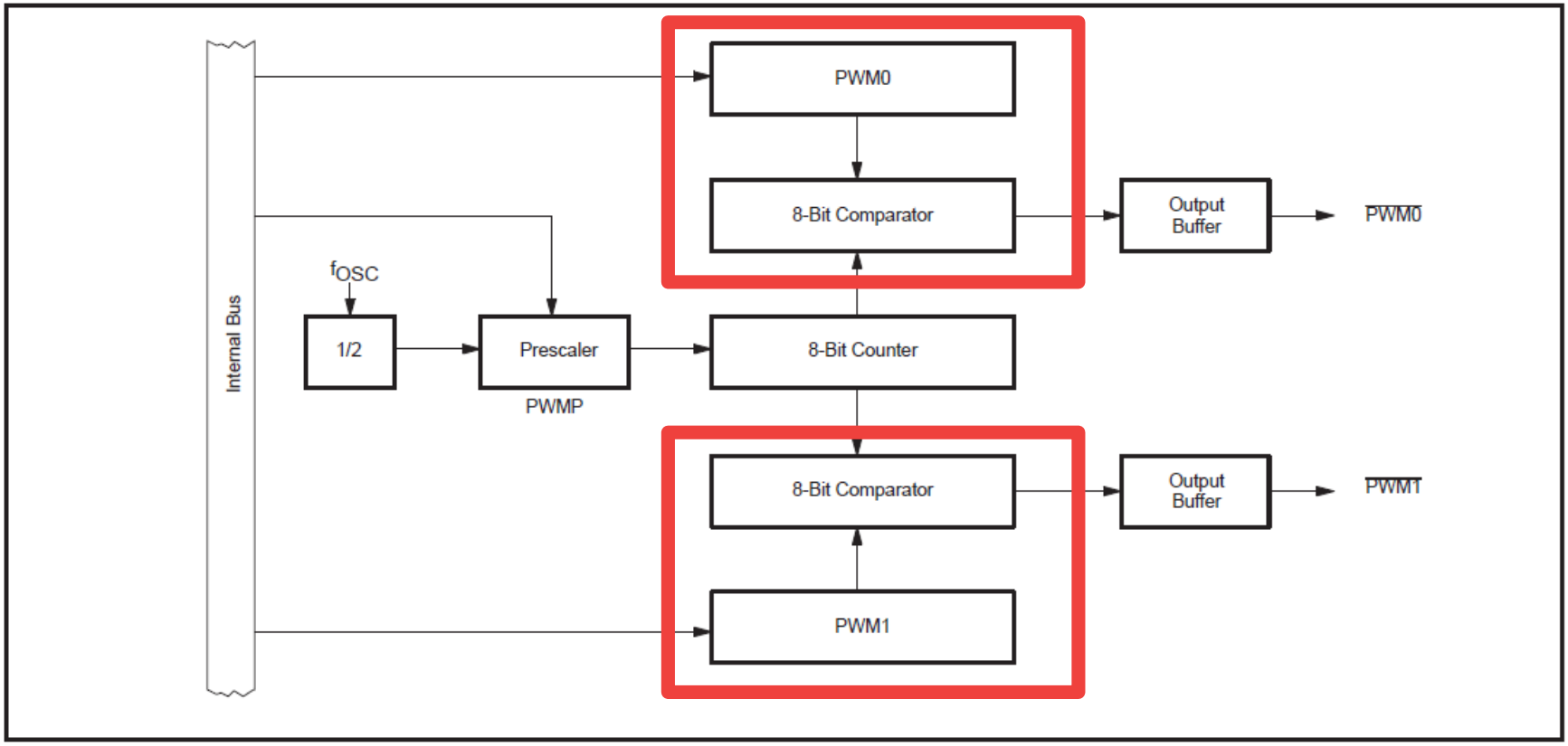


Figure 33. Functional Diagram of Pulse Width Modulated Outputs

PWM

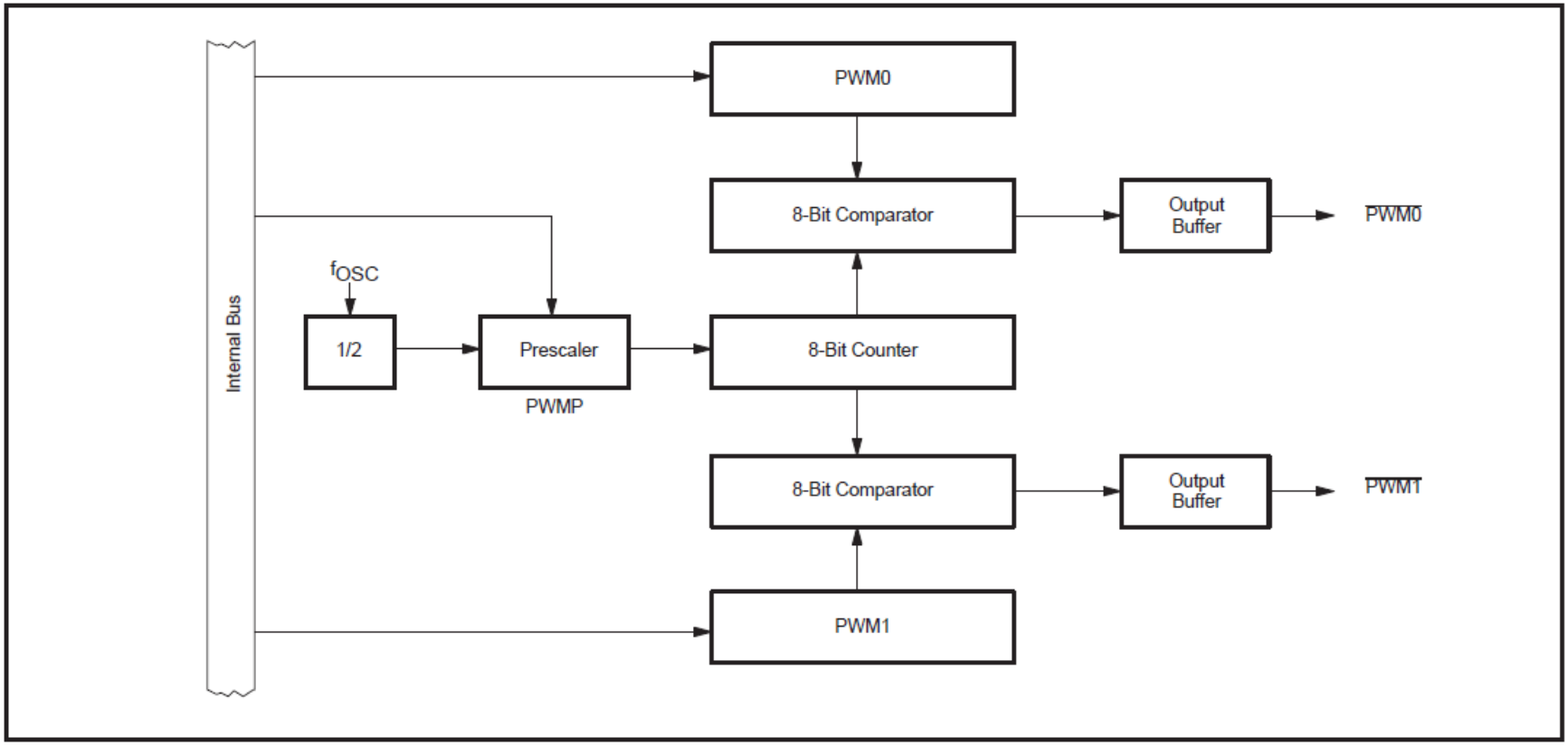
fPWM,counter = fclk/2/(1+PWMP)

fPWM,total = fclk/2/(1+PWMP)/255

Counter bat 0-tik 254-ra.

PWM0 eta PWM1-ekin konparatu Counter-a.

PWM



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PWM

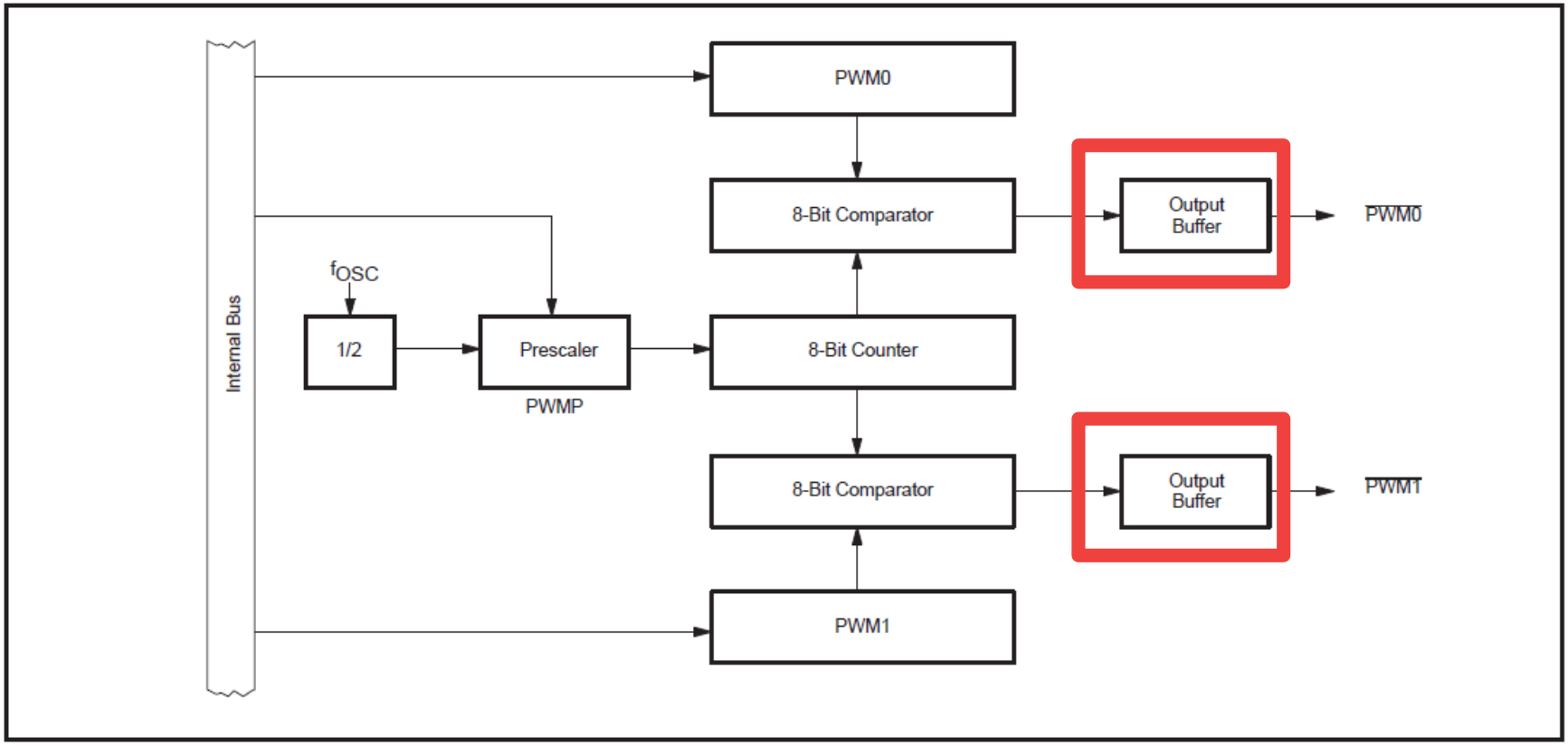

Figure 33. Functional Diagram of Pulse Width Modulated Outputs

PWM

fPWM,counter = fclk/2/(1+PWMP)

fPWM,total = fclk/2/(1+PWMP)/255

Counter bat 0-tik 254-ra.

PWM0 eta PWM1-ekin konparatu Counter-a.

PWMn > Counter → PWMn irteera LOW.
PWMn <= Counter → PWMn irteera HIGH.

PWM

fPWM,counter = fclk/2/(1+PWMP)

fPWM,total = fclk/2/(1+PWMP)/255

Counter bat 0-tik 254-ra.

PWM0 eta PWM1-ekin konparatu Counter-a.

PWMn > Counter → PWMn irteera LOW.
PWMn <= Counter → PWMn irteera HIGH.

PWMn = Round (255-(VPWM,ave/Vcc)*255)
VPWM,real = Vcc * (1-PWMn/255)

PWM

Zein frekuentziarekin eta zenbat clock-etan egongo da HIGH balioarekin PWM-a? Ze baliorekin konfiguratu beharko litzateke PWMx? (Vcc = 5V, fclk = 24MHz)

VPWM,ave	PWMP	fPWM	PWMx	VPWM,real
3V	0000H			
2.5V	0010H			
0.1V	1110H			
0.02V	1000H			
0.015V	0001H			
4.99V	0011H			
4V	1100H			
1.33V	1010H			

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