eman ta zabal zazu

Universidad del País Vasco
Euskal Herriko Unibertsitatea

BILBOKO INGENIARITZA ESKOLA
ESCUELA DE INGENIERÍA DE BILBAO

Teknologia Elektronikoa Saila

KONPUTAGAILUEN ARKITEKTURA
80c552 - Timer2

Kudeaketa eta Informazio Sistemen Informatikaren Ingenieritzako Graduaren 3. maila

Irakaslea: Alain Sanchez
(alain.sanchez@ehu.eus)

2019-2020, 1. lauhilabetea

HELBURUAK

Denbora handia kontatzeko Timer2 dagoela ezagutzea

80c552-aren Timer2-a zelan konfiguratzen den ikastea

Timer 2

Zein da arazorik nagusiena T0 eta T1ekin?

Timer 2

Zein da arazorik nagusiena T0 eta T1ekin?

Zergatik da interesgarria T2? Zer da timer 2-a?

Timer 2

Timer 2, 16 bit-eko kontagailu bat da. TMH2 eta TML2.

Timer 2

Timer 2, 16 bit-eko kontagailu bat da. TMH2 eta TML2.

Bakarrik goruntza kontatzen du.

Timer 2

Timer 2, 16 bit-eko kontagailu bat da. TMH2 eta TML2.

Bakarrik goruntza kontatzen du.

Ez dauka inizializaziorik.

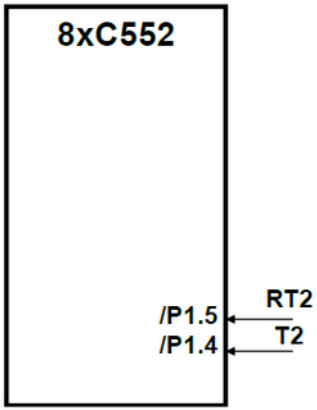
Timer 2

Timer 2, 16 bit-eko kontagailu bat da. TMH2 eta TML2.

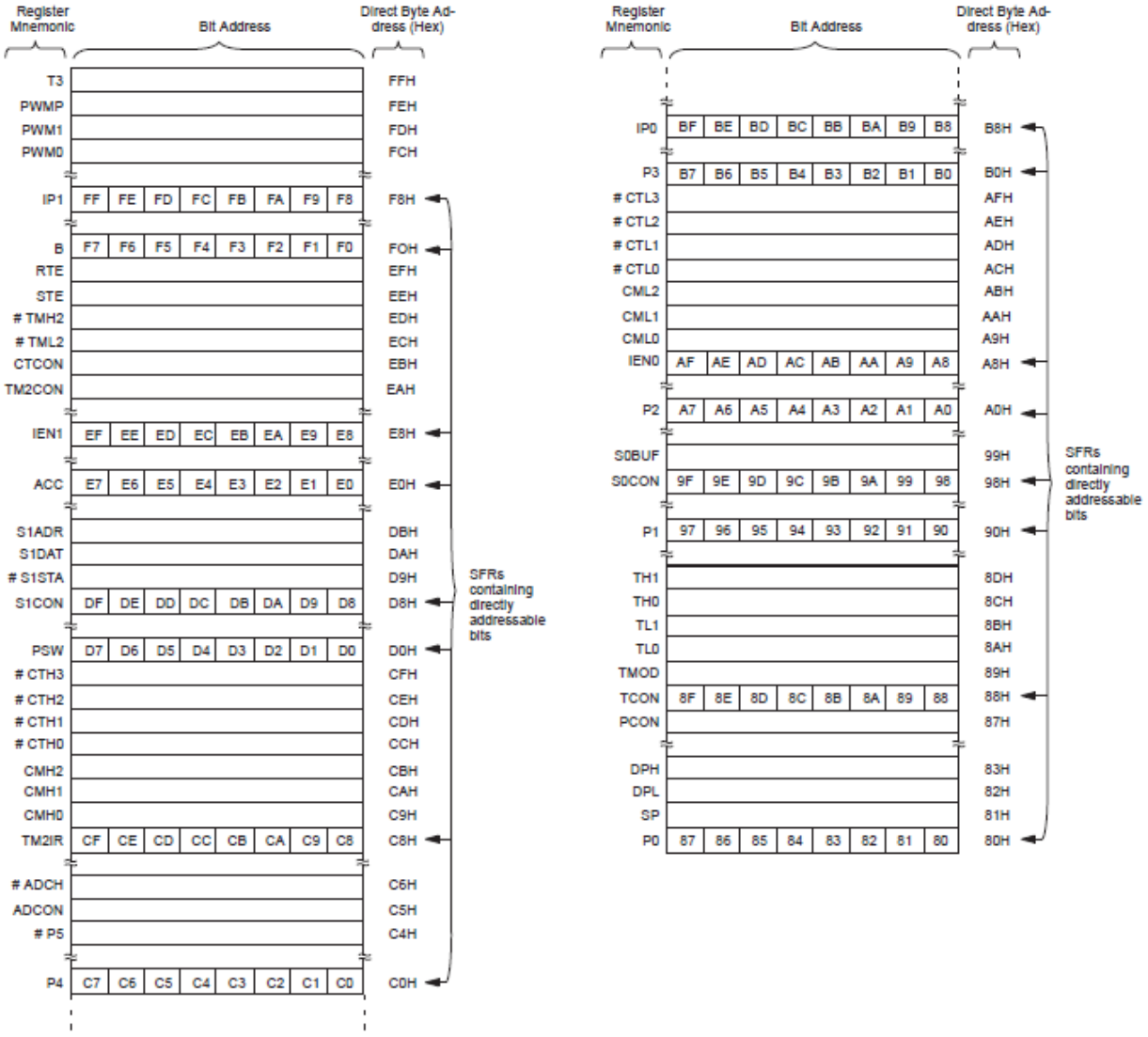
Bakarrik goruntza kontatzen du.

Ez dauka inizializaziorik.

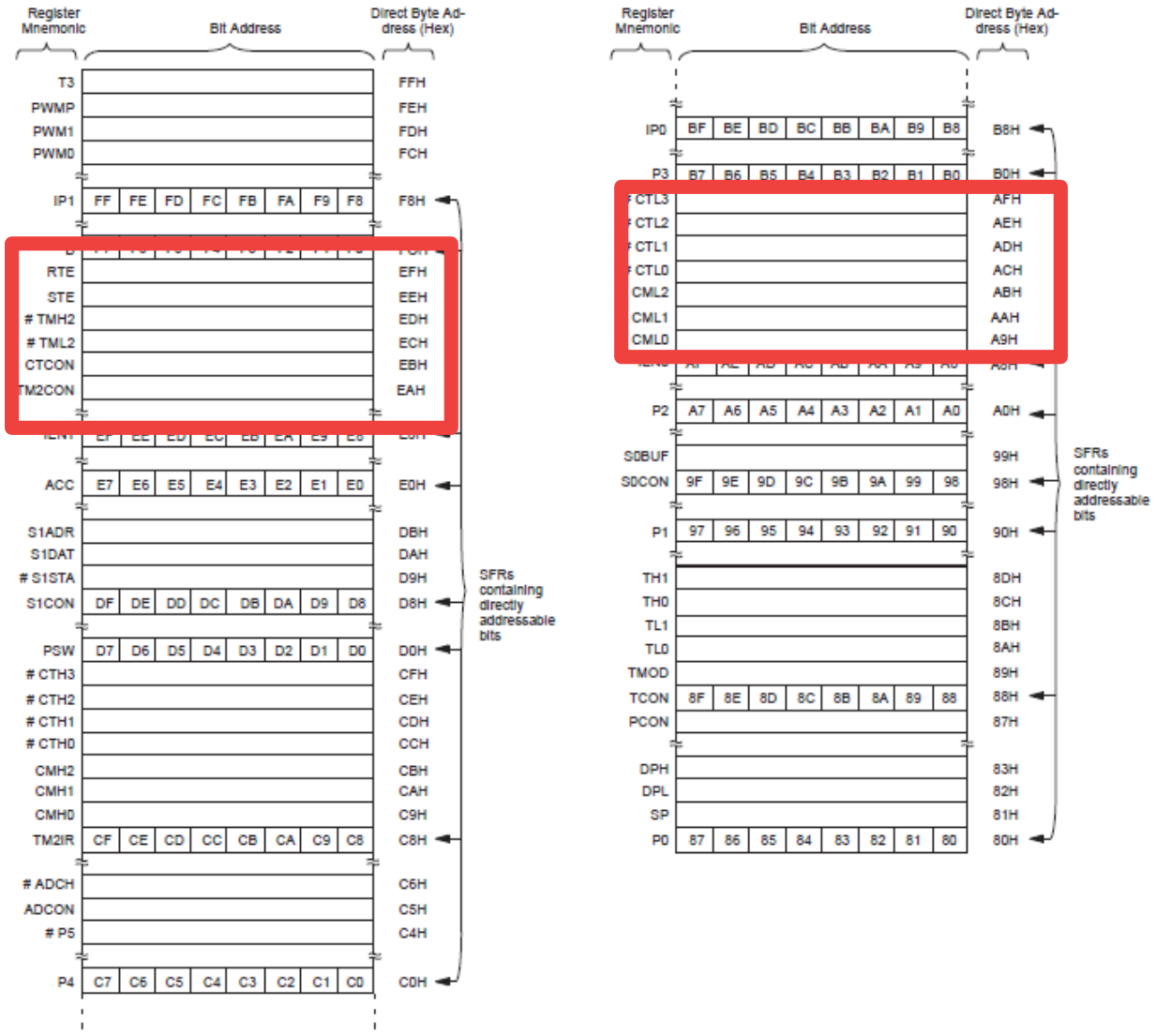
Reset bat dauka.



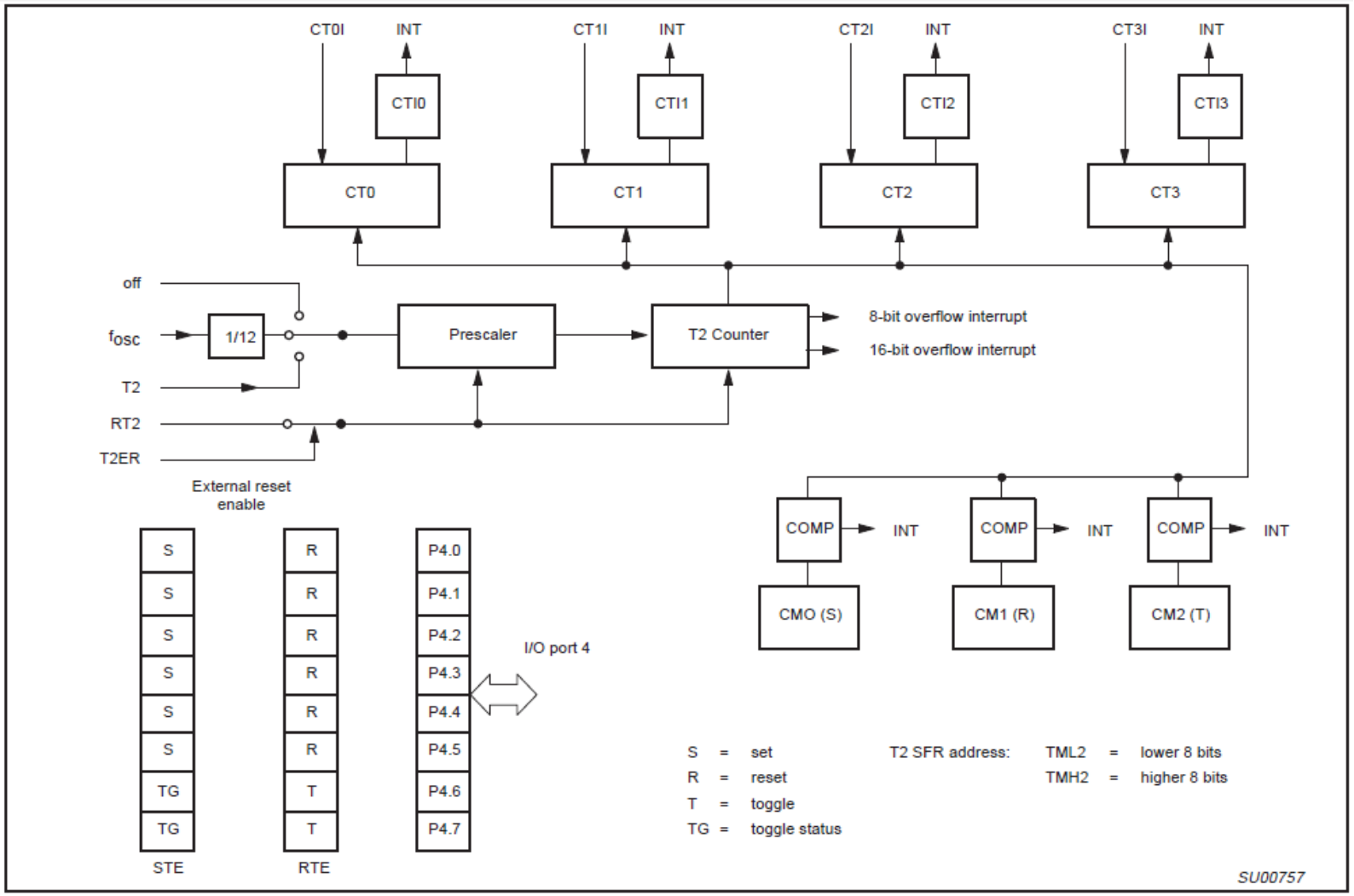
Timer 2


Register Mnemonic
Bit Address
Direct Byte Address (Hex)
T3 FFH
PWMP FEH
PWM1 FDH
PWM0 FCH
IP1 FF FE FD FC FB FA F9 F8 F8H
B F7 F6 F5 F4 F3 F2 F1 F0 F0H
RTE EFH
STE EEH
TMH2 EDH
TML2 ECH
CTCON EBH
TM2CON EAH
IEN1 EF EE ED EC EB EA E9 E8 E8H
ACC E7 E6 E5 E4 E3 E2 E1 E0 E0H
S1ADR DBH
S1DAT DAH
S1STA D9H
S1CON DF DE DD DC DB DA D9 D8 D8H
PSW D7 D6 D5 D4 D3 D2 D1 D0 D0H
CTH3 CFH
CTH2 CEH
CTH1 CDH
CTH0 CCH
CMH2 CBH
CMH1 CAH
CMH0 C9H
TM2IR CF CE CD CC CB CA C9 C8 C8H
ADCH C6H
ADCON C5H
P5 C4H
P4 C7 C6 C5 C4 C3 C2 C1 C0 C0H
SFRs containing directly addressable bits
Register Mnemonic
Bit Address
Direct Byte Address (Hex)
IP0 BF BE BD BC BB BA B9 B8 B8H
P3 B7 B6 B5 B4 B3 B2 B1 B0 B0H
CTL3 AFH
CTL2 AEH
CTL1 ADH
CTL0 ACH
CML2 ABH
CML1 AAH
CML0 A9H
IEN0 AF AE AD AC AB AA A9 A8 A8H
P2 A7 A6 A5 A4 A3 A2 A1 A0 A0H
SDBUF 99H
SDCON 9F 9E 9D 9C 9B 9A 99 98 98H
P1 97 96 95 94 93 92 91 90 90H
TH1 8DH
TH0 8CH
TL1 8BH
TL0 8AH
TMOD 89H
TCON 8F 8E 8D 8C 8B 8A 89 88 88H
PCON 87H
DPH 83H
DPL 82H
SP 81H
P0 87 86 85 84 83 82 81 80 80H
SFRs containing directly addressable bits

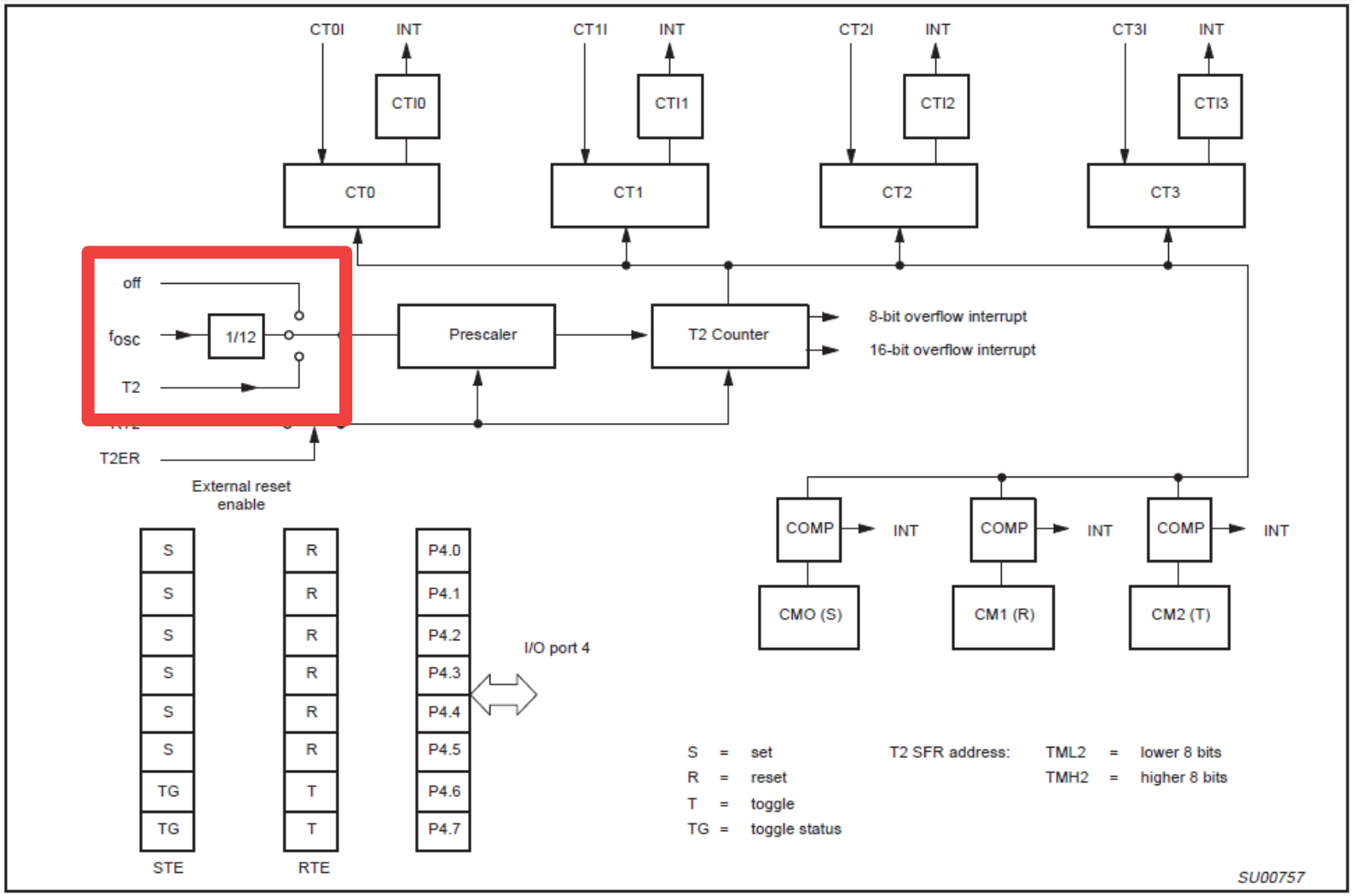
Timer 2


Register Mnemonic
Bit Address
Direct Byte Address (Hex)
T3 FFH
PWMP FEH
PWM1 FDH
PWM0 FCH
IP1 FF FE FD FC FB FA F9 F8 F8H
RTE EFH
STE EEH
TMH2 EDH
TML2 ECH
CTCON EBH
TM2CON EAH
ACC E7 E6 E5 E4 E3 E2 E1 E0 E0H
S1ADR DBH
S1DAT DAH
S1STA D9H
S1CON DF DE DD DC DB DA D9 D8 D8H
PSW D7 D6 D5 D4 D3 D2 D1 D0 D0H
CTH3 CFH
CTH2 CEH
CTH1 CDH
CTH0 CCH
CMH2 CBH
CMH1 CAH
CMH0 C9H
TM2IR CF CE CD CC CB CA C9 C8 C8H
ADCH C6H
ADCON C5H
P5 C4H
P4 C7 C6 C5 C4 C3 C2 C1 C0 C0H
SFRs containing directly addressable bits
IP0 BF BE BD BC BB BA B9 B8 B8H
P3 B7 B6 B5 B4 B3 B2 B1 B0 B0H
CTL3 AFH
CTL2 AEH
CTL1 ADH
CTL0 ACH
CML2 ABH
CML1 AAH
CML0 A9H
P2 A7 A6 A5 A4 A3 A2 A1 A0 A0H
S0BUF 99H
S0CON 9F 9E 9D 9C 9B 9A 99 98 98H
P1 97 96 95 94 93 92 91 90 90H
TH1 8DH
TH0 8CH
TL1 8BH
TL0 8AH
TMOD 89H
TCON 8F 8E 8D 8C 8B 8A 89 88 88H
PCON 87H
DPH 83H
DPL 82H
SP 81H
P0 87 86 85 84 83 82 81 80 80H
SFRs containing directly addressable bits

Timer 2


CT0I
INT
CTI0
CT0
CT1I
INT
CTI1
CT1
CT2I
INT
CTI2
CT2
CT3I
INT
CTI3
CT3
off
fosc
1/12
T2
RT2
T2ER
Prescaler
T2 Counter
8-bit overflow interrupt
16-bit overflow interrupt
External reset enable
COMP
INT
CMO (S)
CM1 (R)
CM2 (T)
S
R
P4.0
P4.1
P4.2
P4.3
P4.4
P4.5
P4.6
P4.7
I/O port 4
TG
T
STE
RTE
S = set
R = reset
T = toggle
TG = toggle status
T2 SFR address:
TML2 = lower 8 bits
TMH2 = higher 8 bits
SU00757

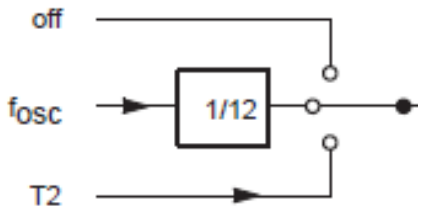
Timer 2


CT0I
INT
CT1I
INT
CT2I
INT
CT3I
INT
CTI0
CTI1
CTI2
CTI3
CT0
CT1
CT2
CT3
off
fosc
1/12
T2
T2ER
External reset enable
Prescaler
T2 Counter
8-bit overflow interrupt
16-bit overflow interrupt
COMP
INT
COMP
INT
COMP
INT
CMO (S)
CM1 (R)
CM2 (T)
S
S
S
S
S
S
TG
TG
STE
R
R
R
R
R
R
T
T
RTE
P4.0
P4.1
P4.2
P4.3
P4.4
P4.5
P4.6
P4.7
I/O port 4
S = set
R = reset
T = toggle
TG = toggle status
T2 SFR address:
TML2 = lower 8 bits
TMH2 = higher 8 bits
SU00757

Timer 2

Hiru timer/counter egoera posible: T2 (counter), fosc/12, off.

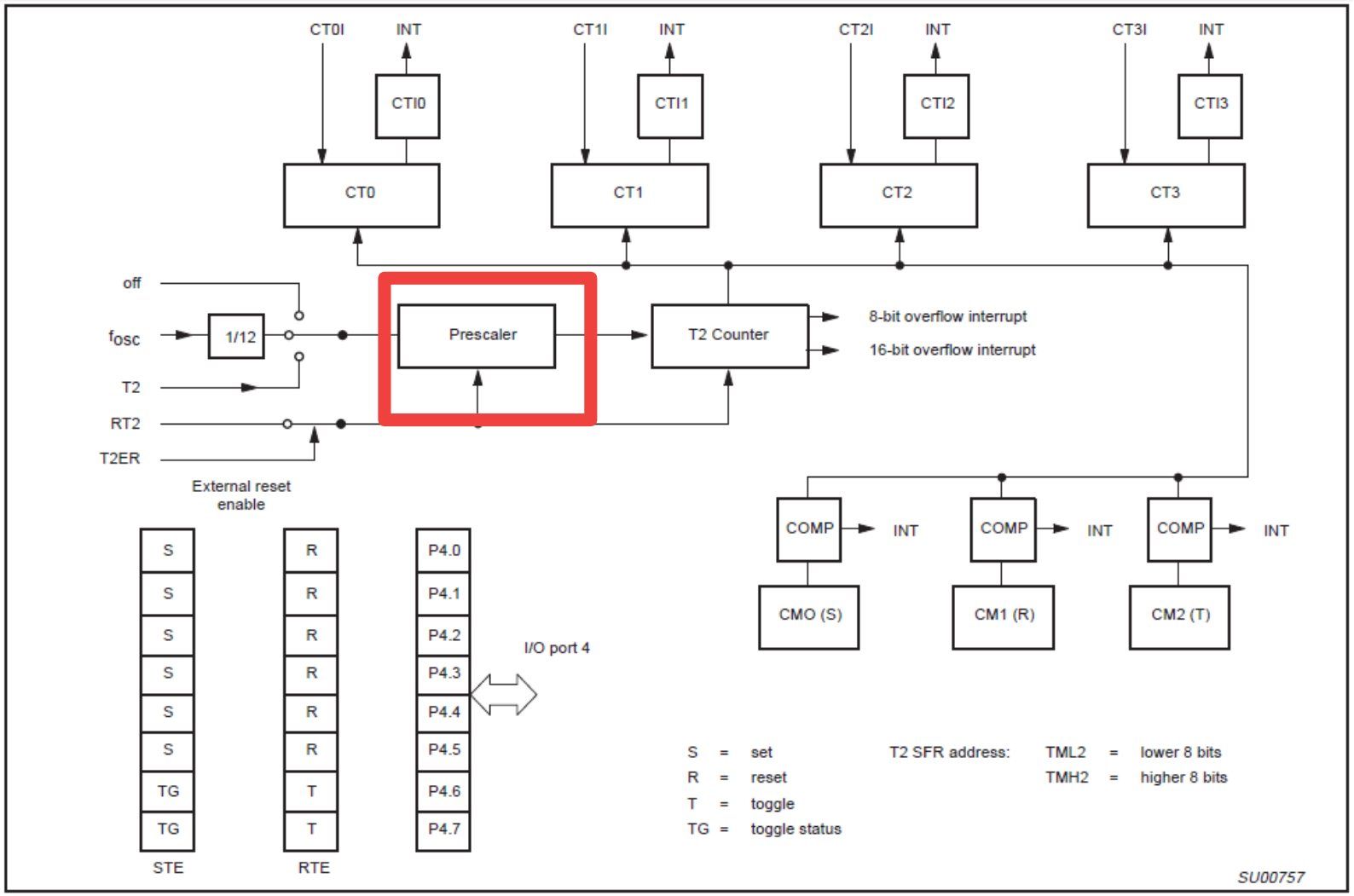
	7	6	5	4	3	2	1	0
TM2CON (EAH)	T2IS1	T2IS0	T2ER	T2BO	T2P1	T2P0	T2MS1	T2MS0
	(MSB)							(LSB)



TM2CON.1 T2MS1
TM2CON.0 T2MS0
} Timer T2 mode select

T2MS1	T2MS0	Mode Selected
0	0	Timer T2 halted (off)
0	1	T2 clock source = $f_{OSC}/12$
1	0	Test mode; do not use
1	1	T2 clock source = pin T2

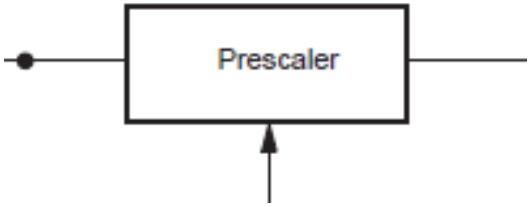
Timer 2


CT0I
INT
CTI0
CT0
CT1I
INT
CTI1
CT1
CT2I
INT
CTI2
CT2
CT3I
INT
CTI3
CT3
off
fosc
1/12
T2
RT2
T2ER
Prescaler
T2 Counter
8-bit overflow interrupt
16-bit overflow interrupt
External reset enable
COMP
INT
CMO (S)
CM1 (R)
CM2 (T)
S
R
P4.0
P4.1
P4.2
P4.3
P4.4
P4.5
P4.6
P4.7
TG
T
I/O port 4
STE
RTE
S = set
R = reset
T = toggle
TG = toggle status
T2 SFR address:
TML2 = lower 8 bits
TMH2 = higher 8 bits
SU00757

Timer 2

Prescaler. fosc/12 beste zatitzaile edo prescaler batekatik zatitu daiteke.

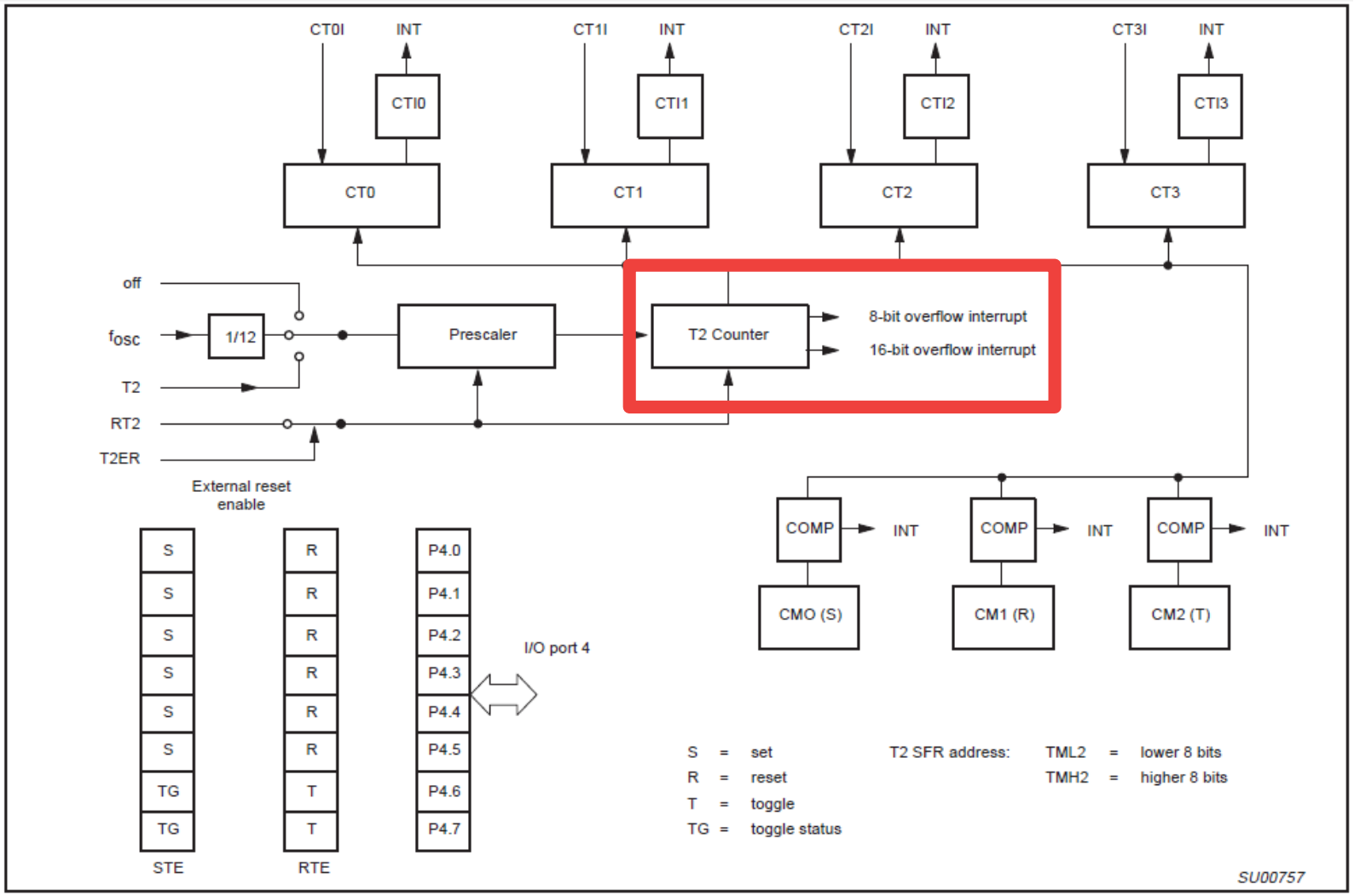
	7	6	5	4	3	2	1	0
TM2CON (EAH)	T2IS1	T2IS0	T2ER	T2BO	T2P1	T2P0	T2MS1	T2MS0
	(MSB)							(LSB)



TM2CON.3 T2P1
TM2CON.2 T2P0
} Timer T2 prescaler select

T2P1	T2P0	Timer T2 Clock
0	0	Clock source
0	1	Clock source/2
1	0	Clock source/4
1	1	Clock source/8

Timer 2


CT0I
INT
CTI0
CT0
CT1I
INT
CTI1
CT1
CT2I
INT
CTI2
CT2
CT3I
INT
CTI3
CT3
off
fosc
1/12
T2
RT2
T2ER
Prescaler
T2 Counter
8-bit overflow interrupt
16-bit overflow interrupt
External reset enable
COMP
INT
CMO (S)
CM1 (R)
CM2 (T)
S
R
T
TG
P4.0
P4.1
P4.2
P4.3
P4.4
P4.5
P4.6
P4.7
I/O port 4
STE
RTE
S = set
R = reset
T = toggle
TG = toggle status
T2 SFR address:
TML2 = lower 8 bits
TMH2 = higher 8 bits
SU00757

Timer 2

Interrupzioak.

	7	6	5	4	3	2	1	0
TM2CON (EAH)	T2IS1	T2IS0	T2ER	T2BO	T2P1	T2P0	T2MS1	T2MS0
	(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
TM2CON.7	TSIS1	Timer T2 16-bit overflow interrupt select
TM2CON.6	T2IS0	Timer T2 byte overflow interrupt select
TM2CON.5	T2ER	Timer T2 external reset enable. When this bit is set, Timer T2 may be reset by a rising edge on RT2 (P1.5).
TM2CON.4	T2BO	Timer T2 byte overflow interrupt flag

Timer 2

Interrupzioak. Enableak.

	7	6	5	4	3	2	1	0
TM2CON (EAH)	T2IS1	T2IS0	T2ER	T2BO	T2P1	T2P0	T2MS1	T2MS0
	(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
TM2CON.7	TSIS1	Timer T2 16-bit overflow interrupt select
TM2CON.6	T2IS0	Timer T2 byte overflow interrupt select
TM2CON.5	T2ER	Timer T2 external reset enable. When this bit is set, Timer T2 may be reset by a rising edge on RT2 (P1.5).
TM2CON.4	T2BO	Timer T2 byte overflow interrupt flag

Timer 2

Interrupzioak. Flag-ak. Programa bidez zerora eraman behar.

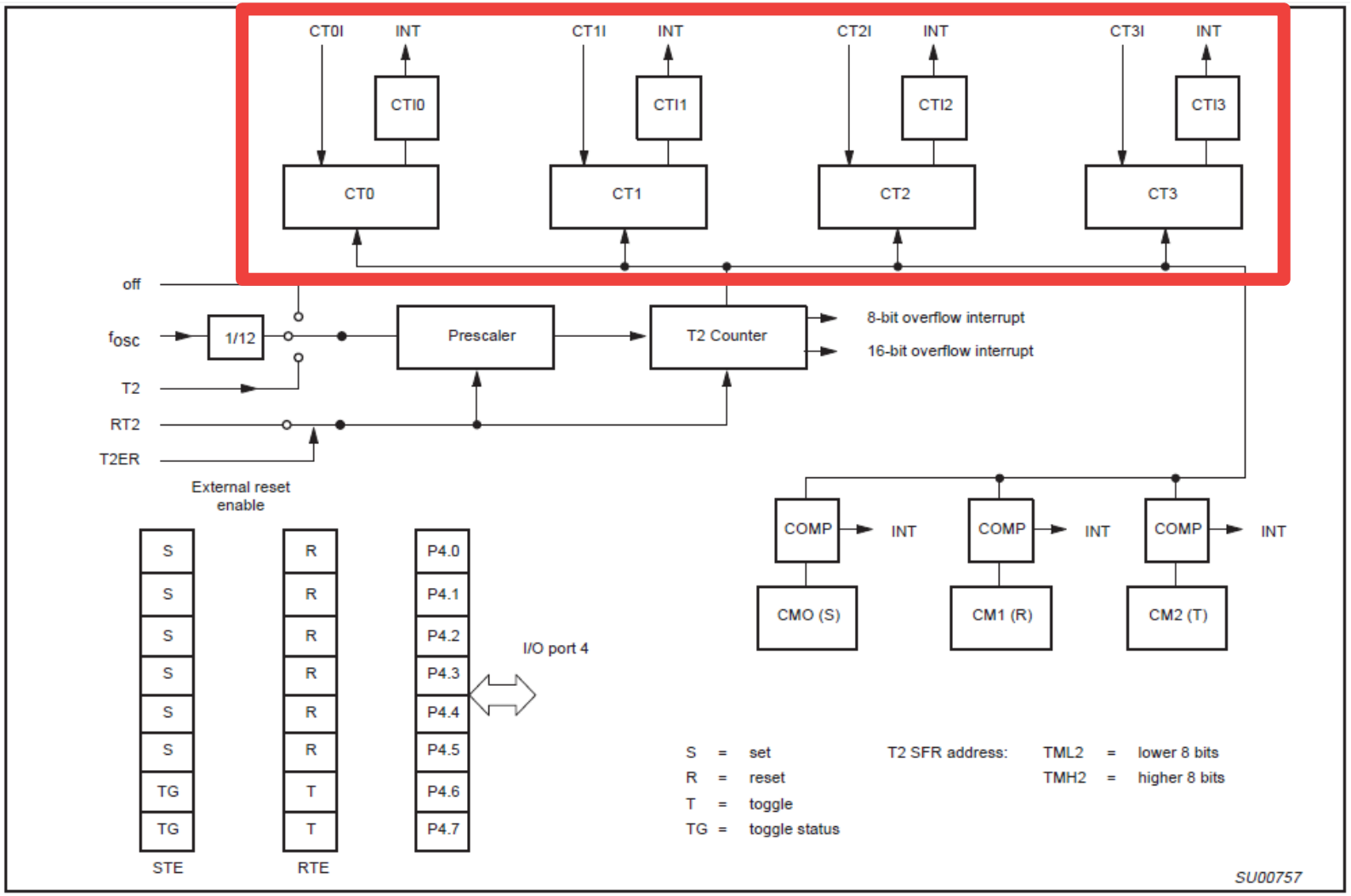
	7	6	5	4	3	2	1	0
TM2CON (EAH)	T2IS1	T2IS0	T2ER	T2BO	T2P1	T2P0	T2MS1	T2MS0
	(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
TM2CON.7	TSIS1	Timer T2 16-bit overflow interrupt select
TM2CON.6	T2IS0	Timer T2 byte overflow interrupt select
TM2CON.5	T2ER	Timer T2 external reset enable. When this bit is set, Timer T2 may be reset by a rising edge on RT2 (P1.5)
TM2CON.4	T2BO	Timer T2 byte overflow interrupt flag

	7	6	5	4	3	2	1	0
TM2IR (C8H)	T2OV	CMI2	CMI1	CMI0	CTI3	CTI2	CTI1	CTI0
	(MSB)							(LSB)

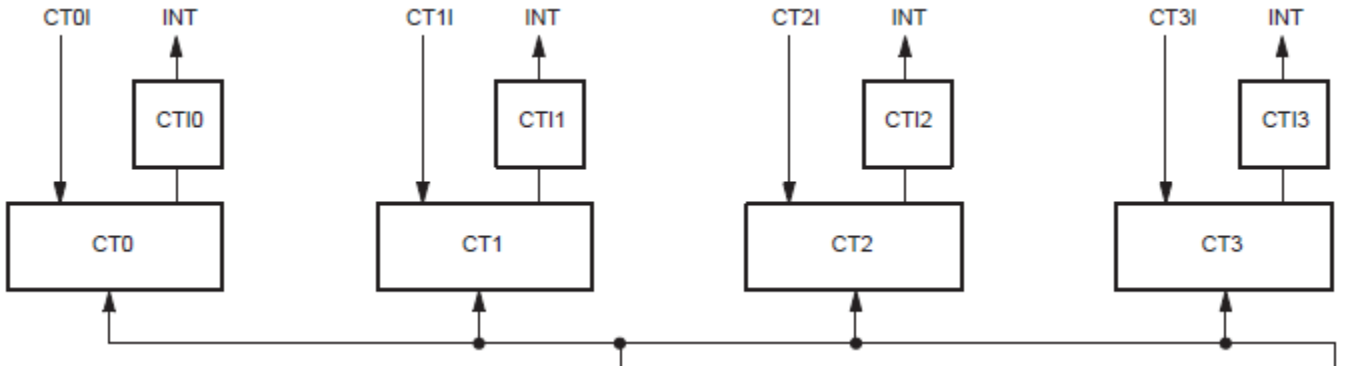
BIT	SYMBOL	FUNCTION
TM2IR.7	T2OV	Timer T2 16-bit overflow interrupt flag
TM2IR.6	CMI2	CM2 interrupt flag
TM2IR.5	CMI1	CM1 interrupt flag
TM2IR.4	CMI0	CM0 interrupt flag
TM2IR.3	CTI3	CT3 interrupt flag
TM2IR.2	CTI2	CT2 interrupt flag
TM2IR.1	CTI1	CT1 interrupt flag
TM2IR.0	CTI0	CT0 interrupt flag

Timer 2


CT0I
INT
CTI0
CT0
CT1I
INT
CTI1
CT1
CT2I
INT
CTI2
CT2
CT3I
INT
CTI3
CT3
off
fosc
1/12
Prescaler
T2 Counter
8-bit overflow interrupt
16-bit overflow interrupt
T2
RT2
T2ER
External reset enable
COMP
INT
CMO (S)
CM1 (R)
CM2 (T)
S
R
P4.0
P4.1
P4.2
P4.3
P4.4
P4.5
P4.6
P4.7
I/O port 4
TG
T
STE
RTE
S = set
R = reset
T = toggle
TG = toggle status
T2 SFR address:
TML2 = lower 8 bits
TMH2 = higher 8 bits
SU00757

Timer 2

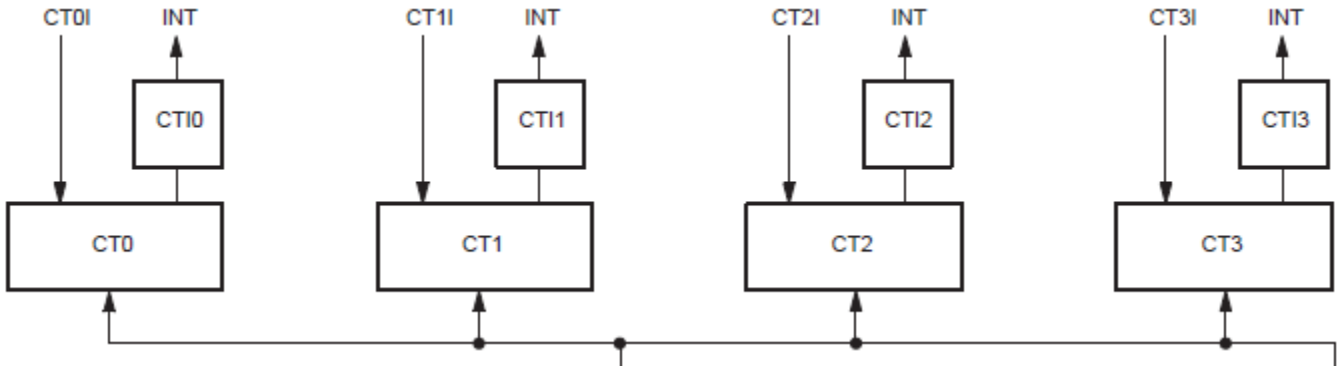
Capture Register. CTxI pinetik aldaketa bat datorrenean, T2 CTHx eta CTLx-era eramaten da.



CTH3#	Capture high 3	CFH	xxxxxxxxB
CTH2#	Capture high 2	CEH	xxxxxxxxB
CTH1#	Capture high 1	CDH	xxxxxxxxB
CTH0#	Capture high 0	CCH	xxxxxxxxB
CMH2#	Compare high 2	CBH	00H
CMH1#	Compare high 1	CAH	00H
CMH0#	Compare high 0	C9H	00H
CTL3#	Capture low 3	AFH	xxxxxxxxB
CTL2#	Capture low 2	AEH	xxxxxxxxB
CTL1#	Capture low 1	ADH	xxxxxxxxB
CTL0#	Capture low 0	ACH	xxxxxxxxB
CML2#	Compare low 2	ABH	00H
CML1#	Compare low 1	AAH	00H
CML0#	Compare low 0	A9H	00H

Timer 2

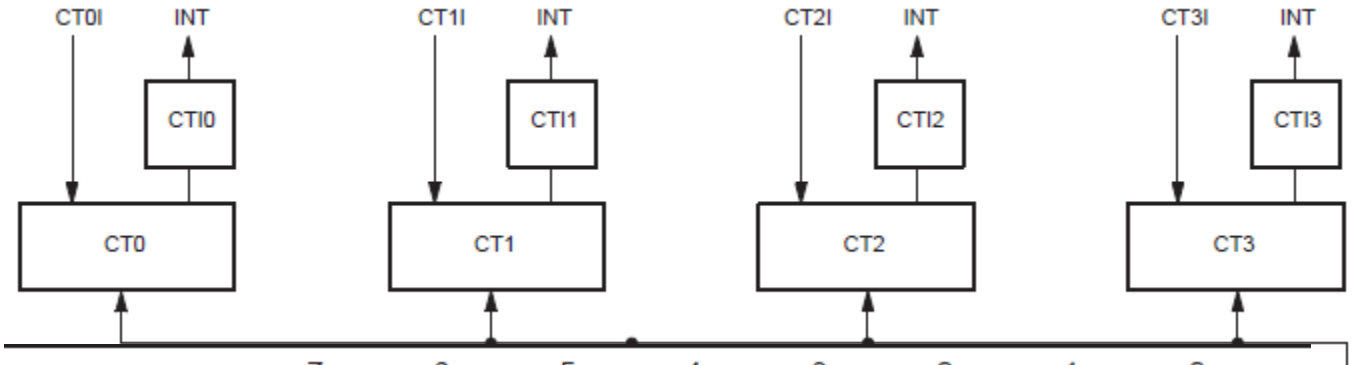
Capture Register. CTxI pinetik aldaketa bat datorrenean, T2 CTHx eta CTLx-era eramaten da.



CTH3#	Capture high 3	CFH		xxxxxxxxB
CTH2#	Capture high 2	CEH		xxxxxxxxB
CTH1#	Capture high 1	CDH		xxxxxxxxB
CTH0#	Capture high 0	CCH		xxxxxxxxB
CMH1#	Compare high 1	CAH		00H
CTL3#	Capture low 3	AFH		xxxxxxxxB
CTL2#	Capture low 2	AEH		xxxxxxxxB
CTL1#	Capture low 1	ADH		xxxxxxxxB
CTL0#	Capture low 0	ACH		xxxxxxxxB
CML1#	Compare low 1	AAH		00H
CML0#	Compare low 0	A9H		00H

Timer 2

Capture Register. CTxI flanko positibo edo negatibo bat izan behar den CTCON-en definitu.

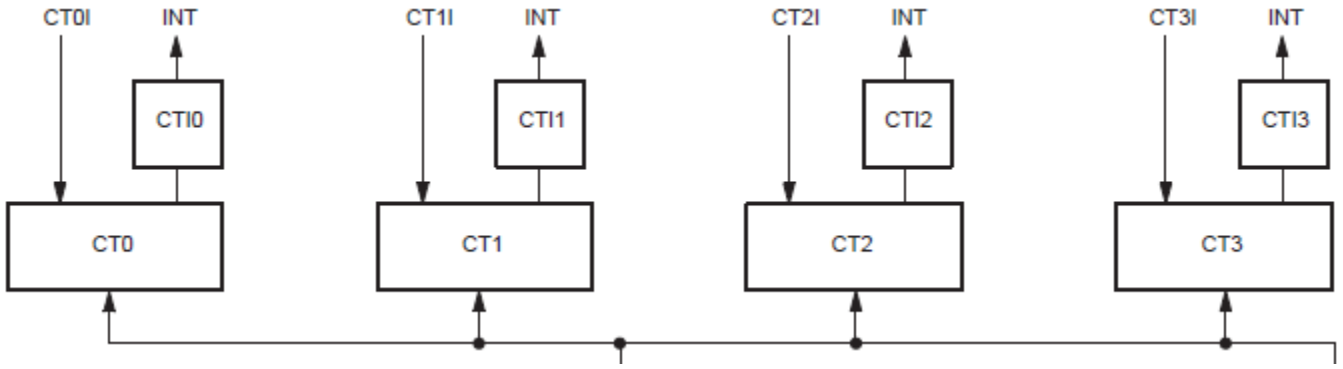


	7	6	5	4	3	2	1	0
CTCON (EBH)	CTN3	CTP3	CTN2	CTP2	CTN1	CTP1	CTN1	CTP0
	(MSB)							(LSB)

BIT	SYMBOL	CAPTURE/INTERRUPT ON:
CTCON.7	CTN3	Capture Register 3 triggered by a falling edge on CT3I
CTCON.6	CTP3	Capture Register 3 triggered by a rising edge on CT3I
CTCON.5	CTN2	Capture Register 2 triggered by a falling edge on CT2I
CTCON.4	CTP2	Capture Register 2 triggered by a rising edge on CT2I
CTCON.3	CTN1	Capture Register 1 triggered by a falling edge on CT1I
CTCON.2	CTP1	Capture Register 1 triggered by a rising edge on CT1I
CTCON.1	CTN0	Capture Register 0 triggered by a falling edge on CT0I
CTCON.0	CTP0	Capture Register 0 triggered by a rising edge on CT0I

Timer 2

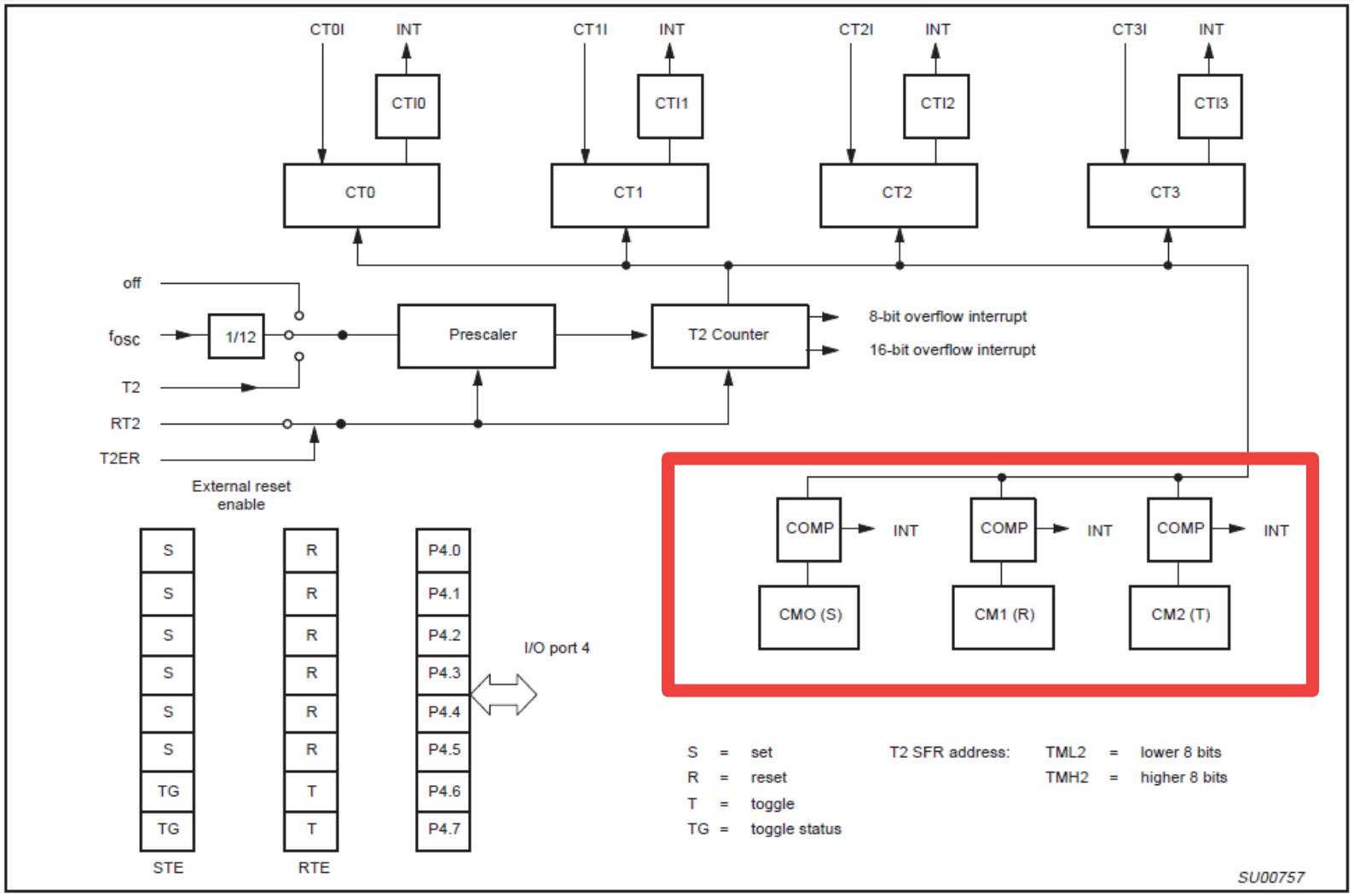
Capture Register. CtxI flanko positibo edo negatibo bat izan behar den CTCON-en definitu.



	7	6	5	4	3	2	1	0
TM2IR (C8H)	T2OV	CMI2	CMI1	CMI0	CTI3	CTI2	CTI1	CTI0
	(MSB)							(LSB)

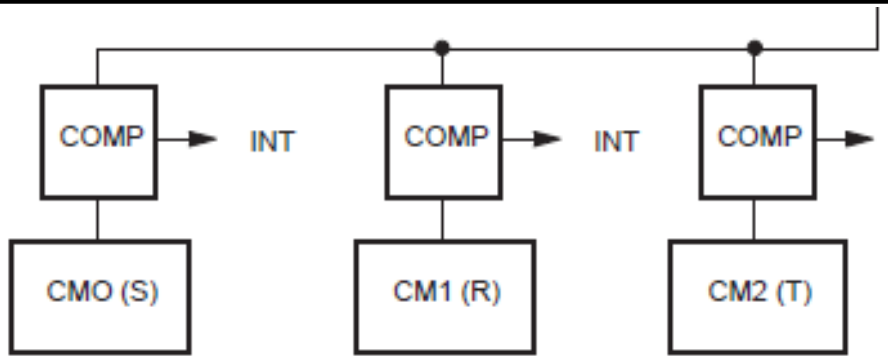
BIT	SYMBOL	FUNCTION
TM2IR.7	T2OV	Timer T2 16-bit overflow interrupt flag
TM2IR.6	CMI2	CM2 interrupt flag
TM2IR.5	CMI1	CM1 interrupt flag
TM2IR.4	CMI0	CM0 interrupt flag
TM2IR.3	CTI3	CT3 interrupt flag
TM2IR.2	CTI2	CT2 interrupt flag
TM2IR.1	CTI1	CT1 interrupt flag
TM2IR.0	CTI0	CT0 interrupt flag

Timer 2


CT0I
INT
CTI0
CT0
CT1I
INT
CTI1
CT1
CT2I
INT
CTI2
CT2
CT3I
INT
CTI3
CT3
off
fosc
1/12
T2
RT2
T2ER
External reset enable
Prescaler
T2 Counter
8-bit overflow interrupt
16-bit overflow interrupt
COMP
INT
CMO (S)
CM1 (R)
CM2 (T)
S
R
T
TG
STE
RTE
P4.0
P4.1
P4.2
P4.3
P4.4
P4.5
P4.6
P4.7
I/O port 4
S = set
R = reset
T = toggle
TG = toggle status
T2 SFR address:
TML2 = lower 8 bits
TMH2 = higher 8 bits
SU00757

Timer 2

Compare Logic. CMx-arekin konparatu eta berdin izatekotan interrupzio bat eskatu.



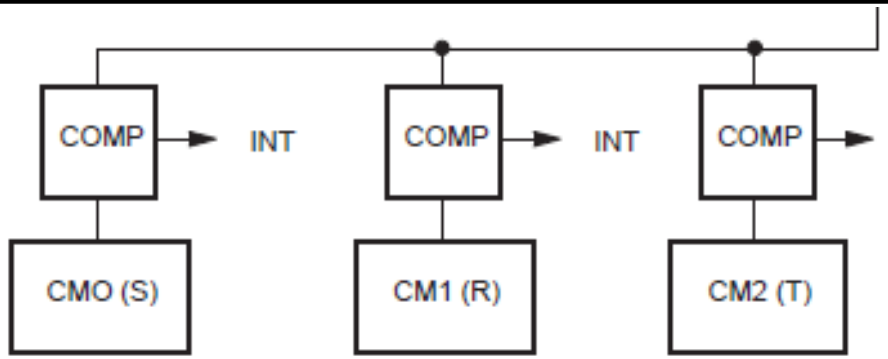
S = set
R = reset
T = toggle
TG = toggle status

T2 SFR address: TML2 = lower 8 bits
TMH2 = higher 8 bits

CTH3#	Capture high 3	CFH	xxxxxxxxB
CTH2#	Capture high 2	CEH	xxxxxxxxB
CTH1#	Capture high 1	CDH	xxxxxxxxB
CMH2#	Compare high 2	CBH	00H
CMH1#	Compare high 1	CAH	00H
CMH0#	Compare high 0	C9H	00H
CTL2#	Capture low 2	AEH	xxxxxxxxB
CTL1#	Capture low 1	ADH	xxxxxxxxB
CML2#	Compare low 2	ABH	00H
CML1#	Compare low 1	AAH	00H
CML0#	Compare low 0	A9H	00H

Timer 2

Compare Logic. CMx-arekin konparatu eta berdin izatekotan interrupzio bat eskatu.



S = set
R = reset
T = toggle
TG = toggle status

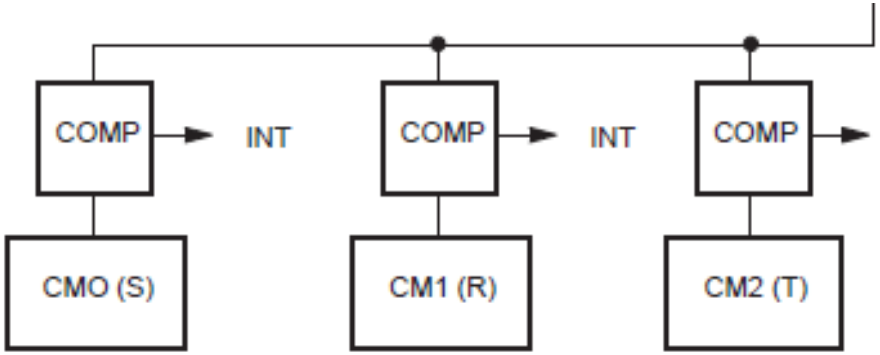
T2 SFR address: TML2 = lower 8 bits
TMH2 = higher 8 bits

	7	6	5	4	3	2	1	0
TM2IR (C8H)	T2OV	CMI2	CMI1	CMI0	CTI3	CTI2	CTI1	CTI0
	(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
TM2IR.7	T2OV	Timer T2 16-bit overflow interrupt flag
TM2IR.6	CMI2	CM2 interrupt flag
TM2IR.5	CMI1	CM1 interrupt flag
TM2IR.4	CMI0	CM0 interrupt flag
TM2IR.3	CTI3	CT3 interrupt flag
TM2IR.2	CTI2	CT2 interrupt flag
TM2IR.1	CTI1	CT1 interrupt flag
TM2IR.0	CTI0	CT0 interrupt flag

Timer 2

Compare Logic. CMx-arekin konparatu eta berdin izatekotan interrupzio bat eskatu. RTE eta STE aldatu.



S = set
R = reset
T = toggle
TG = toggle status

T2 SFR address: TML2 = lower 8 bits
TMH2 = higher 8 bits

RTE (EFH)

7	6	5	4	3	2	1	0
TP47	TP46	RP45	RP44	RP43	RP42	RO41	RP40
(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
RTE.7	TP47	If "1" then P4.7 toggles on a match between CM1 and Timer T2
RTE.6	TP46	If "1" then P4.6 toggles on a match between CM1 and Timer T2
RTE.5	RP45	If "1" then P4.5 is reset on a match between CM1 and Timer T2
RTE.4	RP44	If "1" then P4.4 is reset on a match between CM1 and Timer T2
RTE.3	RP43	If "1" then P4.3 is reset on a match between CM1 and Timer T2
RTE.2	RP42	If "1" then P4.2 is reset on a match between CM1 and Timer T2
RTE.1	RP41	If "1" then P4.1 is reset on a match between CM1 and Timer T2
RTE.0	RP40	If "1" then P4.0 is reset on a match between CM1 and Timer T2

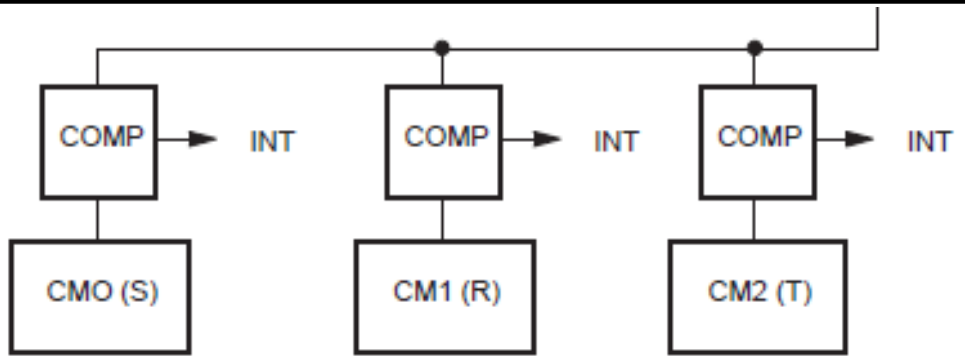
STE (EEH)

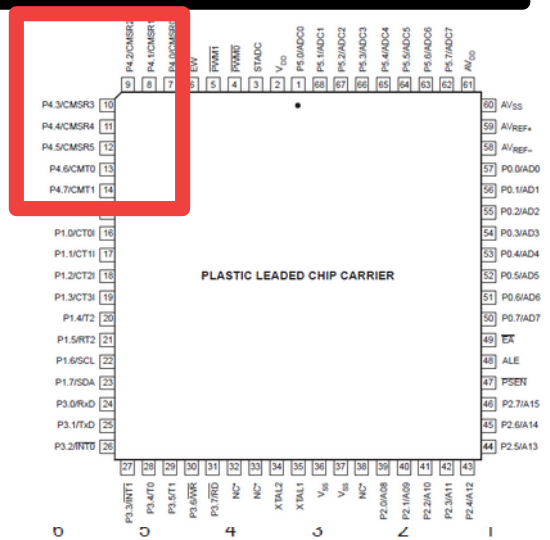
7	6	5	4	3	2	1	0
TG47	TG46	SP45	SP44	SP43	SP42	SP41	SP40
(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
STE.7	TG47	Toggle flip-flops
STE.6	TG46	Toggle flip-flops
STE.5	SP45	If "1" then P4.5 is set on a match between CM0 and Timer T2
STE.4	SP44	If "1" then P4.4 is set on a match between CM0 and Timer T2
STE.3	SP43	If "1" then P4.3 is set on a match between CM0 and Timer T2
STE.2	SP42	If "1" then P4.2 is set on a match between CM0 and Timer T2
STE.1	SP41	If "1" then P4.1 is set on a match between CM0 and Timer T2
STE.0	SP40	If "1" then P4.0 is set on a match between CM0 and Timer T2

Timer 2

Compare Logic. CMx-arekin konparatu eta berdin izatekotan interrupzio bat eskatu. RTE eta STE aldatu.





RTE (EFH)

7	6	5	4	3	2	1	0
TP47	TP46	RP45	RP44	RP43	RP42	RO41	RP40
(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
RTE.7	TP47	If "1" then P4.7 toggles on a match between CM1 and Timer T2
RTE.6	TP46	If "1" then P4.6 toggles on a match between CM1 and Timer T2
RTE.5	RP45	If "1" then P4.5 is reset on a match between CM1 and Timer T2
RTE.4	RP44	If "1" then P4.4 is reset on a match between CM1 and Timer T2
RTE.3	RP43	If "1" then P4.3 is reset on a match between CM1 and Timer T2
RTE.2	RP42	If "1" then P4.2 is reset on a match between CM1 and Timer T2
RTE.1	RP41	If "1" then P4.1 is reset on a match between CM1 and Timer T2
RTE.0	RP40	If "1" then P4.0 is reset on a match between CM1 and Timer T2

STE (EEH)

7	6	5	4	3	2	1	0
TG47	TG46	SP45	SP44	SP43	SP42	SP41	SP40
(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
STE.7	TG47	Toggle flip-flops
STE.6	TG46	Toggle flip-flops
STE.5	SP45	If "1" then P4.5 is set on a match between CM0 and Timer T2
STE.4	SP44	If "1" then P4.4 is set on a match between CM0 and Timer T2
STE.3	SP43	If "1" then P4.3 is set on a match between CM0 and Timer T2
STE.2	SP42	If "1" then P4.2 is set on a match between CM0 and Timer T2
STE.1	SP41	If "1" then P4.1 is set on a match between CM0 and Timer T2
STE.0	SP40	If "1" then P4.0 is set on a match between CM0 and Timer T2

Timer 2

Capture Register, Compare Logic…. Enable?

	7	6	5	4	3	2	1	0
IEN1 (E8H)	ET2	ECM2	ECM1	ECM0	ECT3	ECT2	ECT1	ECT0
	(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
IEN1.7	ET2	Enable Timer T2 overflow interrupt(s)
IEN1.6	ECM2	Enable T2 Comparator 2 interrupt
IEN1.5	ECM1	Enable T2 Comparator 1 interrupt
IEN1.4	ECM0	Enable T2 Comparator 0 interrupt
IEN1.3	ECT3	Enable T2 Capture register 3 interrupt
IEN1.2	ECT2	Enable T2 Capture register 2 interrupt
IEN1.1	ECT1	Enable T2 Capture register 1 interrupt
IEN1.0	ECT0	Enable T2 Capture register 0 interrupt

Timer 2

Interrupt priority?

	7	6	5	4	3	2	1	0
IP0 (B8H)	–	PAD	PS1	PS0	PT1	PX1	PT0	PX0
	(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
IP0.7	–	Unused
IP0.6	PAD	ADC interrupt priority level
IP0.5	PS1	SIO1 (I^2C) interrupt priority level
IP0.4	PS0	SIO0 (UART) interrupt priority level
IP0.3	PT1	Timer 1 interrupt priority level
IP0.2	PX1	External interrupt 1 priority level
IP0.1	PT0	Timer 0 interrupt priority level
IP0.0	PX0	External interrupt 0 priority level

SU00763

Figure 30. Interrupt Priority Register (IP0)

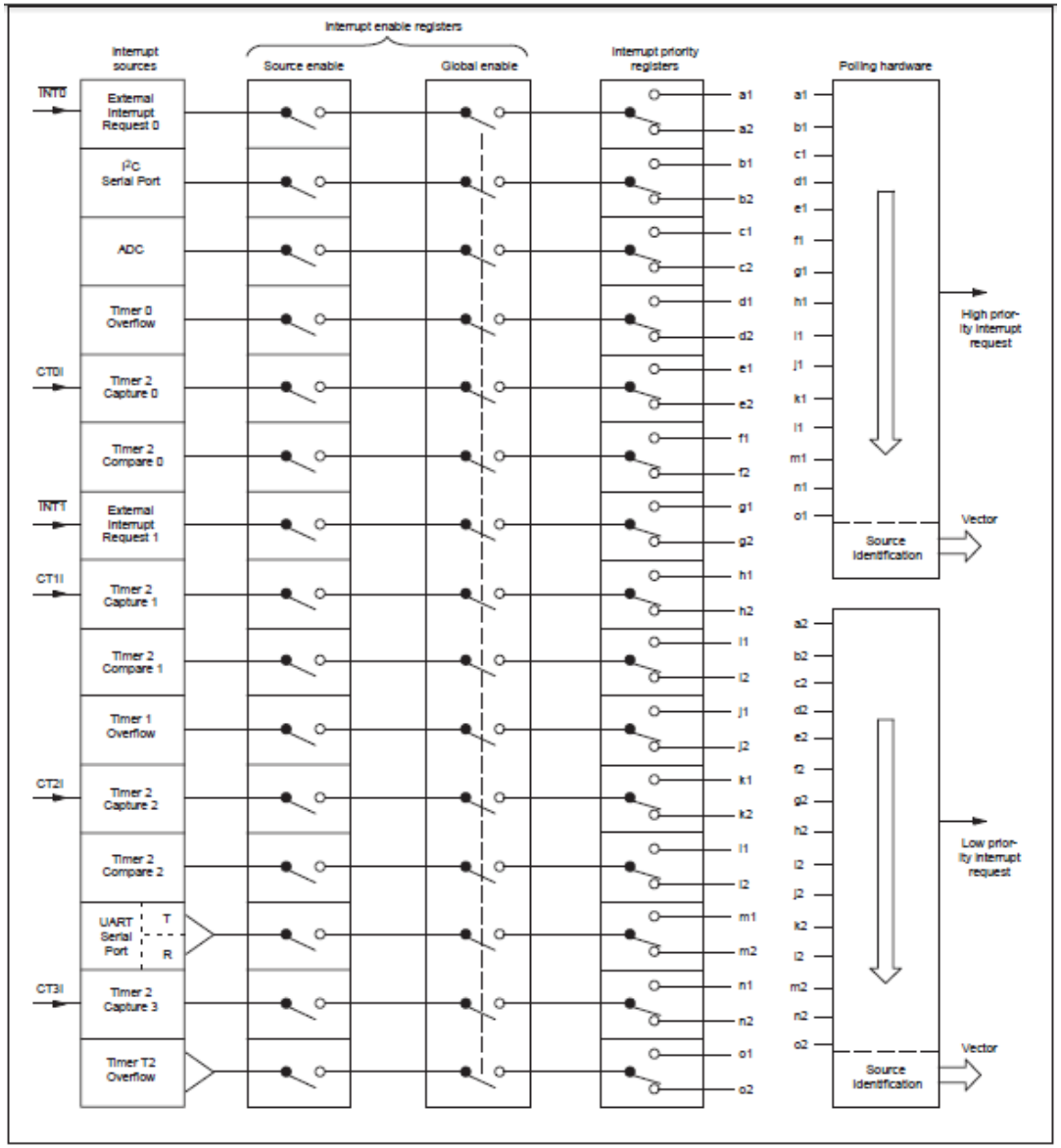
	7	6	5	4	3	2	1	0
IP1 (F8H)	PT2	PCM2	PCM1	PCM0	PCT3	PCT2	PCT1	PCT0
	(MSB)							(LSB)

BIT	SYMBOL	FUNCTION
IP1.7	PT2	T2 overflow interrupt(s) priority level
IP1.6	PCM2	T2 comparator 2 interrupt priority level
IP1.5	PCM1	T2 comparator 1 interrupt priority level
IP1.4	PCM0	T2 comparator 0 interrupt priority level
IP1.3	PCT3	T2 capture register 3 interrupt priority level
IP1.2	PCT2	T2 capture register 2 interrupt priority level
IP1.1	PCT1	T2 capture register 1 interrupt priority level
IP1.0	PCT0	T2 capture register 0 interrupt priority level

SU00764

Figure 31. Interrupt Priority Register (IP1)

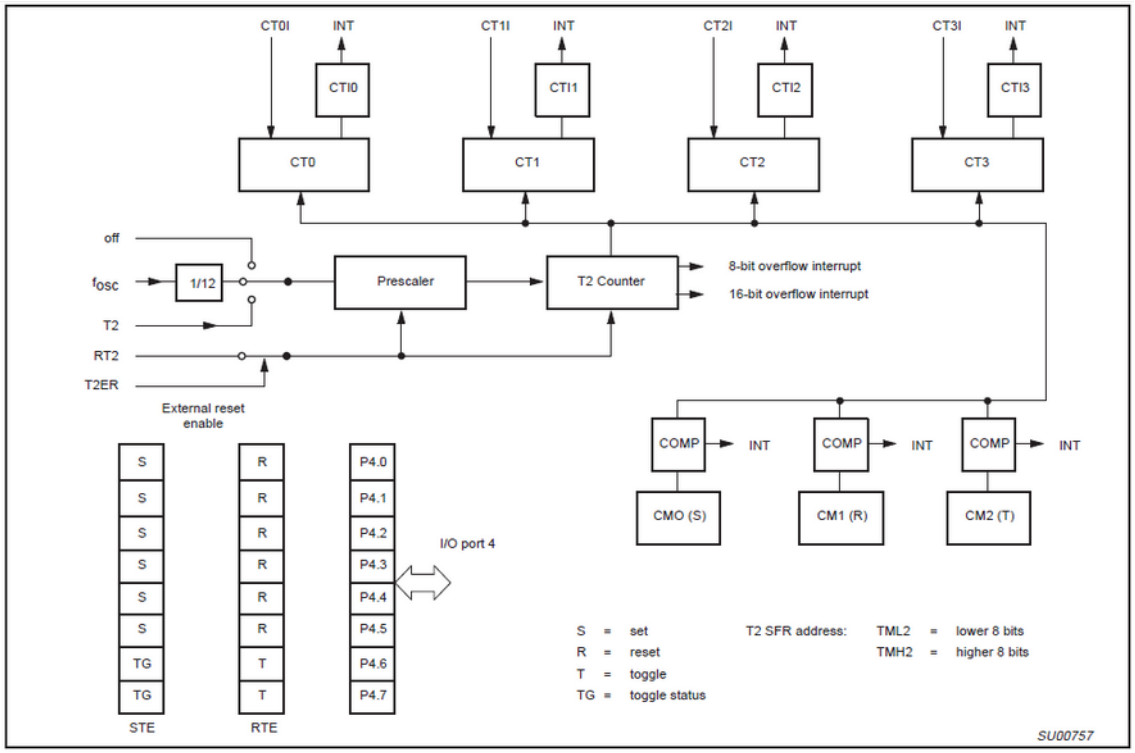
Timer 2


Interrupt enable registers
Interrupt sources
Source enable
Global enable
Interrupt priority registers
Polling hardware
INT0
External Interrupt Request 0
I²C Serial Port
ADC
Timer 0 Overflow
CT0I
Timer 2 Capture 0
Timer 2 Compare 0
INT1
External Interrupt Request 1
CT1I
Timer 2 Capture 1
Timer 2 Compare 1
Timer 1 Overflow
CT2I
Timer 2 Capture 2
Timer 2 Compare 2
UART Serial Port
T
R
CT3I
Timer 2 Capture 3
Timer T2 Overflow
a1 a2 b1 b2 c1 c2 d1 d2 e1 e2 f1 f2 g1 g2 h1 h2 i1 i2 j1 j2 k1 k2 l1 l2 m1 m2 n1 n2 o1 o2
High priority interrupt request
Vector
Source Identification
Low priority interrupt request
Vector
Source Identification

Timer 2

Zelan konfiguratuko litzateke Timer2, Timer0-a heldu ezin litzatekeen aurreko kasuan?

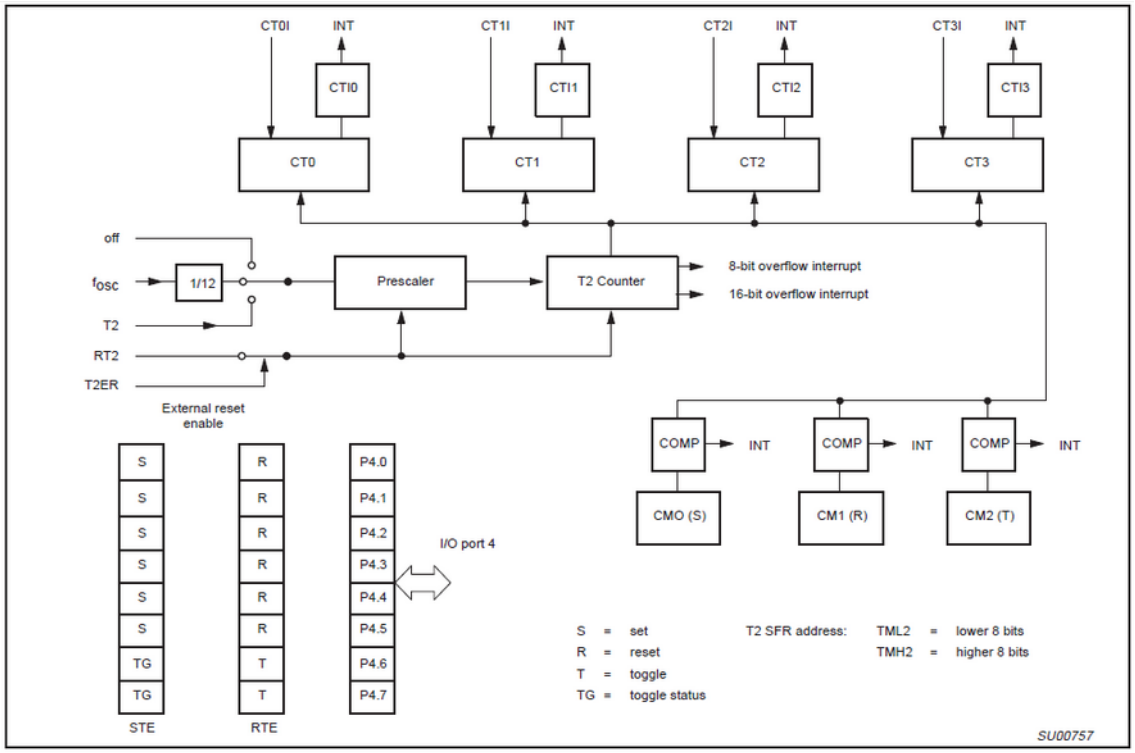
fclk = 24MHz, 34ms neurtu nahi dira. Zelan neurtuko genituzke?



Timer 2

Zelan konfiguratuko litzateke Timer2?

Momentu batetik aurrera kontatu nahi da, eta zenbat denbora igaro den jakin nahi da, kanpotik seinale bat datorrenean.



HELBURUAK

Denbora handia kontatzeko Timer2 dagoela ezagutzea

80c552-aren Timer2-a zelan konfiguratzen den ikastea

eman ta zabal zazu

Universidad del País Vasco
Euskal Herriko Unibertsitatea

BILBOKO INGENIARITZA ESKOLA
ESCUELA DE INGENIERÍA DE BILBAO

Teknologia Elektronikoa Saila

KONPUTAGAILUEN ARKITEKTURA
80c552 - Timer2

Kudeaketa eta Informazio Sistemen Informatikaren Ingenieritzako Graduaren 3. maila

Irakaslea: Alain Sanchez
(alain.sanchez@ehu.eus)

2019-2020, 1. lauhilabetea