Technology
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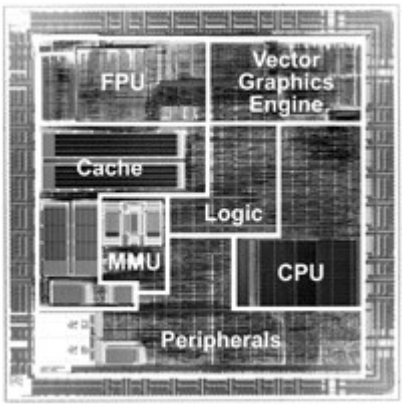
360-MIPS SuperH RISC Processor Enables Personal Access Systems

The SH7750 (SH-4 Series) MPU is a complete solution that helps reduce system OEM's time to market.

The SH-4 series of 2-issue superscalar, 64-bit external data bus RISC microprocessors (MPUs) boosts performance up to the 360-MIPS (Dhrystone) level, while also driving toward a 10¢/MIPS price/performance threshold. The CPU in SH-4 series devices processes two instructions per cycle to far outperform other embedded processors at similar clock rates. The first device in the SH-4 series is the SH7750, which operates with an internal clock of 200 MHz.

SH-4 series MPUs enable exciting new applications. The devices are ideal for the innovative Personal Access products such as Internet appliances that use computing, communications, and multimedia technologies to deliver the information users want where, when, and how they want it.



The SH7750 Launches the SH-4 series, achieving 360 MIPS at 200 MHz and 1.4-Gflops graphics performance. The SuperH architecture is driving toward the 10c/MIPS price/performance point.

Continuing the breakthroughs

The SH-4 series extends the long string of SuperH processor price/performance breakthroughs that have helped redefine the embedded processor market. To date, SuperH processors have scored over 2,000 design wins and lead in cumulative RISC shipments worldwide. According to the February 1997 issue of Andrew Allison's Inside the New Computer Industry newsletter, the 32-bit SuperH™ RISC architecture achieved a 32 percent share in 1996 and is the worldwide leader in shipments over the past three years (1994–1996), during which time 35.1 million SuperH devices were shipped.

Hitachi processors that run the Microsoft® Windows® CE operating system offer performance of from 60 to 360 MIPS. SH-3 MPUs (SH7700 series) are the processors of choice for Windows CE based products (used in 11 of the first 17 H/PCs) and are widely used as the main engine in consumer multimedia products. The volume shipments help drive down device prices and ultimately system cost.

Windows CE based products

"The Hitachi SH-4 embedded processor represents a very high performance processor for the Windows CE operating system," said Ted Kummert, director of the Windows CE multimedia consumer product unit at Microsoft. "The combination of the Windows CE operating system and the SH-4 will be well-suited for key markets like TV set-top boxes, mobile computing devices, and Windows CE based terminals."

Built with 0.25-µm process

The SH-4 series uses a 0.25-µm process and the chip operates at 1.8 V internally from an external supply voltage that can be up to 3.3 V. The 200-MHz/360-MIPS SH7750 dissipates 1.5 Watt, typical, for 240-MIPS/Watt and 1.8-MIPS/MHz ratings. The SH7750 has an 8-KByte instruction cache and a 16-KByte data cache; an on-chip glueless memory interface that supports an 8/16/32/64-bit data bus, with a direct connection to SDRAM, DRAM, SRAM, ROM, and Flash; and a 4-channel DMA controller.

800-MByte/s transfers

With an external bus frequency of up to 100 MHz, the SH7750 achieves high data transfer speeds (800 MByte/s, peak). This bus speed is low relative to other high-speed processors, which helps to minimize RFI and EMI. The MPU's combination of performance, cache size, and high data transfer rate allows more functions to be executed in software, such as soft modems and MPEG decoders, for enhanced system design flexibility and software upgrades.

Upward compatibility

SH-4 series MPUs use a 16-bit, fixed-length instruction set, which is upward compatible with the SH-1, SH-2, SH-3, and SH-3E cores, for high code efficiency and reduced memory size requirements. Moreover, because of the 16-bit, fixed-length instruction set, the 8-KByte instruction cache for the SH7750 is as effective as a 16-KByte instruction cache on most 32-bit, fixed instruction length RISC processors. This allows the SH7750 to achieve its excellent performance while maintaining a low price for the embedded market.

The memory management unit (MMU) of the SH7750 is designed to run with protected-mode operating systems, including Windows CE and others. The MMU has 1-KByte, 4-KByte, 64-KByte, and 1-MByte page sizes, and a 64-entry fully associative translation lookaside buffer (TLB).

To help reduce device count allowing simpler, lower-cost systems the on-chip peripherals include an RTC, 32-bit timers, 2-channel SCI, and PCMCIA interface, as well as a floating-point unit (FPU) that conforms to both the IEEE-754 64-bit double-precision and 32-bit single-precision floating-point standards.

Graphics function: 1.4 Gflops

Manufacturers are improving the graphics capabilities of many products to display sophisticated information and entertainment. The SH7750 provides the FPU and a vector graphics engine (4x4 floating-point data matrix) that combine to achieve 1.4-Gflops peak floating-point performance at 200 MHz. The 128-bit computational processing capability supports 2D and 3D graphics and movement for more realistic images that use up to five million polygons per second.

In an Internet appliance such as a set-top box, the graphics capability of the SH7750 allows advanced OSDs (On-Screen Displays). By offloading computation-intensive graphics operations to the CPU core, the on-chip graphics functions help keep system throughput high.

Virtual reality applications

The 360-MIPS CPU performance, 1.4-Gflops graphics performance, and 800-MByte/s peak bus bandwidth of the SH7750 is enough processing capability to allow the MPU to be used in virtual reality applications. The chip is a perfect front-end for various 3D graphics architectures. It can assist in the seamless decompression of 2D and 3D media content, thus effectively increasing network bandwidth.

Because the SH7750 can provide higher throughput for higher screen update rates and fast geometry transformations for 3D rendering acceleration, it can enable greater levels of interactive content of improved visual quality. The SH7750 also has sufficient power to support VRML and Java-rich Web browsing.

Complete SH-4 support

Hitachi will support the SH-4 series on its D9000, the popular development platform for SuperH processors and Windows CE that enables fast, parallel hardware and software development, and validation. The D9000's baseboard, with plug-in CPU card, plug-in peripheral cards, and VHDL libraries, allows quick configuration of speed, memory, and peripherals. A reconfigurable peripherals interface and power monitoring capability ease the addition and optimization of functions and performance, and a color display option supports Windows CE 2.0.

Hitachi also provides an emulator with JTAG interface to support the SH-4 on-chip debug capability.

For systems that need to reduce development time while keeping device count low, Hitachi plans to offer ASSP (application specific standard product) companion chips that can be used in SH-4-based system designs. The first of these ASSPs will be released in the second half of 1998.

Range of SH-4 MPUs planned

Like the SH-3 series before it, the SH-4 series will expand into a family of processors. Currently in development are higher and lower clock rate SH7750-like versions; different package options that will give

system engineers additional price/ performance points from which to choose; and other devices for specific markets, such as lower-power versions for battery-powered devices.

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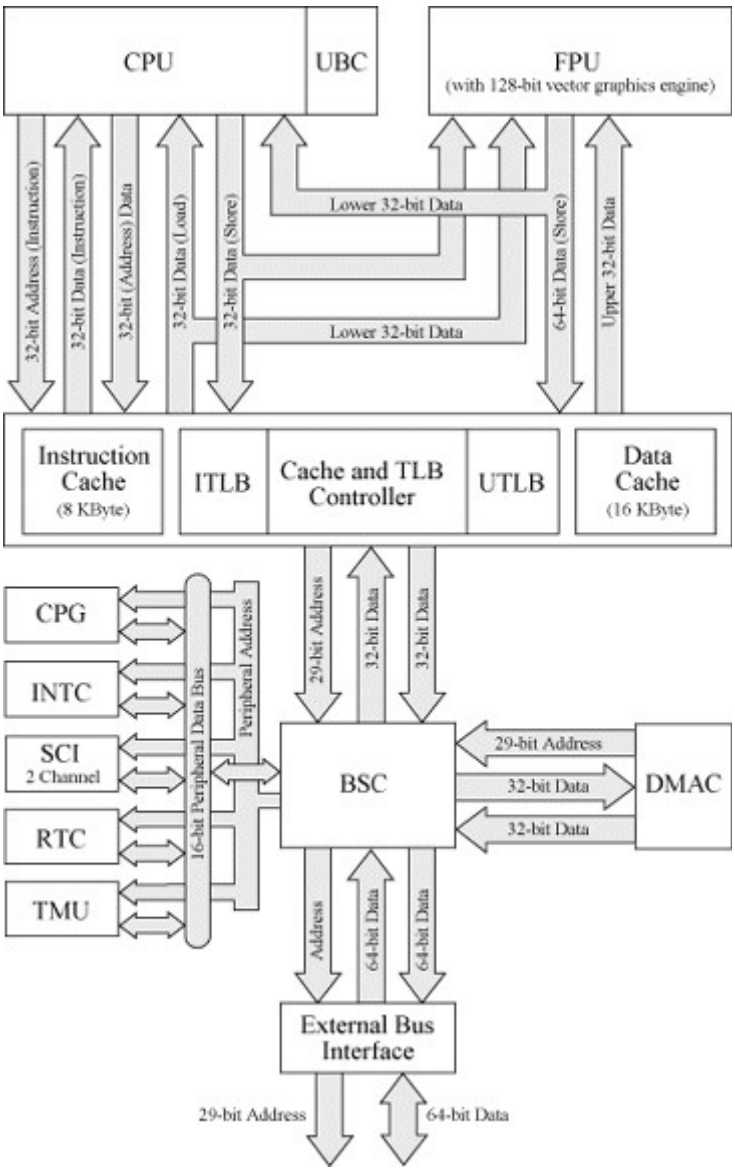

The 360-MIPS, 200-MHz SH7750 RISC microprocessor is ideal for Personal Access applications. Development platform support helps reduce time to market.
