Project Name : SFBW01
Platform : Braswell(For Valleyview-D/I/M System On Chip)

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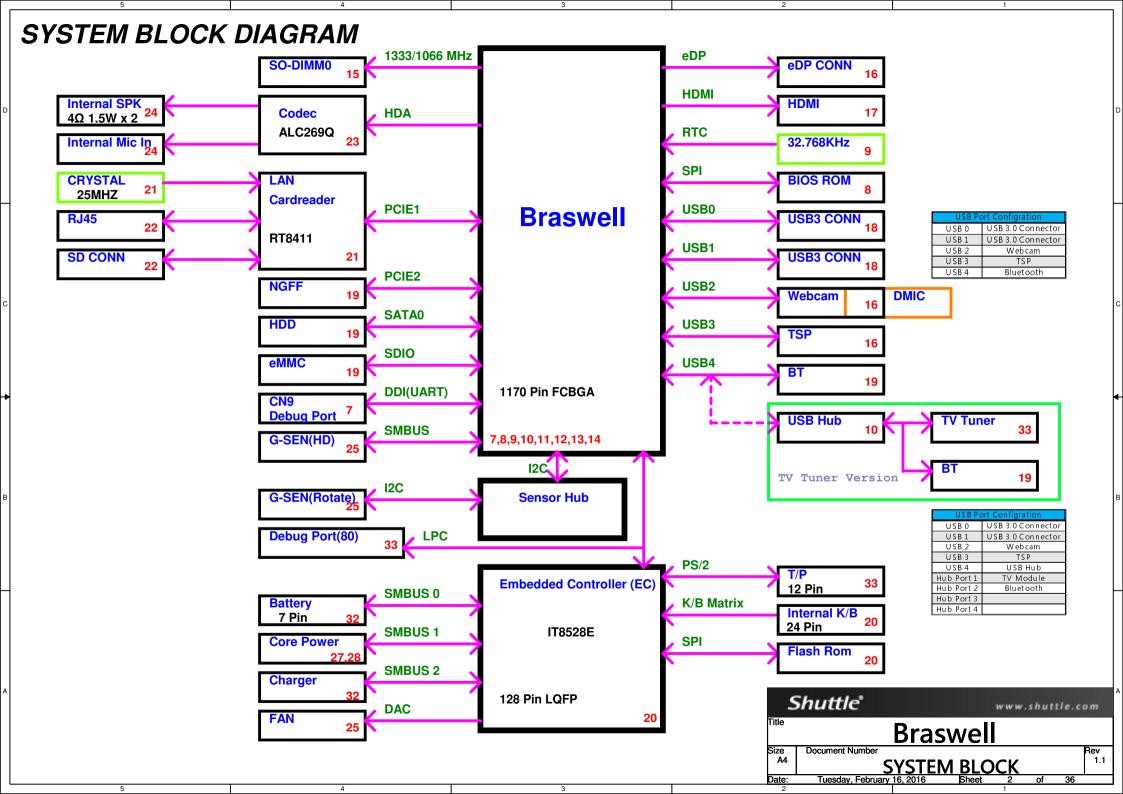
## M/B Schematic Version Change List

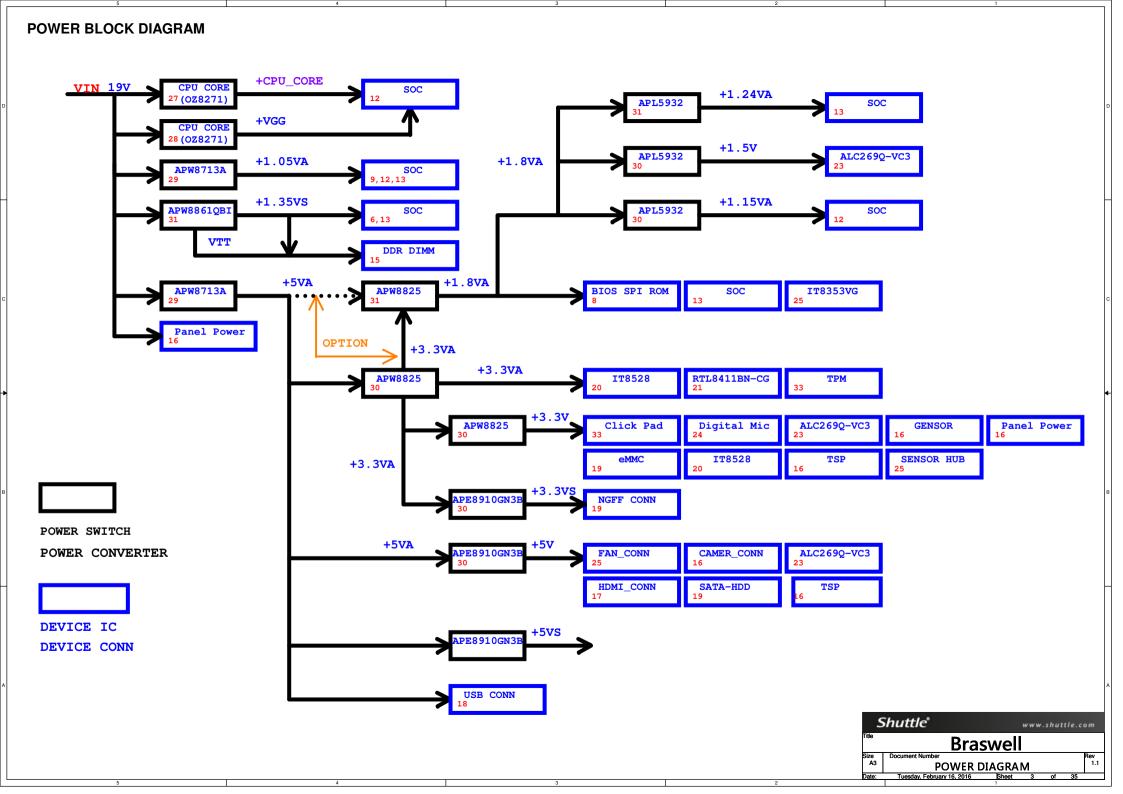
Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

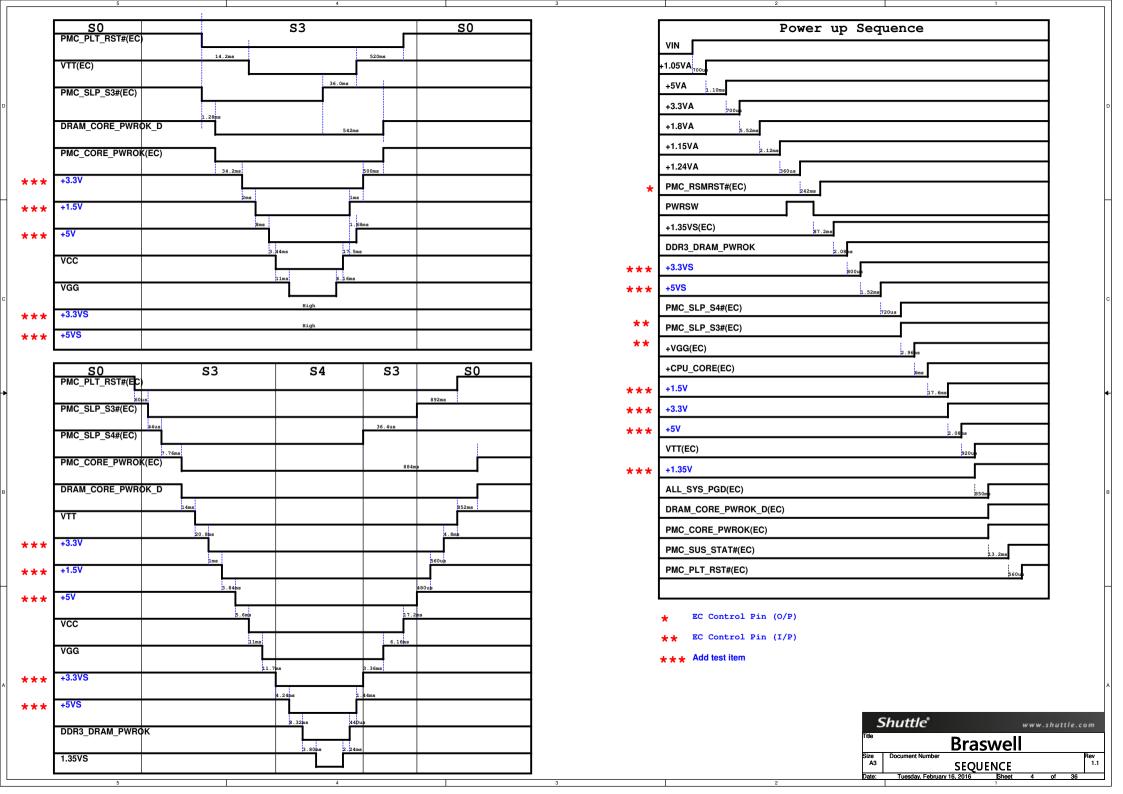
## **Daughter Board Schematic Version Change List**

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

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## **EC GPIO Table**

Port.A A 24 A1 25 A2 28 A3 29 A4 30 A5 31 A6 32 A7 34  B0 108 B1 109 B2 123 B3 110 B4 111 B5 126 B6 4 B7 112  Port.C C 115 C2 116 C3 56 C4 120 C5 57 C6 124 C7 16 C7 16 C9 129 Port.D 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	PWM0/GPA0(Up)  PWM1/GPA1(Up)  PWM2/GPA2(Up)  PWM3/GPA3(Up)  PWM4/GPA4(Up)	BATT_VA_O FF# BTL_BEEP	0	
Port.A  A2 28  A3 29  A4 30  A5 31  A6 32  A7 34   B0 108  B1 109  B2 123  B3 110  B4 111  B5 126  B6 4  B7 112  Port.C  C3 16  C4 120  C5 57  C6 124  C7 16  C7 16  C9 121  C	PWM2/GPA2(Up)  PWM3/GPA3(Up)  PWM4/GPA4(Up)			
Port.A A3 29 A4 30 A5 31 A6 32 A7 34  B1 109 B2 123 B3 110 B4 111 B5 126 B6 4 B7 112 C1 115 C2 116 C3 56 C4 120 C5 57 C6 124 C7 16 C7 16 C7 16  D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	PWM3/GPA3(Up) PWM4/GPA4(Up)	BTL BEEP	1 '	PD
Port.A  A4 30  A5 31  A6 32  A7 34  B0 108  B1 109  B2 123  B3 110  B4 111  B5 126  B6 4  B7 112  A 115  C2 116  C3 56  C4 120  C5 57  C6 124  C7 16  D0 18  D1 21  D2 22  D3 23  D4 15  D5 33  D6 47  D7 48	PWM4/GPA4(Up)	·	0	N C
A4 30 A5 31 A6 32 A7 34  B0 108 B1 109 B2 123 B3 110 B4 111 B5 126 B6 4 B7 112  C0 119 C1 115 C2 116 C3 56 C4 120 C5 57 C6 124 C7 16 C7 16 D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	· ·	OZ8690_CEN	0	N C
A6 32 A7 34  B0 108 B1 109 B2 123 B3 110 B4 111 B5 126 B6 4 B7 112  Port.C C3 56 C4 120 C5 57 C6 124 C7 16  D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48		+1.8V_ON	0	N C
Port.B  A7 34  B0 108  B1 109  B2 123  B3 110  B4 111  B5 126  B6 4  B7 112  C1 115  C2 116  C3 56  C4 120  C5 57  C6 124  C7 16  D0 18  D1 21  D2 22  D3 23  D4 15  D5 33  D6 47  D7 48	PWM5/GPA5(Up)	SENBAT_V	0	PD
Port.B B1 109 B2 123 B3 110 B4 111 B5 126 B6 4 B7 112  C1 115 C2 116 C3 56 C4 120 C5 57 C6 124 C7 16 D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	PWM6/SSCK/GPA6(Up)	PM C_RSM RST#	0	PD
Port.B    B1   109     B2   123     B3   110     B4   111     B5   126     B6   4     B7   112     C1   115     C2   116     C3   56     C4   120     C5   57     C6   124     C7   16     D2   22     D3   23     D4   15     D5   33     D6   47     D7   48	PWM7/RIG1#/GPA7(Up)	EC_BL_PWM	0	NC
Port.B  B2 123  B3 110  B4 111  B5 126  B6 4  B7 112  C1 115  C2 116  C3 56  C4 120  C5 57  C6 124  C7 16  D0 18  D1 21  D2 22  D3 23  D4 15  D5 33  D6 47  D7 48	RXD/SIN 0/GPB0(Up)	PM_SLP_S4#	I	PU
Port.B    B3	TXD/SOUTO/GPB1(Up)	PM_SLP_S3#	I	PU
Port.B  B4 111  B5 126  B6 4  B7 112  C0 119  C1 115  C2 116  C3 56  C4 120  C5 57  C6 124  C7 16  D0 18  D1 21  D2 22  D3 23  D4 15  D5 33  D6 47  D7 48	CTX0/TMA0/GPB2(Dn)	CPU_BL_O N_RT D_DET	I	PU
B4 111 B5 126 B6 4 B7 112  C0 119 C1 115 C2 116 C3 56 C4 120 C5 57 C6 124 C7 16  D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	SM CLK0/GPB3(X)	BAT_SMBCLK	0	N C
B6 4 B7 112  C0 119 C1 115 C2 116 C3 56 C4 120 C5 57 C6 124 C7 16  D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	SMDAT0/GPB4(X)	BAT_SMBDAT	IO	PU
B7 112  C0 119 C1 115 C2 116 C3 56 C4 120 C5 57 C6 124 C7 16  D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	GA20/GPB5(X)	RT C_RST	0	PD
Port.D   C0   119   C1   115   C2   116   C3   56   C4   120   C5   57   C6   124   C7   16   C7   16   C9   C9   C9   C9   C9   C9   C9   C	KBRST#/GPB6(X)	+3.3V	I	PU
Port.C C1 115 C2 116 C3 56 C4 120 C5 57 C6 124 C7 16 D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	RIN G#/PWR FAIL#/CK 3 2K OUT/LPCR ST#/GPB 7(Dn)	SAFTY_PROTECT	0	PD
Port.C C3 56 C4 120 C5 57 C6 124 C7 16 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	CRX0/GPC0(Dn)	LAN_PWR_ON	0	NC
Port.C C3 56 C4 120 C5 57 C6 124 C7 16 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	SM CLK1/GPC1(X)	SMB_CLK_EC	0	PU
Port.C  C4 120  C5 57  C6 124  C7 16  D0 18  D1 21  D2 22  D3 23  D4 15  D5 33  D6 47  D7 48	SMDAT1/GPC2(X)	SMB_DATA_EC	IO	PU
C4 120 C5 57 C6 124 C7 16 D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	KSO16/SMOSI/GPC3(Dn)			
C6 124 C7 16  D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	TMRI0/WUI2/GPC4(Dn)			
C7 16  D0 18  D1 21  D2 22  D3 23  D4 15  D5 33  D6 47  D7 48	KSO17/SMISO/GPC5(Dn)	1.5V_3.3V_5V_ON	0	N C
Port.D D0 18 D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	TMRI1/WUI3/GPC6(Dn)	PANEL_3.3V_ON	0	NC
Port.D D1 21 D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	PWUREQ#/BBO/SMCLK2ALT/GPC7(Up)	+1.35VS_ON	0	NC
Port.D D2 22 D3 23 D4 15 D5 33 D6 47 D7 48	RI1#/WUI0/GPD0(Up)	ADAP_IN	I	PD
Port.D D3 23 D4 15 D5 33 D6 47 D7 48	RI2#/WUI1/GPD1(Up)	PWRBTN#	0	NC
Port.D D4 15 D5 33 D6 47 D7 48	LPCRST#/WUI4/GPD2(Up)	PLT_RST#	I	PU
D4 15 D5 33 D6 47 D7 48	ECSCI#/GPD3(Up)	SM C_W A KE_SCI#	0	NC
D6 47 D7 48	ECSMI#/GPD4(Up)	EC_EXT SM I#	0	PU
D7 48	GINT/CTS0#/GPD5(Up)	CPU_LCDVDD_EN_EC_DET	I	PU
	TACH0A/GPD6(Dn)	FAN_RPM	I	N C
E0 19	TACH1A/TMA1/GPD7(Dn)	PWR_USB#	0	PU
i	L80HLAT/BAO/WUI24/GPE0(Dn)	LID#	I	PU
E1 82	EGAD/WUI25/GPE1(Dn)	+1.05VA_ON	0	N C
E2 83	EGCS#/WUI26/GPE2(Dn)	ALL_SYS_PGD	0	NC
Port.E E3 84	EGCLK/WUI27/GPE3(Dn)	VCORE_ON	0	NC
E4 125	PWRSW/GPE4(Up)	PWRSW	I	PU
E5 35	RT S1#/WUI5/GPE5(Dn)	LVDS_VIN	0	NC
E6 17	K1 31#/ W 013/ GF E3 (DII)	WLAN_ON	0	PD

Port		PIN	Pin Name	Net Name	I/O	PU/PD
F0		85	PS2CLK0/TMB0/GPF0(Up)			
	F1	86	PS2DAT0/TMB1/GPF1(Up)	TXE_DISABLE	0	NC
	F2	87	PS2CLK1/DTR0#/GPF2(Up)	BT_ON	0	PU
D E	F3	88	PS2DAT1/RTS0#/GPF3(Up)			
Port.F	F4	89	PS2CLK2/WUI20/GPF4(Up)	TP_CLK	0	NC
	F5	90	PS2DAT2/WUI21/GPF5(Up)	TP_DATA	IO	NC
	F6	117	PECI/SMCLK2/WUI22/GPF6(Up)	CHG_SM CLK	0	NC
	F7	118	SMDAT2/WUI23/GPF7(Up)	CHG_SMDATA	IO	NC
	G0	106	SSCE1#/GPG0(X)			
Port.G	G1	107	DTR1#/SBUSY/GPG1/ID7(Dn)	+3.3VS_5VS_ON	0	NC
POIL.G	G2	100	SSCE0#/GPG2(X)			
	G6	104	DSR0#/GPG6(X)	WEBCAM_ON	0	NC
	H0	93	CLKRUN#/WUI16/GPH0/ID0(Dn)	PLATFORM_ID1	I	PD
	Н1	94	CRX1/WUI17/SIN1/SMCLK3/GPH1/ID1(Dn)	PID_1_CHG_R_LED	0	NC
	Н2	95	CTX1/WUI18/SOUT1/GPH2/SMDAT3/ID2(Dn)	PID_2_PWR_LED	0	NC
Port.H	Н3	96	HSCE#/WUI1 9/GPH3/ID3(Dn)	VGG_ON	0	NC
	H4	97	HSCK/GPH4/ID4(Dn)	PLATFORM_ID2	I	PD
	Н5	98	HMISO/GPH5/ID5(Dn)	PLATFORM_ID3	I	PD
	H6	99	HMOSI/GPH6/ID6(Dn)	eMMC_RST	0	PU
	10	66	ADC0/GPI0(X)	PLATFORM_ID4	I	PD
	I1	67	ADC1/GPI1(X)	Angle_ID1	I	PU
	I2	68	ADC2/ GPI2(X)	PCIE_WAKE#	I	PU
D+ I	I3	69	ADC3/GPI3(X)	Angle_ID2	I	NC
P ort.I	I4	70	ADC4/WUI28/GPI4(X)	BAT_I	I	NC
	I5	71	ADC5/DCD1#/WUI29/GPI5(X)	BATT_TEMP	I	PU
	I6	72	ADC6/DSR1#/WUI30/GPI6(X)	ADAPTOR_I	I	NC
	17	73	ADC7/CTS1#/WUI31/GPI7(X)	BAT_V	I	PU
	10	76	TACH2/GPJ0(X)	EC_BL_ON	0	NC
	J1	77	GPJ1 (X)	EC_PROCHOT	0	PD
D 41	J2	78	DAC2/TACH0B/GPJ2(X)	FAN_CTRL0	0	NC
PortJ	J3	79	DAC3/TACH1B/GPJ3(X)	VTT_ON	0	NC
	J4	80	DAC4/DCD0#/GPJ4(X)	CHG_REF	0	NC
	J5	81	DAC5/RIG0#/GPJ5(X)		0	NC
	M.0	10	LAD0/GPM0(X)	LPC_AD0_EC	IO	NC
	M.1	9	LAD1/GPM1(X)	LPC_AD1_EC	IO	NC
	M.2	8	LAD2/GPM2(X)	LPC_AD2_EC	IO	NC
Port.M	M.3	7	LAD3/GPM3(X)	LPC_AD3_EC	IO	NC
	M.4	13	LPCCLK/GPM4(X)	CLK_EC_LPC	I	NC
	M.5	6	LFRAME#/GPM5(X)	LPC_FRAME#	I	NC

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