# PWM calculations

The master clock is 48 MHz, which could be used to clock the PWM as is or through dividers.

But we want to clock the PWM as fast as possible to get the largest possible dynamic range. If we clock the PWM with MCLK directly, we can have a sampling frequency of 46875 Hz with a dynamic range of 10 bits by using 1024 as the period count.

Note that the SAM7S64 has a minimum allowed duty cycle count of 2, so the actual dynamic range is 2-1023.