1.

a. **Hostname**: ece000.ece.local.cmu.edu

b. **Vendor ID**: GenuineIntel
Model name: Intel(R) Xeon(R) CPU E5-2620 v3 @ 2.40GHz

c. **Base frequency**: 2.40 GHz
CPU Max MHz: 3200
CPU Min MHz: 1200

d. **Cores per socket**: 6
Number of Sockets: 2
Number of physical cores: 12

e. **Threads per core**: 2
Number of physical cores: 12
Number of hardware threads: 24

f. Number of caches: 4

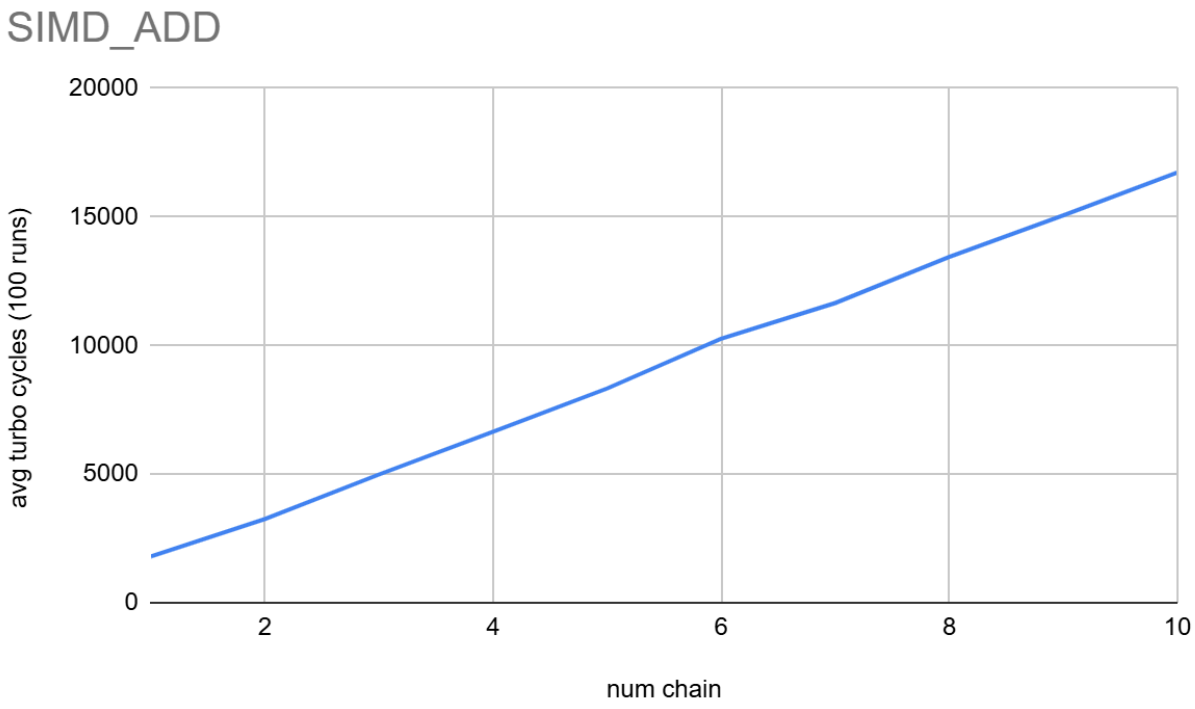
g. **L1d cache**: 32K
L1i cache: 32K
L2 cache: 256K
L3 cache: 15360K

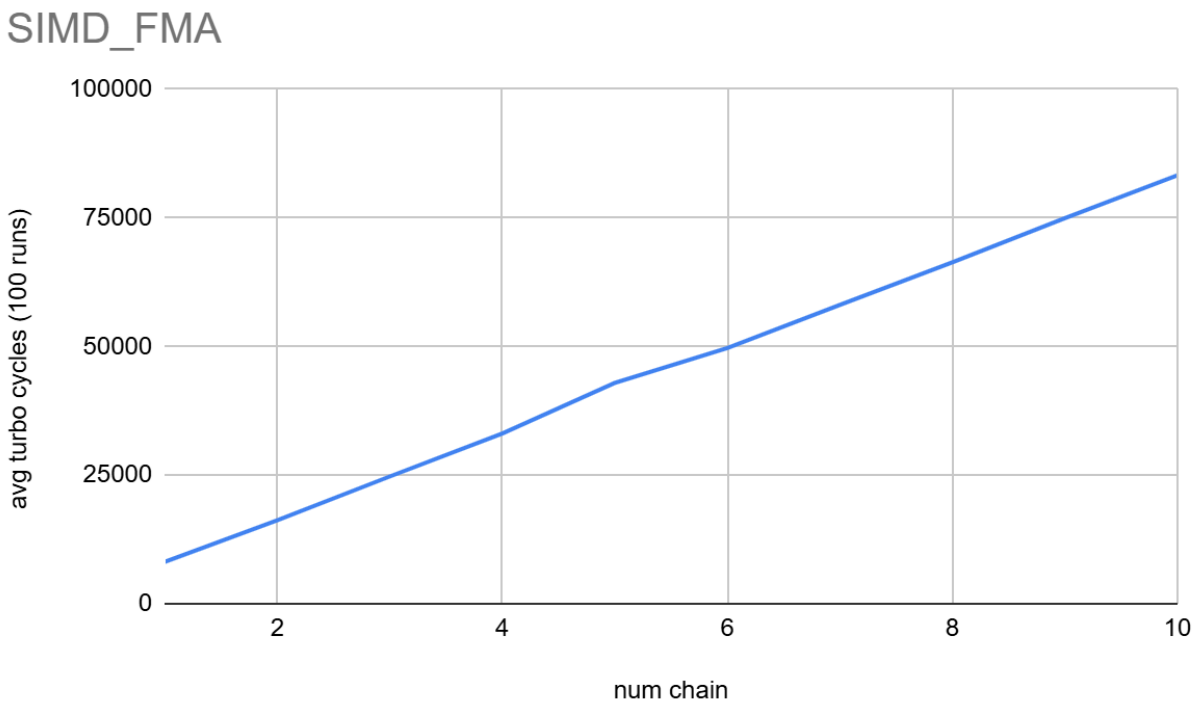
2.

a. **Scalar Multiplication (imul)**: 7.594667
b. **SIMD Addition (vaddpd)**: 14.114133
c. **SIMD Fused multiply-add (vfmadd231pd)**: 21.760000

3.

a. **SIMD Addition (vaddpd)**: 0.390951
b. **SIMD Fused multiply-add (vfmadd231pd)**: 0.078610
c. See the charts below:





In order to find the throughput, we need to compute the time in cycles for one instruction chain to finish. We then gradually increase the number of independent instruction chains and interleave them, until the execution time increases

significantly. Then, throughput is equal to the number of instruction per chain multiplied by the number of chains, over the number of cycles it take for all the instructions to finish.

d. According to the figures above, as the number of instruction chains increases, the number of cycles it takes for the instructions to finish increases linearly. Even after interleaving 10 independent instrction chains, there is still no sudden increase in the number of cycles it take for the instructions to finish. This indicates that The machine very likely only has one function unit for SIMD_ADD and SIMD_FMA.

4.

a. Around 5 hours.