University of Central Florida

Department of Computer Science

CDA 5106: Fall 2023

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Machine Problem 1: Cache Design, Memory Hierarchy Design

by

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Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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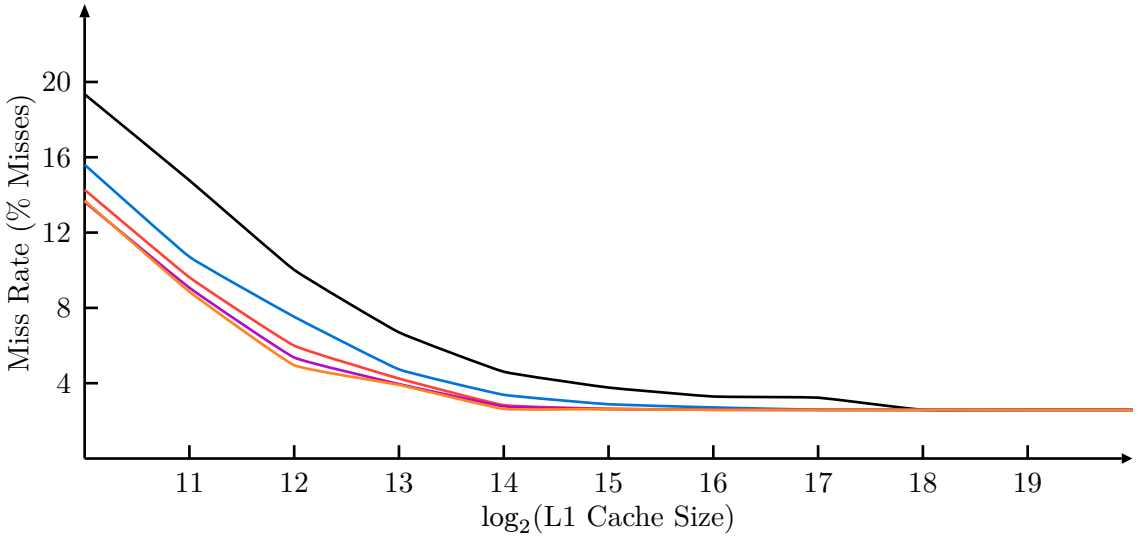
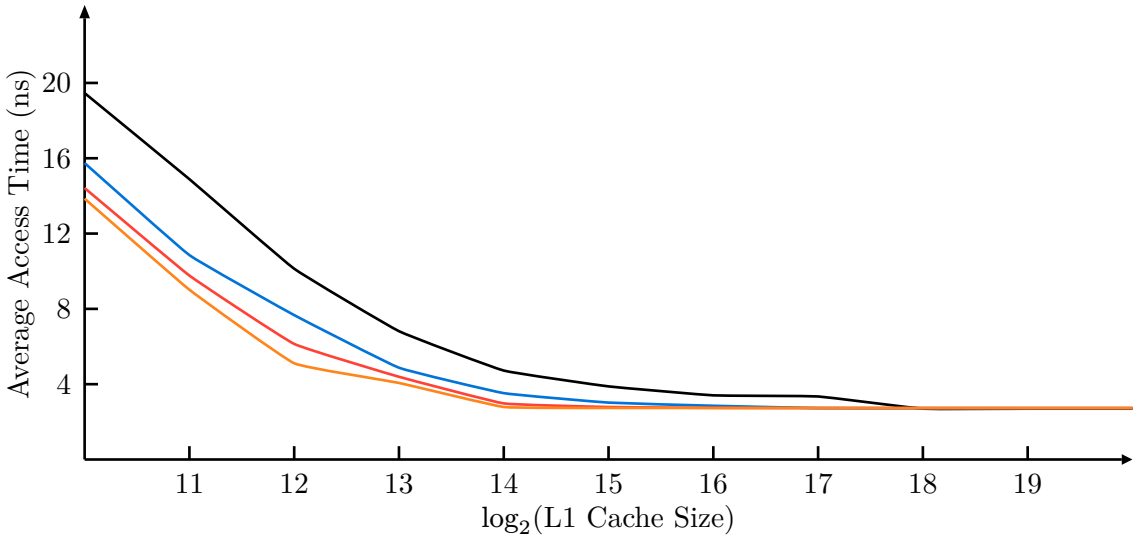
1. L1 Cache Exploration: Size and Associativity



Graph 1: Relation between cache size, associativity, and miss rate



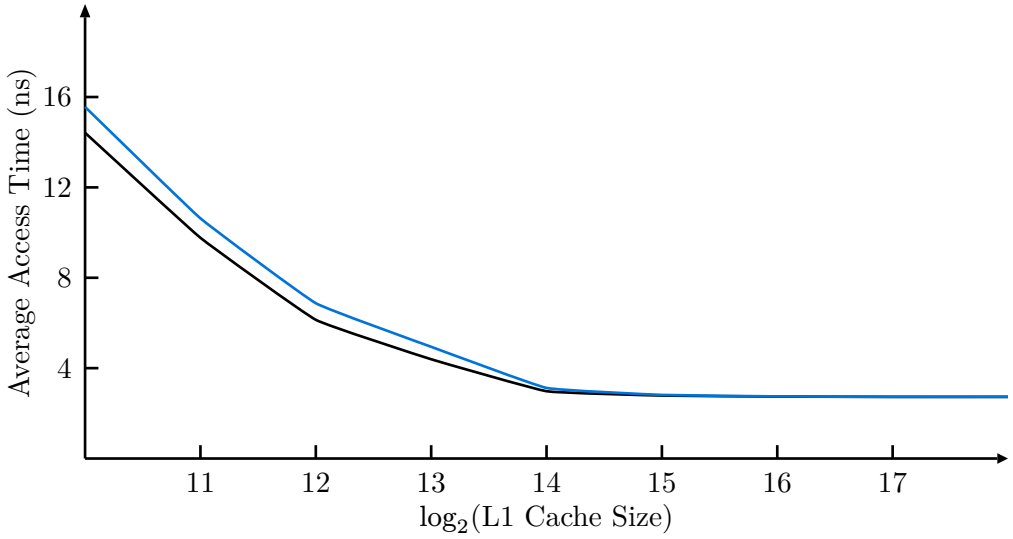
Graph 2: Relation between cache size, associativity, and average access time

Associativity is color coded with an associativity of 1 being colored black, 2 being colored blue, 4 being colored red, 8 being colored purple, and fully-associative cache being colored orange.

As the associativity of the cache grows, the miss rate decreases. Similarly, as the size of the cache grows, the miss-rate decreases. Both have limited gains, and regardless of the associativity, the miss rate converges to 2.582% as the cache size reaches a size of 2^{18}.

The compulsory cache miss rate appears to be 2.582% as that is the miss rate as the cache size grows. For each associativity, 1; 2; 4; 8; and full, the conflict miss rates appear to be 16.762%, 13.021%, 11.688%, 11.045%, and 11.114% respectively. For any given cache size, the best AAT will either be fully associative or tied with fully associative regardless of cache size.

2. Replacement Policy Study

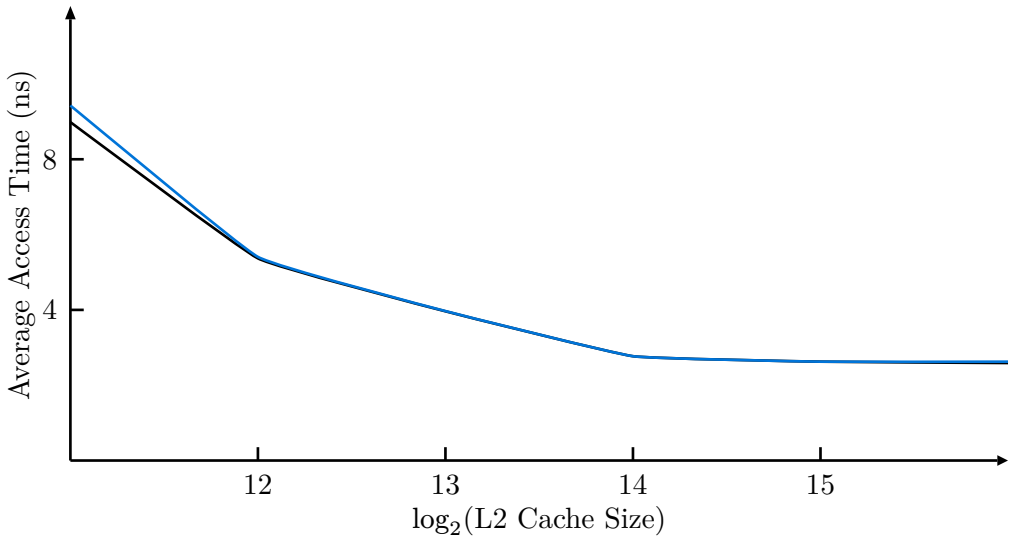


Graph 3: Relation between cache size, associativity, and miss rate

The line for cache with LRU replacement policy is colored black and the line for cache with FIFO replacement policy is colored blue.

Until both policies converge as the cache size reaches a large size, the LRU policy has a lower average access time. Therefore, LRU is the better policy.

3. Inclusion Property Study



Graph 4: Relation between cache size, associativity, and miss rate

The line for cache with non-inclusive inclusion property is colored black and the line for cache with inclusive inclusion property is colored blue.

The non-inclusive inclusion property yields equivalent or better average access times by a minor margin which diminishes to near 0 as the size of the L2 cache grows.