DW_fp_sum4

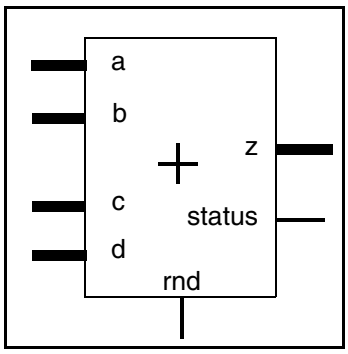
4-Input Floating-Point Adder

Version, STAR, and myDesignWare Subscriptions: IP Directory

Features and Benefits

Revision History

- The precision is controlled by parameters, and covers formats in the IEEE standard
- Exponents can range from 3 to 31 bits
- Fractional part of floating-point number ranges from 2 to 253 bits
- A parameter controls the use of denormal values
- Faster than an equivalent logic using three FP adders for some parameter values
- Result is always more accurate than using three FP adders



Description

DW_fp_sum4 is a floating-point component that is capable of adding four floating-point values, `a`, `b`, `c`, and `d`, to produce a floating-point result `z`. This component generates results with more accuracy than independent FP additions, given that only one rounding computation is done, and special conditions on the inputs can be detected and corrected.

For the case of zero result, when *ieee_compliance* = 0, the sign of a zero result is negative when rounding to –infinity (`rnd` = 3), and positive for any other rounding mode. When *ieee_compliance* = 1, the following is the behavior for the sign of zero:

1. When the zero output is a result of the addition of zero inputs (all inputs are zeros), the sign of the zero output depends on the rounding mode:
   - Rounding to –infinity (`rnd` = 3): the output is +0 when all the inputs are +0, otherwise, it is -0.
   - Other rounding modes: the output is -0 when all the inputs are -0, otherwise, it is +0.
2. When the zero output is a result of the addition of non-zero inputs, the output is -0 when the rounding mode is –infinity (`rnd` = 3), otherwise the output is +0.

Component pins are described in Table 1-1 and configuration parameters are described in Table 1-2.

Table 1-1 Pin Description

Pin Name	Width	Direction	Function
a	(*sig_width* + *exp_width* + 1) bits	Input	Input data
b	(*sig_width* + *exp_width* + 1) bits	Input	Input data
c	(*sig_width* + *exp_width* + 1) bits	Input	Input data

Table 1-1 Pin Description (Continued)

Pin Name	Width	Direction	Function
d	(*sig_width* + *exp_width* + 1) bits	Input	Input data
z	(*sig_width* + *exp_width* + 1) bits	Output	((a + b) + c) + d
status	8 bits	Output	Status flags for the result z For details, see STATUS Flags in the *Datapath Floating-Point Overview.*
rnd	3 bits	Input	Rounding mode; supports all rounding modes described in the *Datapath Floating-Point Overview*;

Table 1-2 Parameter Description

Parameter	Values	Description
sig_width	2 to 253 bits	Word length of fraction field of floating-point numbers a, b, c, d, and z
exp_width	3 to 31 bits	Word length of biased exponent of floating-point numbers a, b, c, d, and z
ieee_compliance	0 or 1	Level of support for IEEE 754: ■ 0: No support for IEEE 754 NaNs and denormals; NaNs are considered infinities and denormals are considered zeros ■ 1: Fully compliant with the IEEE 754 standard, including support for NaNs and denormals For more, see IEEE 754 Compatibility in the *Datapath Floating-Point Overview*.
arch_type	0 or 1	Controls the use of an alternative architecture Default value is 0 (previous architecture)

Table 1-3 Synthesis Implementations

Implementation Name	Function	License Feature Required
rtl	Synthesis model	DesignWare

Table 1-4 Simulation Models

Model	Function
DW02.DW_FP_SUM4_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_fp_sum4_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_fp_sum4.v	Verilog simulation model source code

Table 1-5 Functional Description

a	b	c	d	status[a]	z[b]
a (FP)	b (FP)	c (FP)	d (FP)	*	a + b + c + d (FP)

a. The details of `status` flags, if used, can be found in Table 9 of the *Datapath Floating-Point Overview*.
b. The actual value of the result is defined by the rounding mode.

The parameters *ieee_compliance* and *arch_type* control the functionality of this component. Different values of *arch_type* result in slightly different numeric behaviors, but in any case, the component is more accurate than the implementation of the same function using basic floating-point adders.

When the parameter *arch_type* = 0, the component provides an output that is independent of the input order. This feature implies that the operation is done as if infinite precision was internally used, and only at the end the rounding operation is performed to obtain the final result.

When *arch_type* = 1, the component is sensitive to the input order, in the same way that a tree of FP adders would be, when configured as ((`a` + `b`) + (`c` + `d`)). Only one rounding operation is performed to compute the output value. The logic produced by this component when *arch_type* = 1 is smaller and faster than when *arch_type* = 0. This configuration is faster or competitive with a network of three FP adders, with superior accuracy.

When the parameter *ieee_compliance* = 0, the component considers denormal values as zeros and NaN values as infinity. When *ieee_compliance* = 1, the component operates with denormals and NaNs as described in the IEEE Standard 754.

For more information about the floating-point system defined for all the DW_fp components, including `status` flag bits, and integer and floating-point formats, refer to the *Datapath Floating-Point Overview*.

Suppressing Warning Messages During Verilog Simulation

The Verilog simulation model includes macros that allow you to suppress warning messages during simulation.

To suppress all warning messages for all DWBB components, define the DW_SUPPRESS_WARN macro in either of the following ways:

- Specify the Verilog preprocessing macro in Verilog code:

  ```
  `define DW_SUPPRESS_WARN
  ```

- Or, include a command line option to the simulator, such as:

  `+define+DW_SUPPRESS_WARN` (which is used for the Synopsys VCS simulator)

The warning messages for this model include the following:

- If an invalid rounding mode has been detected on `rnd`, the following message is displayed:

  ```
  WARNING: <instance_path>:
      at time = <timestamp>: Illegal rounding mode.
  ```

  To suppress this message, use the DW_SUPPRESS_WARN macro explained earlier.

Related Topics

- Datapath – Floating-Point Overview
- DesignWare Building Block IP User Guide

HDL Usage Through Component Instantiation - VHDL

```
library IEEE,DWARE;
use IEEE.std_logic_1164.all;
use DWARE.DW_Foundation_comp_arith.all;

entity DW_fp_sum4_inst is
      generic (
        inst_sig_width : POSITIVE := 23;
        inst_exp_width : POSITIVE := 8;
        inst_ieee_compliance : INTEGER := 0;
        inst_arch_type : INTEGER := 0
        );
      port (
        inst_a : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        inst_b : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        inst_c : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        inst_d : in std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        inst_rnd : in std_logic_vector(2 downto 0);
        z_inst : out std_logic_vector(inst_sig_width+inst_exp_width downto 0);
        status_inst : out std_logic_vector(7 downto 0)
        );
    end DW_fp_sum4_inst;


architecture inst of DW_fp_sum4_inst is

begin

    -- Instance of DW_fp_sum4
    U1 : DW_fp_sum4
    generic map (
          sig_width => inst_sig_width,
          exp_width => inst_exp_width,
          ieee_compliance => inst_ieee_compliance,
          arch_type => inst_arch_type
          )
    port map (
          a => inst_a,
          b => inst_b,
          c => inst_c,
          d => inst_d,
          rnd => inst_rnd,
```

```
            z => z_inst,
            status => status_inst
            );


end inst;

-- pragma translate_off
configuration DW_fp_sum4_inst_cfg_inst of DW_fp_sum4_inst is
 for inst
 end for; -- inst
end DW_fp_sum4_inst_cfg_inst;
-- pragma translate_on
```

HDL Usage Through Component Instantiation - Verilog

```
module DW_fp_sum4_inst( inst_a, inst_b, inst_c, inst_d, inst_rnd,
          z_inst, status_inst );

parameter inst_sig_width = 23;
parameter inst_exp_width = 8;
parameter inst_ieee_compliance = 0;
parameter inst_arch_type = 0;


input [inst_sig_width+inst_exp_width : 0] inst_a;
input [inst_sig_width+inst_exp_width : 0] inst_b;
input [inst_sig_width+inst_exp_width : 0] inst_c;
input [inst_sig_width+inst_exp_width : 0] inst_d;
input [2 : 0] inst_rnd;
output [inst_sig_width+inst_exp_width : 0] z_inst;
output [7 : 0] status_inst;

    // Instance of DW_fp_sum4
    DW_fp_sum4 #(inst_sig_width, inst_exp_width, inst_ieee_compliance, inst_arch_type)
U1 (
                .a(inst_a),
                .b(inst_b),
                .c(inst_c),
                .d(inst_d),
                .rnd(inst_rnd),
                .z(z_inst),
                .status(status_inst) );

endmodule
```

Revision History

For notes about this release, see the *DesignWare Building Block IP Release Notes*.

For lists of both known and fixed issues for this component, refer to the STAR report.

For a version of this datasheet with visible change bars, click here.

Date	Release	Updates
July 2020	DWBB_201912.5	■ Adjusted the description of the *ieee_compliance* parameter in Table 1-2 on page 2 ■ Added "Suppressing Warning Messages During Verilog Simulation" on page 3 ■ Added this Revision History table and the document links on this page

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