FSA0M_A
UMC 0.18 µm Mixmode/RFCMOS Process

MEMAKER

Overview
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Chapter 1

Synchronous Dual-Port SRAM Compiler Overview

This chapter contains the following sections:

- 1.1 Description
- 1.2 Features
- 1.3 Logic Symbol & Recommended Operating Conditions
- 1.4 Physical Attributes
- 1.5 Timing Diagram
- 1.6 Configuration Ranges
- 1.7 Pin Description

1.1 Description

The FSA0M_A_SJ is a synchronous dual-port SRAM compiler. It is created according to UMC's 0.18 µm Mixmode/RFCMOS process design rules and can be incorporated with Faraday's 0.18 µm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configuration.

Given the desired size and timing constraints, the FSA0M_A_SJ compiler is capable of providing the suitable synchronous RAM layout instances in minutes. It can automatically generate the data sheets, Verilog/VHDL behavioral simulation models, SCS or ViewLogic symbols, place & route models, and the test patterns to be used in the ASIC designs. The length of the duty cycle can be neglected as long as the setup/hold times and the minimum high/low pulse widths are satisfied. This allows a more flexible clock falling edge during each operation. Both the word write and byte write operations are supported.

1.2 Features

- Synchronous read and write operations
- Fully customized layout density
- Available in 1.8 V ± 10%
- Automatic power down to eliminate the DC current
- Clocked address inputs and CSA(B) to the RAM at the CKA(B) rising edge
- Clocked WEA(B)N input pins to the RAM at the CKA(B) rising edge
- Clocked DIA(B) input pins to the RAM at the CKA(B) rising edge
- Byte write or word write operations available
- Verilog/VHDL timing simulation model generator
- SPICE netlist generator
- Memaker preview UI
- BIST code supported
- Multi-block options of the best aspect ratio
- Minimum metal requirement: 5 metal layers

1.3 Logic Symbol & Recommended Operating Conditions

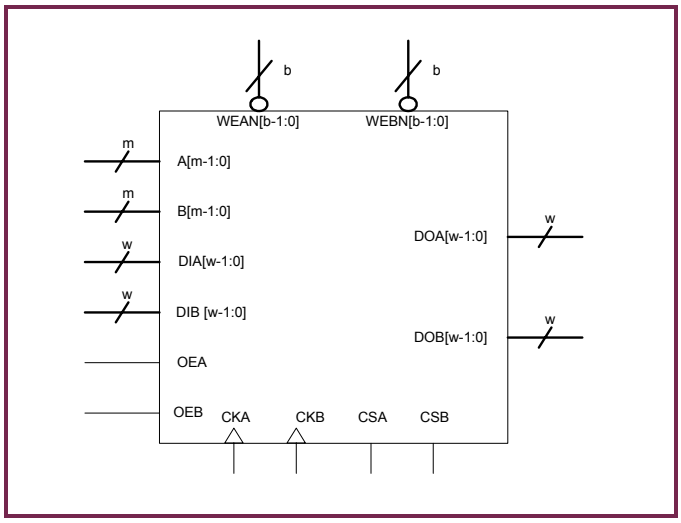

Figure 1-1. Logic Symbol of FSA0M_A_SJ

Table 1-1. Recommended Operating Conditions of FSA0M_A_SJ

Symbol	Description	Condition	Min	Typ	Max	Unit
VCC	Power supply	RAM power	1.62	1.8	1.98	V
VIL	Input low voltage	CMOS	-0.37	-	0.69	V
VIH	Input high voltage	CMOS	1.15	-	2.28	V
VOL	Output low voltage	CMOS	-	-	0.4	V
VOH	Output high voltage	CMOS	1.22	-	-	V
T_j	Operating junction temperature	-	-40	25	125	°C

1.4 Physical Attributes

Table 1-2. Physical Attributes of FSA0M_A_SJ

Structure	Gate process	Single gate
	Block layout metal usage	M1, M2, M3, M4
	Chip-level routing	M5, M6
	Antenna diode	Every input pin
Process metal options	5 metal layers	M5 (Thick) + M1 ~ M4 (Thin)
	6 metal layers	M6 (Thick) + M1 ~ M5 (Thin)

1.5 Timing Diagram

1.5.1 Read Cycle Timing Diagram (OEA [B] = High)

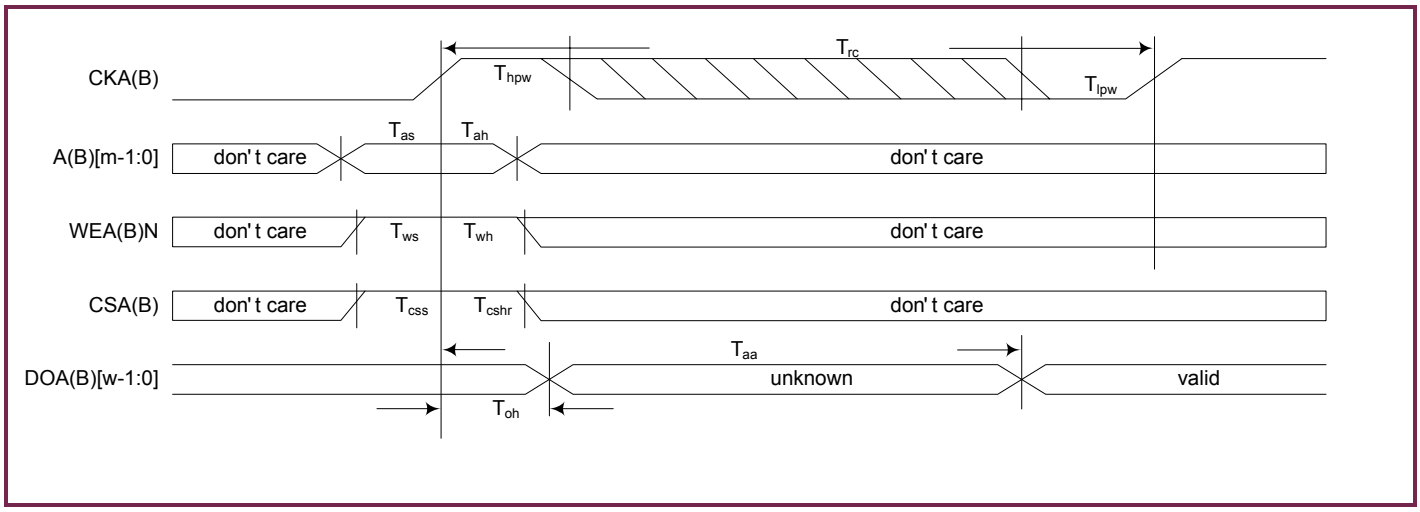

Figure 1-2. Read Cycle Timing Diagram of FSA0M_A_SJ

1.5.2 Read Cycle Timing Specifications

Table 1-3. Read Cycle Timing Specifications of FSA0M_A_SJ

Symbol	Description	Timing (ns)		Remarks
		1K x 16	4K x 16	
T_{aa}	Address access time from the CKA(B) rising edge	2.75	3.24	Minimum
T_{oh}	Output data hold time from the CKA(B) rising edge	1.24	1.47	Maximum
T_{rc}	Read cycle time	3.73	4.41	Minimum
T_{as}	Address setup time before the CKA(B) rising edge	1.24	1.24	Minimum
T_{ah}	Address hold time after the CKA (B) rising edge	0.19	0.19	Minimum
T_{ws}	WEA (B)N setup time before the CKA(B) rising edge	0.69	0.69	Minimum
T_{wh}	WEA(B)N hold time after the CKA(B) rising edge	0.13	0.13	Minimum
T_{css}	CSA(B) setup time before the CKA(B) rising edge	1.43	1.43	Minimum
T_{cshr}	CSA(B) hold time after the CKA(B) rising in read cycle	0.00	0.00	Minimum
T_{hpw}/T_{lpw}	Clock high/low pulse width	1.24	1.47	Minimum

Note: Operating under the worst case condition: 125 °C, 1.62 V with the 0.01 pf load and 0.02 ns input slew

1.5.3 Write Cycle Timing Diagram (OEA [B] = High)

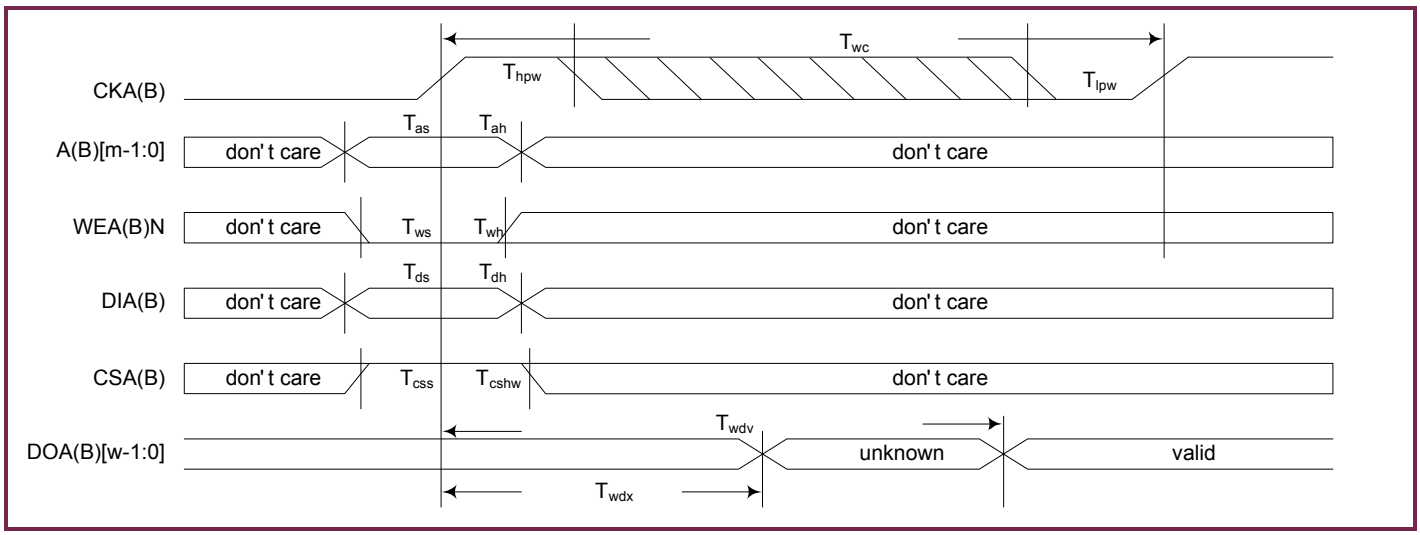

Figure 1-3. Write Cycle Timing Diagram of FSA0M_A_SJ

1.5.4 Write Cycle Timing Specifications

Table 1-4. Write Cycle Timing Specifications of FSA0M_A_SJ

Symbol	Description	Timing (ns)		Remarks
		1K x 16	4K x 16	
T_{wc}	Write cycle time	2.83	3.80	Minimum
T_{ws}	WEA (B)N setup time before the CKA (B) rising edge	0.69	0.69	Minimum
T_{wh}	WEA (B)N hold time after the CKA (B) rising edge	0.13	0.13	Minimum
T_{ds}	Input data setup time before the CKA (B) rising edge	0.29	0.29	Minimum
T_{dh}	Input data hold time after the CKA (B) rising edge	0.13	0.13	Minimum
T_{wdx}	Output data invalid from the CKA (B) rising edge	1.87	2.21	Maximum
T_{wdv}	Output data valid from the CKA (B) rising edge	1.32	1.55	Minimum
T_{css}	CSA (B) setup time before the CKA (B) rising edge	1.43	1.43	Minimum
T_{cshw}	CSA (B) hold time after the CKA (B) rising in the write cycle	0.00	0.00	Minimum

1.6 Configuration Ranges

Table 1-5. Word Range of FSA0M_A_SJ

Word Range	
Block option = 1	64, 80, …4080, 4096
Block option = 2	128, 160, …8160, 8192
Block option = 4	256, 320, …16320, 16384
Block option = 8	512, 640, …32640, 32768

Table 1-6. Bit Range of FSA0M_A_SJ

Bit Range	
Block option = 1	1, 2, …127, 128
Block option = 2	1, 2, …63, 64
Block option = 4	1, 2, …31, 32
Block option = 8	1, 2, …15, 16

Table 1-7. Byte Range of FSA0M_A_SJ

Byte Range		Remarks
Block option = 1	128, 127, …2, 1	Bit width * byte ≤ 128
Block option = 2	64, 63, …2, 1	Bit width * byte ≤ 64
Block option = 4	32, 31, …2, 1	Bit width * byte ≤ 32
Block option = 8	16, 15, …2, 1	Bit width * byte ≤ 16

1.7 Pin Description

Table 1-8. Pin Description of FSA0M_A_SJ

Pin Names	Pin Descriptions
CKA	Clock signal of the A port addresses, CSA, WEAN, and DIA, latched at the rising edge
CKB	Clock signal of the B port addresses, CSB, WEBN, and DIB, latched at the rising edge
A[m-1:0]	Address signals of the width m for the A port
B[m-1:0]	Address signals of the width m for the B port
DIA[w-1:0]	Input data of width w for the A port
DIB[w-1:0]	Input data of width w for the B port
OEA	Output enable signal of the A port, active high
OEB	Output enable signal of the B port, active high
CSA	Chip select of the A port, active high
CSB	Chip select of the B port, active high
WEAN[b-1:0]	Write enable signals of b bytes for the A port, active low
WEBN[b-1:0]	Write enable signals of b bytes for the B port, active low
DOA[w-1:0]	Output data of width w (tri-state) for the A port
DOB[w-1:0]	Output data of width w (tri-state) for the B port
CKA	Clock signal of the A port addresses, CSA, WEAN, and DIA, latched at the rising edge

Chapter 2

Synchronous Single-Port RAM Compiler Overview

This chapter contains the following sections:

- 1.1 Description
- 1.2 Features
- 1.3 Logic Symbol & Recommended Operating Conditions
- 1.4 Physical Attributes
- 1.5 Timing Diagram
- 1.6 Configuration Ranges
- 1.7 Pin Description

2.1 Description

The FSA0M_A_SU is a high density, synchronous single port RAM. It is implemented by using UMC 0.18 µm Mixmode/RFCMOS process technology and can be incorporated with Faraday's 0.18 µm standard cells. Different combinations of words, bits, and aspect ratios can be used to generate the most desirable configuration.

Given the desired size and timing constraints, the FSA0M_A_SU compiler is capable of providing suitable synchronous RAM layout instances in minutes. It automatically generates the data sheets, Verilog behavioral simulation models, SCS or ViewLogic symbols, place & route models, and test patterns to be used in the ASIC designs. The length of the duty cycle can be neglected as long as the setup/hold times and the minimum high/low pulse widths are satisfied. This allows a more flexible clock falling edge during each operation. Both word write and byte write operations are supported.

2.2 Features

- Synchronous read and write operations
- Fully customized layout density per customer configuration
- Available in 1.8 V ± 10%
- Automatic power down mechanism to eliminate the DC current
- Clocked address inputs and CS to RAM at CK rising edge
- Clocked WEB input pin to RAM at CK rising edge
- Clocked DI input pins to RAM at CK rising edge
- Byte write and word write operations available
- Tri-state buffer
- Verilog/VHDL timing simulation model generator
- SPICE netlist generator
- GDSII layout database
- Memaker preview UI
- BIST code supported
- Multi-block options for the best aspect ratio

2.3 Logic Symbol & Recommended Operating Conditions

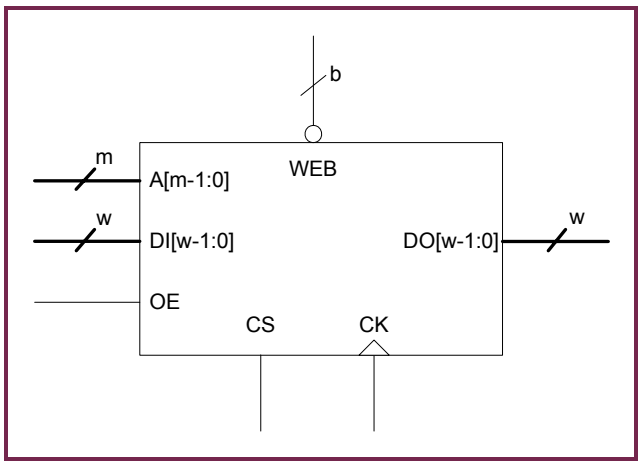

Figure 2-1. Logic Symbol of FSA0M_A_SU

Table 2-1. Recommended Operating Conditions of FSA0M_A_SU

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VCC	Power supply	RAM power	1.62	1.8	1.98	V
V_{IL}	Low input voltage	CMOS	-0.3		0.69	V
V_{IH}	High input voltage	CMOS	1.05		2.28	V
V_{OL}	Low output voltage	CMOS			0.4	V
V_{OH}	High output voltage	CMOS	1.22			V
T_J	Operating junction temperature		-40	25	125	℃

2.4 Physical Attributes

Table 2-2. Physical Attributes of FSA0M_A_SU

Structure	Gate process	Single gate
	Block layout metal usage	M1, M2, M3, M4
	Chip-level routing	M5, M6
	Antenna diode	Provided for every input pin
Process metal option	Five (5) metal layers	M5 (thick) + M1 ~ M4 (thin)
	Six (6) metal layers	M6 (thick) + M1 ~ M5 (thin)

2.5 Timing Diagram

2.5.1 Read Cycle Timing Diagram (OE = High)

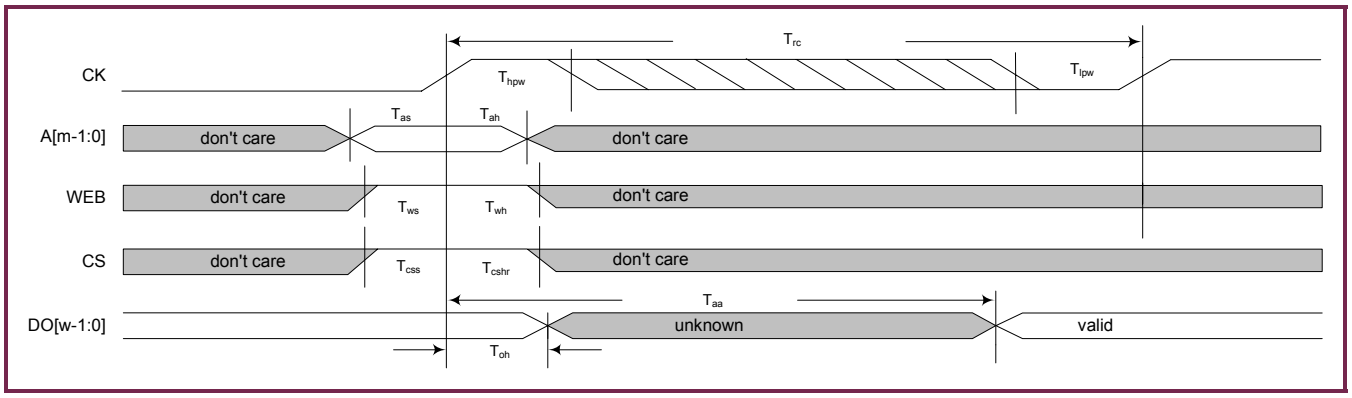

Figure 2-2. Read Cycle Timing Diagram of FSA0M_A_SU

2.5.2 Read Cycle Timing Specifications

Table 2-3. Read Cycle Timing Specifications of FSA0M_A_SU

Symbol	Description	Timing (ns)[3]	Remark
		4K x 16	
T_{aa}	Data access time from the CK rising edge	3.52	Minimum
T_{oh}	Output data hold time after the CK rising edge	1.99	Maximum
T_{rc}	Read cycle time	4.14	Minimum
T_{as}	Address setup time before the CK rising edge	1.15	Minimum
T_{ah}	Address hold time after the CK rising edge	0.10	Minimum
T_{ws}	WEB setup time before the CK rising edge	0.82	Minimum
T_{wh}	WEB hold time after the CK rising edge	0.10	Minimum
T_{css}	CS setup time before the CK rising edge	1.44	Minimum
T_{cshr}	CS hold time after the CK rising edge in the read cycle	0.23	Minimum
Thpw/T_{lpw}	Clock high/low pulse width	0.77	Minimum

[3] Operating under the worst case condition, at 125 °C and 1.62 V

2.5.3 Write Cycle Timing Diagram (OE = High, CS = High)

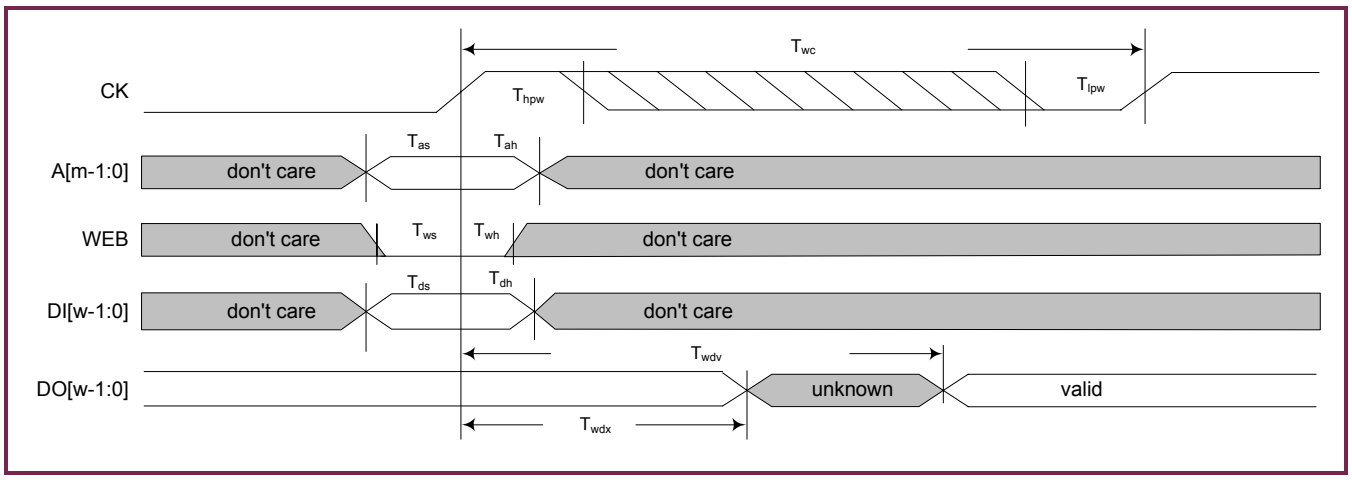

Figure 2-3. Write Cycle Timing Diagram of FSA0M_A_SU

2.5.4 Write Cycle Timing Specifications

Table 2-4. Write Cycle Timing Specifications of FSA0M_A_SU

Symbol	Description	Timing (ns)[4]	Remark
		4K x 16	
T_{wc}	Write cycle time	4.14	Minimum
T_{ds}	Input data setup time before the CK rising edge	1.01	Minimum
T_{dh}	Input data hold time after the CK rising edge	0.01	Minimum
T_{wdx}	Output data invalid after the CK rising edge	1.99	Maximum
T_{wdv}	Output data valid after the CK rising edge	2.64	Minimum

[4] Operating under the worst case condition, at 125 °C and 1.62 V

2.6 Configuration Ranges

Table 2-5. Word Range of FSA0M_A_SU

Word Range	
Block option = 1	64, 80, . . . , 4096
Block option = 2	128, 160, . . . , 8192
Block option = 4	256, 320, . . . , 16384
Blick option = 8	512, 640, . . . , 32768
Block option = 16	1024, 1280, . . . , 65536

Table 2-6. Bit Range of FSA0M_A_SU

Bit Range	
Block option = 1	1, 2, 3, . . . , 128
Block option = 2	1, 2, 3, . . . , 64
Block option = 4	1, 2, 3, . . . , 32
Block option = 8	1, 2, 3, . . . , 16
Block option = 16	1, 2, 3, . . . , 8

Table 2-7. Byte Range of FSA0M_A_SU

Byte Range		Remarks
Block option = 1	128, 127, . . . , 2, 1	Bit width * byte ≤ 128
Block option = 2	64, 63, . . . , 2, 1	Bit width * byte ≤ 64
Block option = 4	32, 31, . . . , 2, 1	Bit width * byte ≤ 32
Block option = 8	16, 15, . . . , 2, 1	Bit width * byte ≤ 16
Block option = 16	8, 7, . . . , 2, 1	Bit width * byte ≤ 8

2.7 Pin Description

Table 2-8. Pin Description of FSA0M_A_SU

Pin	Description
CK	Clock signal of the addresses, CS, WEB, and DI, latched at the rising edge
A[m-1:0]	Address signals of width m
DI[w-1:0]	Input data of width w
OE	Output enable signal, active high
CS	Chip select, active high
WEB[b-1:0]	Write enable signals of b bytes, active low
DO[w-1:0]	Output data of width w (Tri-state)

Chapter 3

Usage of Memory EDA Deliverables

This chapter contains the following sections:

- 3.1 Memory EDA Deliverable Items
- 3.2 Using Verilog Simulation Model
- 3.3 Using VHDL Simulation Model
- 3.4 Using Synopsys Synthesis Model
- 3.5 Using LEF P & R Model
- 3.6 Using P & R Model
- 3.7 Using TLF and CLF P & R Timing Model
- 3.8 Using LVS Netlist, GDSII Layout, and H-Cell List

3.1 Memory EDA Deliverable Items

Table 3-1. Memory EDA Deliverable Items

Deliverable Items	Description
Symbol	• EDIF • Synopsys
Simulation model (Front-end)	• Verilog • VHDL
Physical layout (Back-end)	• GDSII
P & R model (Back-end)	• Apollo FrameView • LEF
P & R timing model (Back-end)	TLF
Static timing analysis	STA (PrimeTime)
Synthesis model	Timing model of Synopsys synthesis
LVS netlist	SPICE netlist without capacitance
Command file	Chip level DRC and LVS command files (Dracula and Calibre)

Table 3-2. EDA Tool Versions

EDA Model	EDA Tool	Version
Synopsys	• Synopsys Library Compiler • Synopsys Design Compiler • Synopsys PrimeTime	2000.05
Verilog	Cadence Verilog-XL	2.7
VHDL	Mentor ModelTech ModelSim	5.4e
ECS	Cohesion Designer Series (ECS)	4.46
Cadence	Cadence DFII	4.4.3
	Cadence Dracula	4.7.09-1999
GDSII & Netlist	Mentor Calibre	8.7_28.1
LEF	Avant! Milkyway	2000.2.3.4.0.8.4

3.2 Using Verilog Simulation Model

After generating the Verilog model, please refer to the following steps to simulate the design model.

Step 1: Check the syntax of the Verilog model:

verilog <name.v>

Where ***<name>.v*** is the Verilog model.

Step 2: The functional simulation can be accomplished in your test bench where the model is instantiated.

Verilog +define+functional test-bench

Step 3: Run the simulator:

verilog <test-bench>.v

The simulation output is written to the file, verilog.log, which is saved in the current working directory.

3.3 Using VHDL Simulation Model

After generating the VHDL model, please refer to the following steps to simulate the design model.

Step 1: Create the working library:

It is necessary to compile any VHDL model through ModelSim.

vlib work

Step 2: Compile the VHDL design:

vcom <name>.vhd

where ***<name>.vhd*** is the VHDL model.

Step 3: Instantiate the VHDL model within a test bench:

You can reference <name>_pkgs by using the clause:

Use work.<name>_pkgs.all;

You are then ready to compile the test bench:

vcom test-bench.vhd

Step 4: Run the simulator:

vsim

ModelSim will trigger a pop-up GUI window. Please refer to the ModelSim user manual for more details.

However, the retain time is not supported in the VHDL vital. While generating the SDF file, the users might ignore the information on the retain time, or use SDF 2.1 instead.

3.4 Using Synopsys Synthesis Model

After generating the Synopsys model, please refer to the following steps to simulate the design model.

Step 1: Initiate the Synopsys design compiler environment:

dc_shell

Step 2: Please follow the steps in the Synopsys commands to include the Synopsys model

read_lib <name>_<case>.lib

write_lib <name>_<case>

link_library= <name>_<case>.db

target_library= <name>_<case>.db

read –f verilog design.v

write_timing –context verilog –f sdf –v2.1 –o output

where ***<name>_<case>*** is the name of the Synopsys library, ***<name>_<case>.lib*** is the Synopsys model, ***design.v*** is the top-level netlist, and ***output*** is the name of the output file. Faraday provides three-corner models to the customers for the design synthesis. Please setup three-corner case as: <WC>: worst-case; <TC>: typical-case; <BC>: best-case

Step 3: Please invoke the Synopsys PrimeTime environment when using PrimeTime to generate a SDF:

pt_shell

Step 4: Please execute the following steps in the Synopsys commands to generate a SDF:

read_db <name>_<case>.db

set link_path <name>_<case>.db

read_verilog design.v

write_sdf –version 2.1 –o output

3.5 Using LEF P & R Model

After generating the LEF model, please refer to the following steps to input the LEF model.

Step 1: Invoke Cadence silicon ensemble environment.

Step 2: Please type the command in its command window:

INPUT LEF FILENAME "<path>/<name>.lef"

where ***<path>*** is the path to the LEF model and ***<name>.lef*** is the LEF model. This creates the block and pin information in the silicon ensemble for placing and routing.

3.6 Using P & R Model of Milkyway FrameView

After generating the LEF model, please refer to the following steps to translate the LEF model to Milkyway FrameView.

Step 1: Create the definition file of the cell type and name it as "lef2Arcs.map":

This file contains one instance per line in the form:

gdsMacroCell ***<name>***

where ***<name>*** is the name of the memory block instance.

Step 2: Invoke the Synopsys Milkyway environment, please enter the command in the command window

auNLIApi

In the command window, please fill the form with the library name, LEF file name, and lef2Arcs.map, and click "OK" to generate the cell view.

Step 3: Run "Blockage, Pin & Via (BPV)" to create the frame view.

3.7 Using TLF and CLF P & R Timing Model

After generating the Synopsys model without the IDDQ, please follow the steps below to generate the TLF model.

Step 1: Invoke the Cadence silicon ensemble environment.

Step 2: Please type the command in the Unix command window:

syn2tlf –o <name>_<case>.tlf <name>_<case>.lib

where ***<name>_<case>.lib*** is the Synopsys model, and ***<name>_<case>.tlf*** is the name of the output file.

After generating the Synopsys model without the IDDQ, please follow the steps below to generate the CLF model.

Step 1: Invoke the Synopsys Apollo environment.

Step 2: Please type the command in the Unix command window:

libc –o <name>_<case>.clf <name>_<case>.lib

where ***<name>_<case>.lib*** is Synopsys model, and ***<name>_<case>.clf*** is the name of the output file. The converter will divide the output into three sections.

<name>_<case>.clf.time: For the timing information

<name>_<case>.clf.logic: For the logic function

<name>_<case>.clf.power: For the power information

3.8 Using LVS Netlist, GDSII Layout, and H-Cell List

After generating the LVS netlist, the GDSII layout, and H-Cell list, we recommend that you use these deliverables to verify the conjunction. You may use the verification tools such as Cadence Dracula, or Mentor Graphic Calibre to compare between the GDSII and LVS netlist. However, the LVS netlist should be combined onto the chip-level netlist when the chip is fully assembled. This precautionary action ensures that the P & R (Place & Route) tools cause no circuit shorts or open circuits in your chip. The H-Cell list file is a cell correspondence file for Mentor Calibre hierarchical LVS comparison.

You could refer to the following usage to include your H-Cell list while working on the hierarchical LVS verification:
calibre –lvs –hcell ***fsa0a_d_sl.hcell***
where ***fsa0a_d_sl.hcell*** is generated along with GDSII selection from Memaker.

Please use this hierarchical correspondence information while working on the hierarchical LVS verification per the requirement of the tool.